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NORTHEAST ELECTRONICS CORPORATION

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LONG LINE EQUIPMENT TESTING ANNEXE
ROOM 224 10 LONSDALE ST.
MELBOURNE VIC. 3000

P.M.G. Department
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INSTRUCTION MANUAL

LLE
642

FOR

LONG LINE EQUIPMENT TESTING ANNEXE
ROOM 224 10 LONSDALE ST.
MELBOURNE VIC. 3000

MODEL 58B
IMPULSE COUNTER AND NOISE MEASURING SET

LLE 642

ISSUE 1

NORTHEAST ELECTRONICS CORPORATION

P.O. BOX 649 – CONCORD, N.H. 03301

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SECTION 1

DESCRIPTION

1.1 GENERAL DESCRIPTION. The Model 58B is an impulse counter and noise measuring set utilizing digital readout and high speed integrated logic circuits to measure impulse noise distribution from 20 to 107 dBrn at four threshold levels at a count rate adjustable from 4/sec. to 40,000/sec. A control provides for selection of threshold level separations of 2, 4 or 6 dB. A built-in timer permits selection of observation periods up to one hour.

1.2 At the same time the set will measure the RMS value of steady state noise from 0 to 100 dBrn, weighted, flat, or longitudinal noise-to-ground.

1.3 Three internal weighting networks, C MSG, flat, and 10.2-51 kHz for 40.8 kilobit data systems are provided. Connections for external networks are also available with flat response to 108 kHz.

1.4 Input impedances of 135, 150, 600, and 900Ω, bridging or terminated, with excellent common mode rejection are provided, plus dial through capability with holding circuit.

1.5 An output monitor, with flat response to 108 kHz provides a means for observing or recording the signal being measured.

1.6 A phase jitter and phase hit measuring accessory, Model 58BXPJ, in a matching cover, is also available on an optional basis.

1.7 The unit operates from 115 or 230V ac, weighs 27 pounds and measures $14\frac{1}{2}$"w x 12"h x 9 3/8"d. A relay rack-mounted unit designated 58BR is also available.

SECTION 2

SPECIFICATIONS

SENSITIVITY

Impulse Noise: 20 dBrn to 107 dBrn
Circuit Noise (Metallic): 0 dBrn to 99.9 dBrn

ACCURACY (Impulse)

Impulse Noise:

C Msg ±1 dB	20 to 107 dBrn
FLAT ±1 dB	20 to 107 dBrn
10.2-51 kHz ±1 dB	30 to 107 dBrn
Ext (Wide Band) ±1 dB	30 to 107 dBrn

COUNTING RATE

Blanking interval adjustable from 0.25 seconds to 25μs, in four decade ranges coupled with a vernier control.

Accuracy: ±20% of vernier setting.

INPUT IMPEDANCE

Without balance transformer: ±5% < 10°
100 Hz - 108 kHz

With balance transformer:
900 ±5% <10° 100 Hz-25 kHz
600 ±5% <10° 100 Hz-50 kHz
150 ±5% <10° 100 Hz-108 kHz
135 ±5% <10° 100 Hz-108 kHz

Bridging (at 1 kHz):
25,000Ω without balance transformer
12,000Ω with transformer

Noise to Ground:
Across Line 41,000Ω
To Ground 50,000Ω

HOLD CIRCUIT

DC resistance 700Ω ±10%

INPUT DC BLOCKING

Input DC blocked for 150 V dc with or without input transformer.

COMMON MODE REJECTION

With balance transformer:
>80 dB 50 Hz to 10 kHz
Without balance transformer:
>70 dB 100 Hz to 10 kHz
>50 dB 50 Hz to 108 kHz

MONITOR OUTPUT

Monitor output impedance: 600Ω nominal
Output level adjustable from approximately 0 dBm to -40 dBm into 600Ω load.

POWER REQUIREMENTS

115V ac or 230V ac, 50/400 Hz
approx. 10 watts

SIZE: 14½" w x 12"h x 9 3/8"d

WEIGHT: 27 lb.

CIRCUIT NOISE (STEADY STATE):

Network	Test Freq.	Accuracy	
C Msg	1 kHz	±0.5 dB	0 to 99.9 dBrn
FLAT	1 kHz	±0.5 dB	10 to 99.9 dBrn
FLAT	1 kHz	±1.0 dB	0 dBrn
10.2-51 kHz	25 kHz	±0.5 dB	10 to 99.9 dBrn
10.2-51 kHz	25 kHz	±1.5 dB	0 dBrn
Ext (Wide Band)	25 kHz	±0.5 dB	10 to 99.9 dBrn

NOISE TO GROUND 40 dBrn to 139.9 dBrn Accuracy: ±1.0 dB

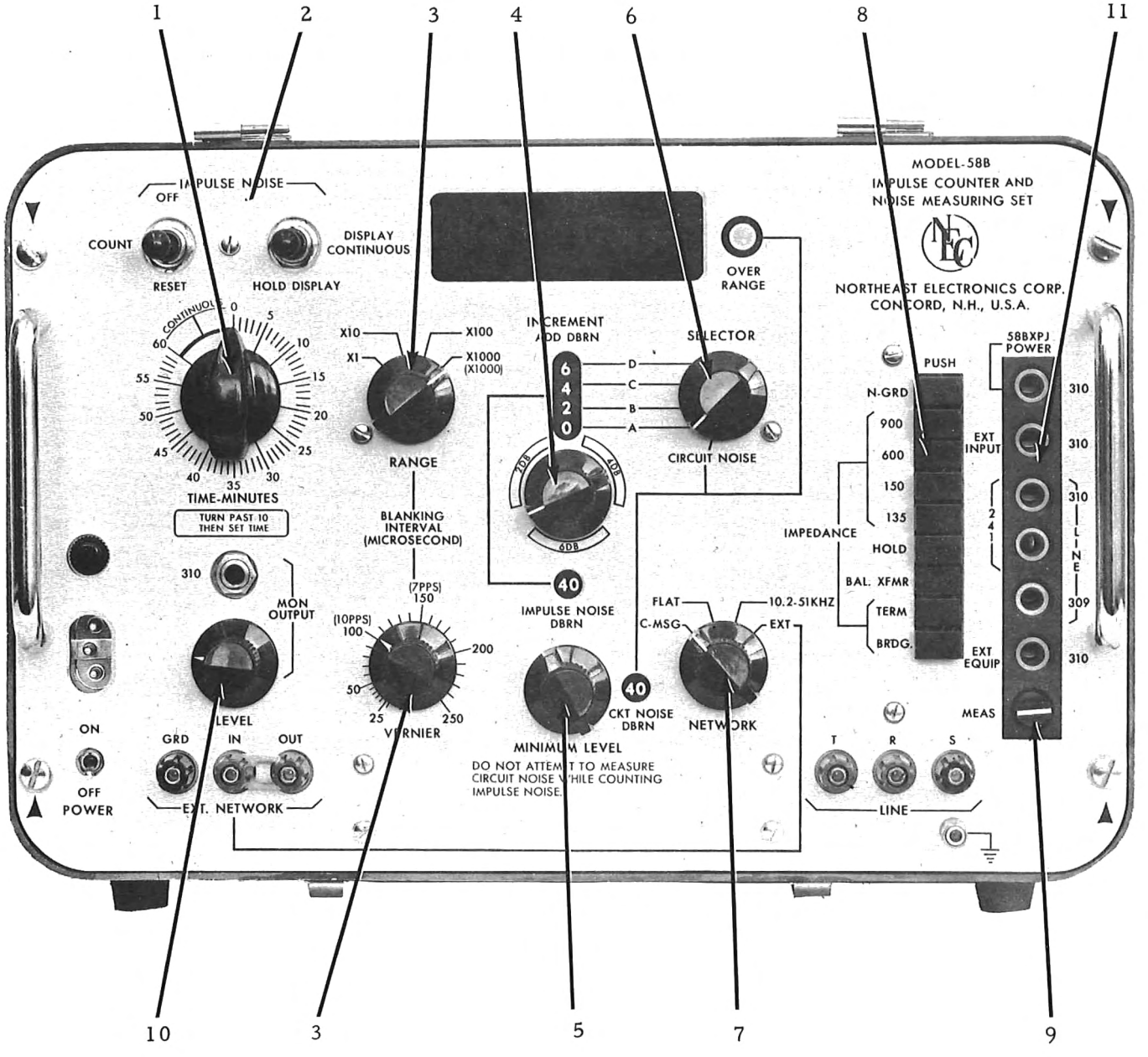

Figure 3-1 Front Panel Controls.

OPERATING INSTRUCTIONS

3.1 FRONT PANEL CONTROLS (Refer to Fig. 3-1).

Name of Control	Function
1. TIME-MINUTES	60 minute timer (A 30 minute timer is optional). Both provided with a continuous operating position.
2. IMPULSE NOISE	RESET-OFF: Resets all impulse counting logic to zero or disables counting logic until released. HOLD or CONTINUOUS DISPLAY: Allows display to follow the impulse count sequence or holds display until released without interrupting the count.
3. BLANKING INVERVAL	VERNIER: Adjusts desired blanking interval in microseconds. RANGE: Selects desired decade multiplier.
4. INCREMENT (Impulse Noise)	Attenuator provides for 2, 4, or 6 dB spread between the four threshold levels and scaled by 0, 3, 6 and 9 dB. Results in 12 different threshold combinations.
5. MINIMUM LEVEL	Attenuator, 0 to 90 dBrn in 10 dB steps for circuit noise measurements. Attenuator, 20 to 80 dBrn in 10 dB steps for impulse noise measurements.
6. SELECTOR	Selects levels of A, B, C, D or circuit noise measuring circuits.
7. NETWORK	Selects C MSG, FLAT, 10.2-51 kHz or external network.
8. INPUT (pushbutton switch)	Provides for selecting the following: Impedance 135, 150, 600 or 900Ω Bridging or terminate Noise-to-Ground (N-GND) Hold circuit Balance transformer
9. MEAS (Turnbutton switch)	Provides for connecting line circuit to external equipment (Dial, etc.)
10. LEVEL (Mon output)	Provides for adjusting monitor output to desired level.
11.	Jacks are provided for type 241, 309 and 310 plugs for Line, External Equipment and accessories.

3.2 OPERATION. Connect an AC cord to the 115V ac line. Turn power switch on.

CAUTION: If unit is to be operated from a 230V ac source, proceed as follows:

1. Remove four captive screws on front panel.

2. Remove unit from case.

3. Locate S12, 115-230V ac selector switch mounted on partition - upper left-hand corner and place switch in 230 position.

4. Replace unit in case and secure captive screws.

5. Connect an AC cord to the 230V ac line. Turn power switch on.

3.3 Connect the external line to be tested to the appropriate line jack or to the line tip-ring-sleeve binding posts. A type 309, type 310, type 241 or a twin banana plug can be used to establish connection to the 58B input circuit.

3.4 If the line connection is to be dialed:

a. Connect a dial or telephone to the EXT EQUIP jack. A 310 type plug must be used.

b. Place MEAS turnbutton switch in vertical position. This transfers all line jacks to the EXT EQUIP jack.

c. Depress corresponding pushbuttons for desired functions. i.e. 900, TERM, HOLD, BAL XFMR.

d. Dial the desired number.

e. When line connection has been established, place MEAS turnbutton switch in the horizintal position.

f. The dial may now be removed. The internal hold circuit will maintain the connection.

3.5 Set NETWORK switch to desired weighting characteristics. If an external network is to be used, remove shorting link between IN and OUT binding posts and make appropriate filter connections to these binding posts. External network to be used should be for 600Ω impedance and have an insertion loss of approximately 0.6 dB. Filters with other insertion losses can be used with the difference added to or subtracted from the sensitivity settings of the Model 58B.

3.6 To set sensitivity (circuit noise measurement). It is strongly advised that circuit noise, metallic and/or noise-to-ground measurements be made separately and not simultaneously with impulse noise tests. Set SELECTOR switch to CIRCUIT NOISE position.

a. If readout display is extinguished and OVER RANGE lamp is on, decrease sensitivity by setting MINIMUM LEVEL control to a higher number until lamp goes out. Simultaneously, the readout display will be illuminated.

b. If both the OVER RANGE lamp and readout display are extinguished increase sensitivity by setting MINIMUM LEVEL control to a lower number until readout display becomes illuminated. Allow at least one second interval between steps when adjusting MINIMUM LEVEL control.

c. Read display directly.

d. If noise-to-ground measurement is to be made, push N-GND pushbutton and add 40 dB to reading.

3.7 To set sensitivity (impulse measurement). The sensitivity of each of the four impulse channels - A, B, C and D - is

The sum of the MINIMUM LEVEL control setting and the individual INCREMENT control setting. The INCREMENT control automatically sets the threshold of each channel simultaneously.

i.e.

Min. Level (Imp. Noise dBrn)	Increment (Threshold setting)	Channel	Channel Sensitivity
40	12	D	52 dBrn
40	8	C	48 dBrn
40	4	B	44 dBrn
40	0	A	40 dBrn

3.8 Set SELECTOR switch to CHANNEL A.

3.9 a. Set blanking interval. Adjust the VERNIER and RANGE controls to equal the bit period. i.e. Bit rate = 1800 per second. 1 bit period = approx. 556μs. To convert bit rate to 1 bit period:

$$\text{1 bit period (seconds)} = \frac{1}{\text{bit rate}} = \frac{1}{1800} = .000556 \text{ sec.}$$

1. Set VERNIER to approximately 55 on dial.

2. Set RANGE to X10. This is approximately 550μs.

b. To set blanking interval for a maximum count rate of 10 pps, (same as TTS 58A):

1. Set VERNIER to 100 on dial.

2. Set RANGE to X1000. This is approximately 0.1 second or 100,000μs.

c. To set blanking interval for a maximum count rate of 7 pps:

1. Set VERNIER to approximately 143 on dial.

2. Set RANGE to X1000. This is approximately 0.143 seconds or 143,000μs..

3.10 Set timer to desired time in minutes.

3.11 Immediately and momentarily depress the COUNT/RESET key switch to the RESET position. This resets all counters to 0 and establishes the start of the impulse noise test.

CAUTION: From the start and during the course of an impulse noise test, DO NOT readjust or activate any control or controls other than the MON output level control, DISPLAY keyswitch or SELECTOR switch as this may cause the instrument to accumulate erroneous counts.

The SELECTOR switch may be activated to observe accumulated counts on any channel at any time, but DO NOT advance selector to CIRCUIT NOISE position.

3.12 During an impulse noise test, accumulated counts on any one or all four channels can be observed and recorded at any precise moment by activating the DISPLAY switch to the HOLD position. The DISPLAY switch must be released and reactivated as each channel is observed.

3.13 At the end of test, when mechanical timer has returned to 0, set SELECTOR switch to each channel and record individual readings. i.e. (see paragraph 3.7):

Min. Level (Impulse Noise dBrn)	Increment (Threshold setting)	Channel	Channel Sens.	Readings (Impulse Hits)
40	12	D	52 dBrn	21
40	8	C	48 dBrn	43
40	4	B	44 dBrn	92
40	0	A	40 dBrn	186

Readings indicate that a total of 186 impulse hits exceeded a threshold level of 40 dBrn; 92 of these exceeded a threshold level of 44 dBrn; 43 exceeded a threshold level of 48 dBrn and 21 exceeded a level of 52 dBrn.

3.14 TO MONITOR

a. Plug headset into the MON OUTPUT jack. This jack will accept a 310 type plug. Signal is to tip; ring and sleeve are ground.

b. Adjust MON OUTPUT for desired level.

c. Monitor output response is determined by NETWORK switch.

SECTION 4

CIRCUIT DESCRIPTION

4.1 INPUT CIRCUIT LINE SECTION (See Fig. 7-2)

a. The balanced input circuit provides a choice of connectors for establishing connection to a line. Turnbutton switch S-1, connects all line Jacks to the EXT EQUIP jack for dialing purposes.

b. The hold circuit, made up of resistors R101, R102 and inductor L1, is placed across the line by activating switch S-17.

c. Resistors R106 through R109 and R111 through R114 are used as terminating resistors. The selectable termination is made up of a pair of resistors appearing across the input line terminals via the BRDG/TERM switch S-19 and S-20. Capacitor C2, in series with the terminating resistors provide dc blocking up to 150 V.

d. Resistors R103, R104, R105 and R110 constitute a 40dB balanced attenuator for longitudinal noise measurements.

e. Activating switch S-18 places the input balance transformer T-2 across the line for maximum longitudinal rejection to low frequencies. The transformer is connected for a 1.1 transfer of the input signal with minimal loss.

f. Resistors R29 and R30 are used to equalize the terminated impedance appearing across the line when the input balance transformer T-2 is in the out position. With T-2 out of the circuit, capacitors C102 and C103 provide dc blocking up to 150 V.

4.2 INPUT BALANCED AMPLIFIER (See Fig. 7-2)

a. The amplifier presents a balanced input to the line when the transformer T-2 is not in the circuit, and has an input impedance of 24.8Kohm, the resistance of R115 and R116.

b. Intergrated circuit IC101 and the emitter follower transistor Q102 constitute the voltage amplifier. The gain is set at 20dB when the MINIMUM LEVEL control is in the 0 to 40 dBrn positions, and a loss of 10dB when in the 50 to 90 dBrn. positions. As a 20dB amplifier, the gain is controlled by resistors R115 and R117. When relay RY102 is energized, resistors R118 is placed in shunt with R117 thus increasing the negative feedback by 30dB with a net gain of -10dB.

c. Input balance is maintained by keeping the ratio of the voltage divider, R116 and the branch R119 through R124, equal to the ratio of the voltage divider, R115 and R117, R118. The relay RY101 is operated when relay RY102 is energized. Variable capacitors C104, C105, C106, and potentiometers R121 and R122 provide the means for optimizing the input balance.

d. Resistors R129 through R135 form voltage dividers for impedance level equalization. Relays RY103, RY104 and RY105 are individually activated when the corresponding input impedance is selected.

4.3 WEIGHTING NETWORKS (See Fig 7-3)

a. The C-MSG weighting characteristics are determined by the passive elements of the filter. Transistors Q201 and Q202 constitute a voltage amplifier with approximately 14dB of gain which compensates for the insertion loss of the passive filter. The variable resistor R210 is used for adjusting the overall gain of the C-MSG. Network.

b. The 10.2 to 51KHz bandpass filter network is a cascaded high pass, low pass filter with approximately 18dB/ octave slopes.

c. In the Flat weighting network, capacitor C217 limits the high frequency response with a 6dB/octave roll-off. Resistors R215, R216 introduce an adjustable amount of loss, (typically 0.6dB) for level equalization.

d. The impedance for the networks, is 600 ohms for both source and load. The 600 ohm source impedance is provided by the voltage dividers for impedance equalization. The 600 ohm "L" pad attenuator (switch S3, deck 7)provide the load impedance This "L" pad attenuator controls a total of 30dB of attuation in 10dB steps common to all modes of operation.

4.4 BUFFER AMPLIFIER (See Fig.7-3)

a. The intergrated circuit IC201 and the emitter follower Q203 constitute a voltage amplifier with an adjusted gain of approximately 26dB. The gain adjustment control, R219 has a range of approximately ±2dB.

b. Diodes, CR201 through CR206 are used as limiters and thus limit the output voltage swing to approximately 2 volts, peak to peak.

c. The output of the amplifier is connected to two 1000 ohm "L" pad attenuators. One attenuator (switch S5, deck 5) controls a total of 9dB attenuation in 3dB steps common to all four impulse channels. The second attenuator, (switch S3, deck 2) controls 30dB of attenuation in 10dB steps common only to the circuit noise channel.

4.5 AMPLIFIER, CIRCUIT NOISE (See Fig. 7-4)

a. The intergrated circuit, IC901 is a voltage amplifier with an adjusted gain of approximately 47dB. A range of approximately ±2dB is provided by the gain adjustment control, R905. The output is connected to the monitor output level control R2 through R935.

b. The single stage transistor amplifier Q901 is designed to deliver a maximum of 0dBm into a 600 ohm load. The output impedance is approximately 600 ohms.

4.6 A.C. to D.C. CONVERTER (See Fig. 7-4)

a. The output of the intergrated circuit amplifier IC901 is connected to the A-D converter via coupling capacitor C905, resistor R906 and capacitor C908.

b. Transistors Q902 and Q903 form a cascade amplifier. Transistor Q902 is connected in a common emitter configuration and Q903 in a common base configuration.

c. The collector of Q903 drives two types of detector circuits. The first, an average detector made up of diodes CR901, CR902, resistors R919 through R922 and capacitors C914 and C915. Negative feedback is taken from this average detector.

d. The second detector is a combination average and peak detector which results in an RMS value of the signal being detected. Transistor Q904 is an emitter follower and supplies the power neccessary to drive the low impedance detector diode/resistor combinations, CR903, R917 and CR904, R923.

e. The RMS detector outputs are connected to a balanced DC amplifier, IC902. The dc gain of this amplifier is determined by R925 and the series-parallel combination R928, R929 and R930. The gain control, R929, is used as a means for adjusting the dc threshold voltage.

f. The resistor-capacitor combination, R932 and C922 is used to reduce the ripple at the lower frequencies.

4.7 D.C. TO LOG CONVERTER (See Fig. 7-5)

a. The intergrated circuit IC706 and associated circuitry function as the D.C. to log converter. When switch Q704 is open and switch Q705 is closed capacitor C706 charges linearly through closed switch, Q706 to a given positive voltage determined by the level of the negative voltage at the input (TP11.12).

b. The slope at which capacitor C706 charges for a given dc voltage is a function of the value of the charging capacitor C706 and the resistor R717.

c. The D.C. voltage limits from the output of the A.C. to D.C. converter, corresponding to an operating dynamic range of 12dB, is approximately -1.5 V dc to -6.0 Vdc.

d. A reference voltage of +1.5 Vdc sets the threshold at which the capacitor, C706 will charge to a positive voltage. This reference voltage is derived from the voltage divider R705, R706 and R707.

e. When the input negative voltage is below the dynamic range, less than -1.5 Vdc, the capacitor C706 is effectively disconnected from the charging circuit and remains uncharged. This condition occurs whenever the summing junction, pin 4 of IC706 is positive respect to ground, and causes the output of IC706 to saturate at -12 Vdc. The output of IC706 is connected to the inverting input, pin 4 of IC707 and results in its output to saturate at approximately +12 Vdc. This turns off the switch Q706 and effectively opens the charging path.

f. In the reverse condition, when switch Q704 is closed and switch Q705 is open, the capacitor C706 has an accumulated positive charge.

g. The negative voltage from the AC to DC converter is effectively disconnected from the summing point of IC706, and a discharge path connected around capacitor C706. This discharge path consists of resistors R714, R715 and transistor Q704.

h. The capacitor, C706, discharges at a logarithmic rate with the discharge time being a function of resistors R714 and R715. The variable resistor R15 provide the means for calibrating the upper end of the 12dB dynamic operating range.

i. Resistors R712 and R713 in the base circuit of Q704 regulate the base current being injected into the discharge circuit. The effect of this base current on the discharge time is non-linear and has the least effect when the capacitor is charged to a maximum value. This provides an adjustment for calibrating the lower half of the 12dB dynamic operating range.

4.8 CONVERTER CONTROL LOGIC. The control logic for the D.C. to log converter is derived from a 440Hz clock frequency provided by the astable multivibrator, Q701 and Q702. During the charging cycle of capacitor C706, the multivibrator frequency is counted by IC701, IC702 and IC705, providing the necessary digital division.

4.9 At a count of 200, the Q output, pin 9 of IC705 provide a high to low transition to the clock input, pin 1 of the second flip-flop and causes $\overline{Q}$, pin 13 to go from high to low. This in turn reverses the switch condition and initiates the discharge cycle.

4.10 During the discharge cycle, the multivibrator frequency signal continues to be counted and stored by the two decade counters, IC701 and IC702. The accumulated count is a direct function of the discharge cycle period and in turn is a function of the initial charged potential of the capacitor C706. When capacitor C706 discharges to zero, pin 10 of IC706 goes slightly negative causing pin 10 of IC707 to switch from -12 to +12 Vdc. This transition is differentiated by the RC combination R731 and C715 and the resulting differentiated pulse used to trigger the Transfer and Reset Pulse Generator, IC703. (See Fig 4-1)

4.11 The binary count which has accumulated in the two decade counters, IC701 and IC702 during the discharge cycle is the information which appears at the input of the latches, IC537 and IC538 via the gate matrix, IC533 and IC534. The transfer pulse generated, clocks the four quad bi-stable latches and transfers the information to the output of the latches. This information is then committed to memory until new information is transfered. The transfer pulse appears at pin 2 of IC703 and is connected to pins 4 and 13 of IC537 through IC540.

4.12 Immediately following the transfer pulse, a reset pulse is generated which resets the two decade counters IC701 and IC702 to a binary count of zero. This reset pulse appears at pin 14 of IC703 and is connected to pins 2 and 3 of the decade counters. Simultaneously, a second reset pulse is generated which is used to clear the two flip-flops, IC705. This causes $\overline{Q}$ pin 13 of the second flip-flop to go from low to high. This again reverses the switch condition of Q704 and Q705 and establishes the start of a new charge cycle. This second reset pulse appears at pin 13 of IC703 and is connected to pin 12 of IC704 and pins 2 and 6 of IC705. The transistor Q703 is used to provide a +12 V logic level and necessary inversion to properly operate transistors Q704 and Q705.

4.13 The decade counters IC701 and IC702 provide the binary information for the tenths digit and the units digit respectively. The binary information for the tens digit is derived from a combination of a two bit full adder manually programmed by the MINIMUM LEVEL CONTROL S-3 (decks 3,4,5 and 6) and follows the truth table described in fig.4-2. The binary information for the tens digit appears at the input of the latch IC539 via gate matrix IC536. (See Fig 4-5) Only these three digits are used when reading circuit noise. The fourth digit is extinguished. A decimal point is controlled by the SELECTOR switch S-4 (deck 3A) and appears between the tenths digit and the units digit when in the CIRCUIT NOISE position.

4.14 OVER RANGE AND READOUT CONTROL LOGIC.

4.15 An overrange condition is said to exist whenever the negative input d.c. voltage at the drain of Q705 exceeds the -6 Vdc level which corresponds to the upper limit of the 12dB dynamic range.

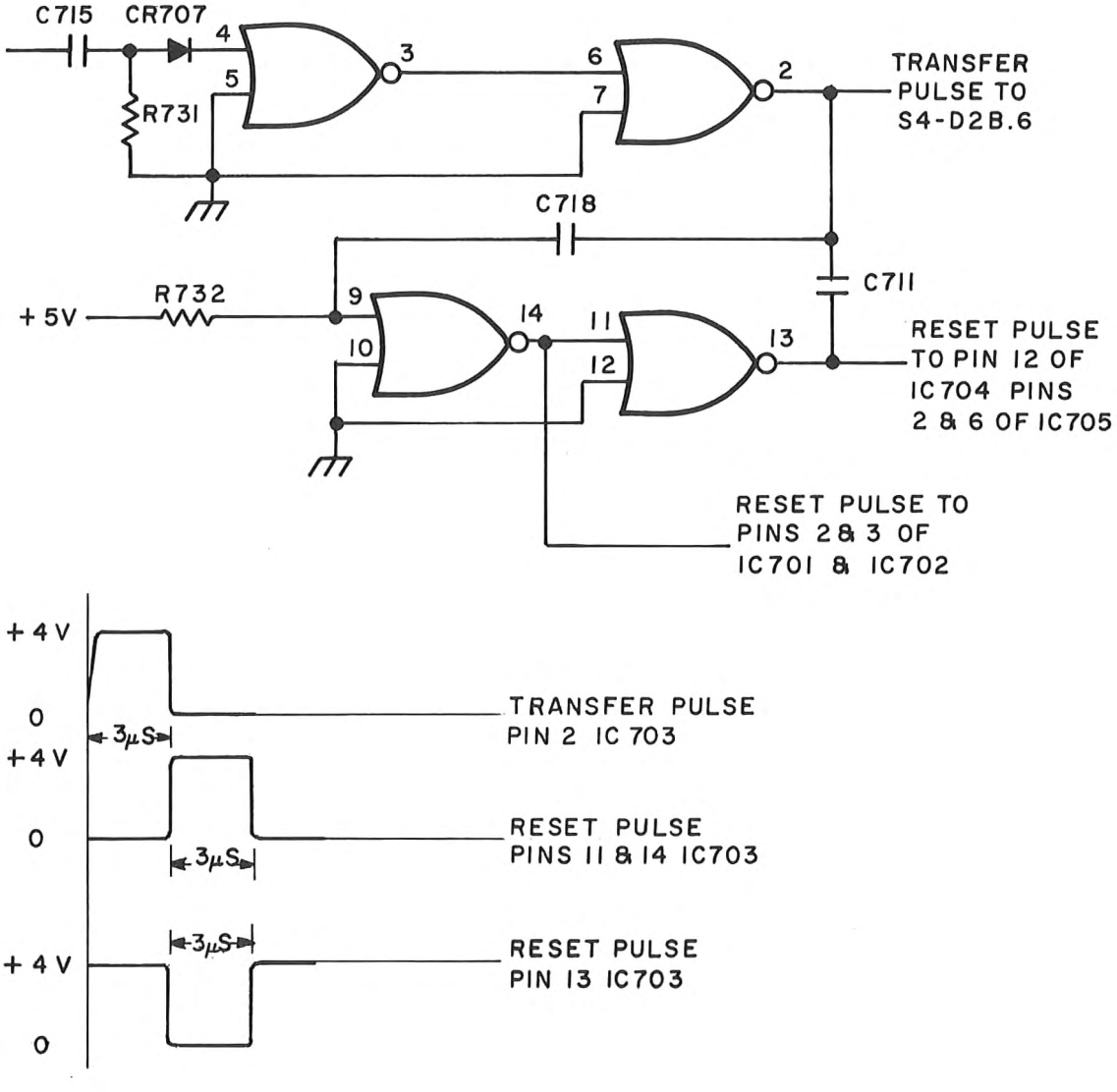

Figure 4-1 Transfer and Reset Pulse Generator.

	0	1	1	2	2	3	3	4	4	5	5	6	6	7	7	8	8	9	9	X	TENS DIGIT READOUT
C IN	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	SPILLOVER PULSE FROM PIN 9 IC705
A	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	TENS DIGIT BINARY INFORMATION TO GATE MATRIX
B	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	
C	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	
D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	
C2	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	PIN 10 IC535
Σ2															1	0					PIN 12 IC535

C IN = SPILLOVER PULSE AT A COUNT OF 300 UPDATES
TENS DIGIT TO NEXT HIGHER NUMBER

BINARY INFORMATION A AND B DERIVED FROM TWO BIT FULL ADDER IC535
BINARY INFORMATION C AND D DERIVED FROM S-3 DECK 5 AND 6

MINIMUM LEVEL CONTROL SETTING										
dBRN	0	10	20	30	40	50	60	70	80	90
S 3	LOGIC LEVELS									
DECK 3	0	1	0	1	0	1	0	1	0	1
DECK 4	0	0	1	1	0	0	1	1	0	0
				C_2				Σ_2		
DECK 5	0	0	0	0 / 1	1	1	1	1 / 0	0	0
								C_2		
DECK 6	0	0	0	0	0	0	0	0 / 1	1	1

0 = GROUND
1 = +5VDC

C_2, Σ_2 } WHERE INDICATED, LOGIC LEVELS DERIVED FROM IC535

Fig. 4-2 Truth Table

At exactly 12dB above threshold, the logic extinguishes the readout tubes and illuminates the overrange lamp DS-2. An overrange condition causes the capacitor C706 to charge to a higher voltage, resulting in a discharge period equal to or greater than an accumulation of 320 counts in decade counters IC701 and IC702. NOTE: The first 200 counts during the charge cycle of capacitor C706 is ignored and does not appear in the final reading. The accumulation of 320 counts corresponds to 12.0dB. Normally, the reset pulse from the Transfer-Reset Pulse Generator IC703 connected to the clock input, pin 12 of IC704, continues to clock the fixed logic levels at the J & K input and keeps the Q output, pin 8, at a logical zero. When an overrange condition exists, the reset pulse connected to the clock input pin 12 of IC704 is overriden by a pulse connected to the PRESET, pin 13 and allows the Q output, pin 8, to go to a logical 1 level which turns on transistors Q707 and Q711. (See table on page 4-11)

4.16 (See Fig. 4-3) The reset pulse W3 assures that the Q outputs of the dual flip-flop IC705 are at logical zeros at the start of each charge cycle of capacitor C706. The spillover pulses W2, from pin 11 of IC702 occur at each 100 counts. The first spillover count which occurs during the charge cycle causes the Q output pin 9 of IC705 to go to a logical 1. The second spillover count which occurs at an accumulated count of 200 causes the Q output pin 9 of IC705 to go from a high to a low. (See W4). This high to low transition causes the Q output pin 12 of IC705 to go to a logical 1. (See W5).

4.17 If the discharge cycle period corresponds to an accumulated count of 300 or more, a third spillover count occurs and causes the Q output pin 9 of IC705 to go to a logical 1. (See W4). This results in both Q outputs of IC 705 to be at a logical one level and this condition is recoginzed by applying this information to a three input NAND gate IC305. (See Fig. 4-4)

4.18 An accumulation of 320 counts or greater is recognized by OR-ing the B and C outputs of the tens digit latch, resulting in a logical one level at the junction of R517, CR501 and CR502 This information is applied to the third input of IC305. (See Fig. 5). with logical one levels present at the inputs of the NAND gate IC305, the output of IC305, pin 8 goes from high to low and a preset pulse is generated. (See W7). This preset pulse overrides the reset pulse present at the clock input, pin 12 and sets the Q output of IC704 pin 8, to a logical 1. (See W8). The preset pulse continues to override the reset pulse and keeps the Q output of IC704 pin 8 at a logical 1, holding Q707 and Q711 in an "ON" condition.

4.19 One other overrange condition exists in addition to the one described in par. 4.17. When the MINIMUM LEVEL CONTROL S-3 is in the 90dBrn position. In this position, the operating dynamic range is restricted to 10dB. At exactly 100dBrn, the readout tubes are extinguished and the overrange lamp DS-2 is illuminated (See Fig. 4-5).

4.20 The tens digit is manually programmed by the MINIMUM LEVEL CONTROL S-3 (decks 3,4,5 and 6) A binary count of 9 is programmed when S-3 is in the 90dBrn position, and this binary information appears at the output of the latch, IC539 via gate matrix IC536. When the capacitor C706 discharge cycle period corresponds to an accumulated count of 300 or more, a logical one level is made to appear at the Q output, pin 9 of IC705. (See Fig. 3 W4 shaded area) This pulse is applied to pin 5, C in, of the 2-Bit Full Adder, IC535, and

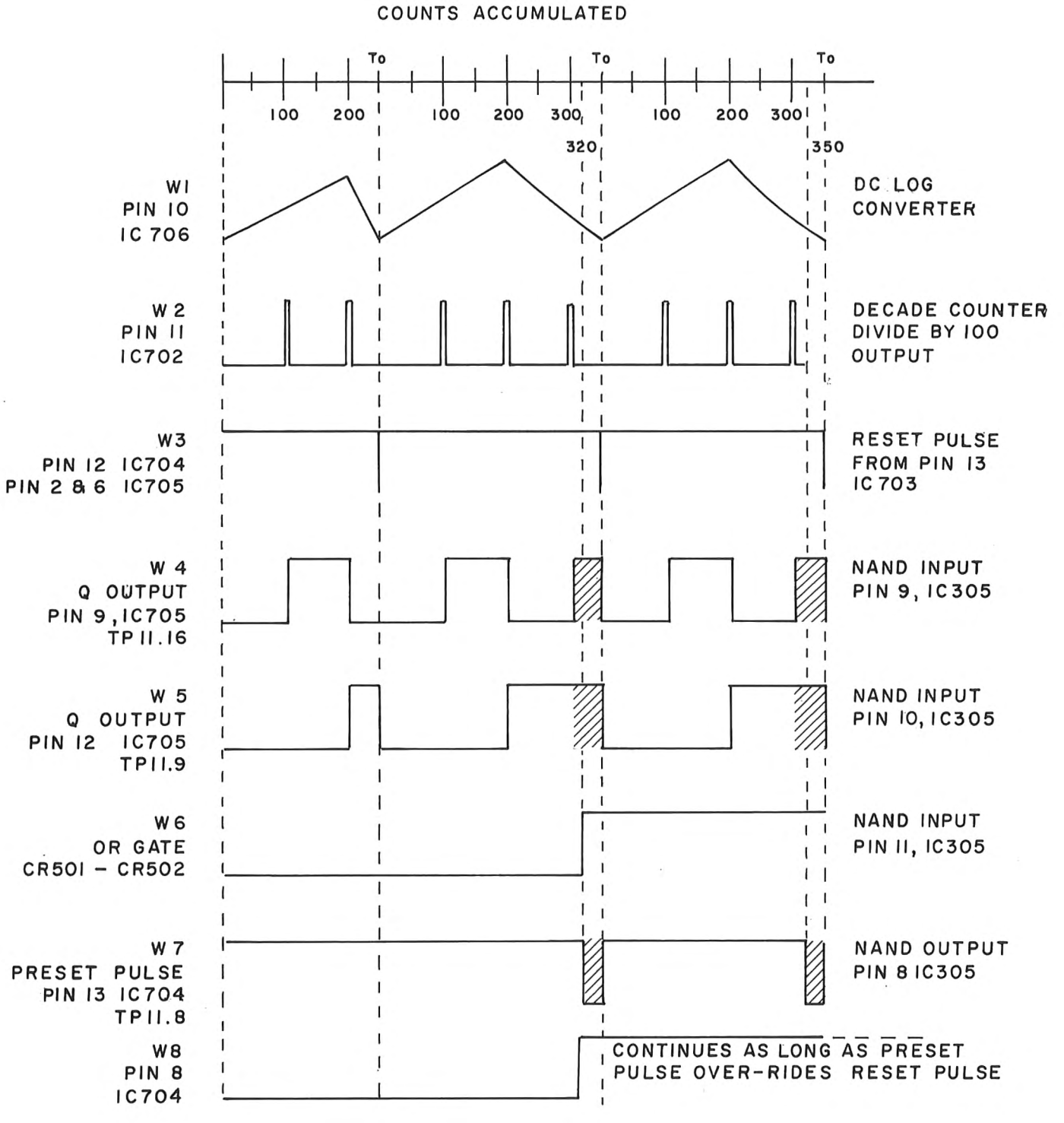

Figure 4-3 DC to LOG Converter Logic

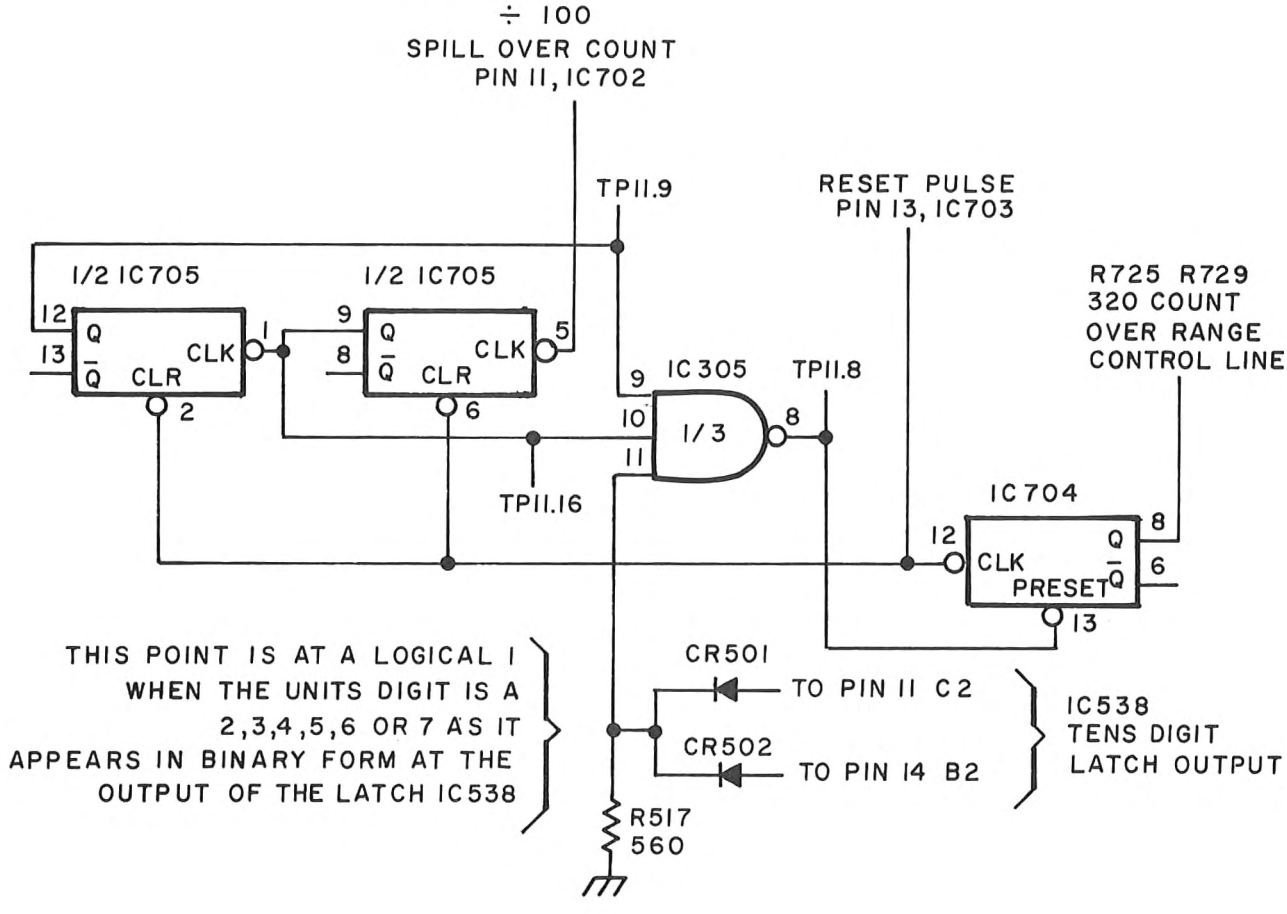

Figure 4-4 12dB Over Range Logic Schematic

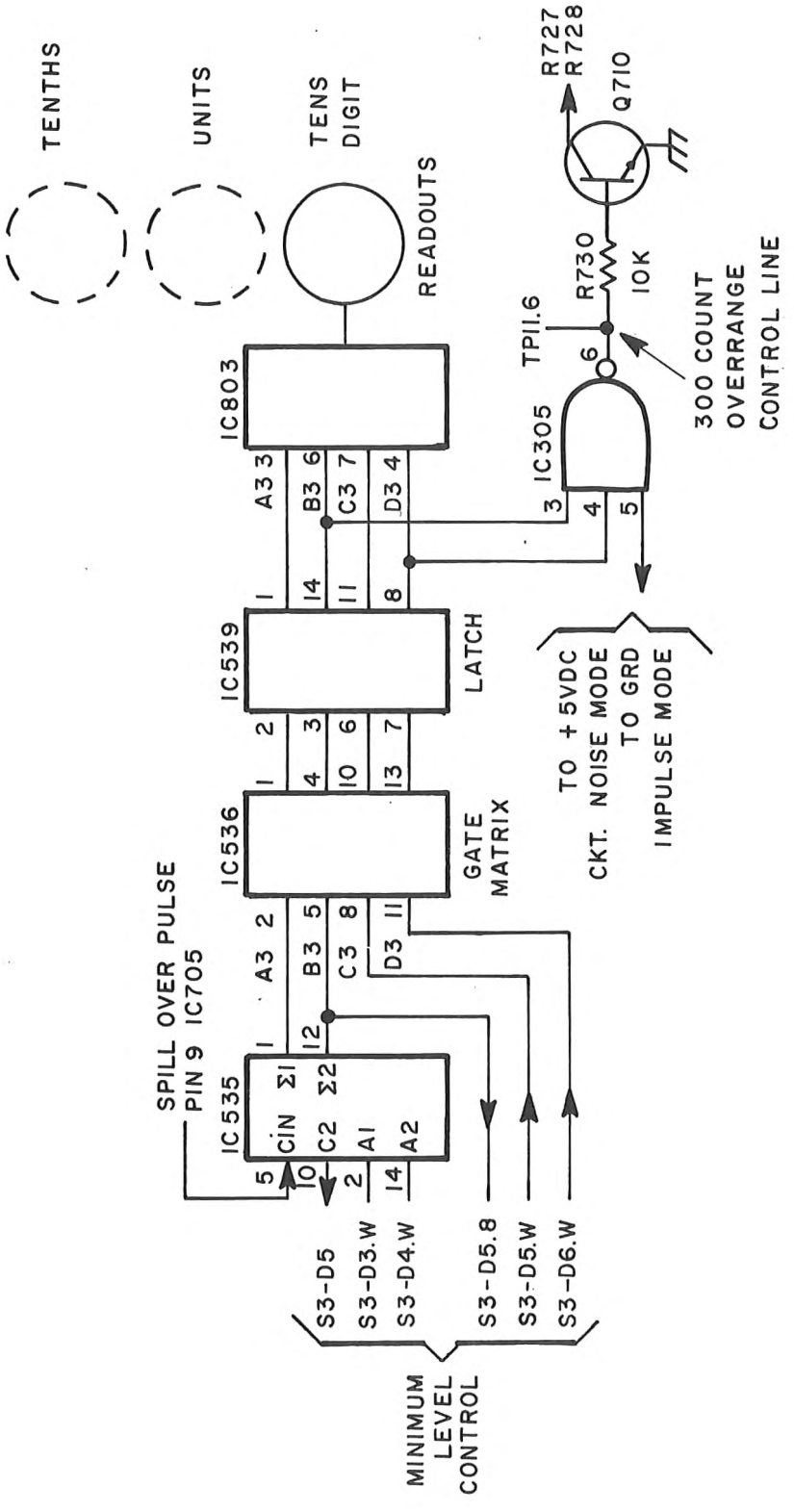

Figure 4-5 100dB Over Range Logic Schematic

updates the binary count appearing at the output of the latch IC539 to 10. This new binary information is applied to the 3 input NAND gate IC305 and the output pin 6 is caused to go from high to low turning off transistor Q701 (See table below).

4.21 All overrange information appear on either the 300 count overrange control line or the 320 count overrange control line. An other condition exists where both the readout tubes and the over-range lamp DS-2 are extinguished. This occurs when the input signal is below the threshold setting of the MINIMUM LEVEL CONTROL S-3.

4.22 When this condition exist, the output of IC707 pin 10, saturates at +12 Vdc and turns on transistor Q707. The table below describes the state of the logic transistors for the indicated READOUT tubes and OVERRANGE lamp conditions corresponding to the various operating conditions.

4.23 When the SELECTOR control switch S-4 is in any of the IMPULSE channel positions, a ground is connected to the base of transistors Q703 and Q707 through diodes CR1 and CR2. The ground connected to the base of transistor causes the transistor switch, Q704 to remain closed and continues to hold a discharge condition on capacitor C706. The ground connected to the base of transistor Q707 guarantees that the readout tubes will remain illuminated when in the IMPULSE NOISE mode.

4.24 IMPULSE PEAK DETECTORS (See Fig. 7-6)

4.25 In each impulse peak detector configuration there is an input amplifier driving a d.c. biased diode bridge which holds a d.c. amplifier in an off condition. The input signal being measured in channel A, is ac coupled by capacitor C301 from the INCREMENT control S-5 (wiper of deck 5) to the non-inverting input, pin 5 of amplifier IC301.

4.26 Variable resistor R302, in series with resistors R301 and R303, form a voltage divider and provide a means for balancing the amplifier sensitivity to both signal polarities. The amplifier sensitivity is adjusted for approximately -40dB and is determined by the combination of the voltage divider R309 and resistor R315 in series with R316, and the ratio of resistors R306 and R304. Variable resistor R316 is used to adjust the channel A sensitivity.

4.27 The resistor voltage divider R307 and R309 biases the intergrated circuit amplifier IC302 in an OFF condition such that the output of the amplifier pin 10 is at approximately

CONDITIONS

READOUT TUBES	ILLUMINATED	EXTINGUISHED	EXTINGUISHED	
OVERRANGE LAMP	EXTINGUISHED	EXTINGUISHED	ILLUMINATED	
TRANSISTORS	OPERATION WITHIN DYNAMIC RANGE	OPERATION BELOW DYNAMIC RANGE	OVERRANGE 300 COUNT	320 COUNT
Q707	OFF	ON	OFF	ON
Q708	ON	OFF	OFF	OFF
Q709	OFF	OFF	ON	OFF
Q710	ON	ON	OFF	ON
Q711	OFF	OFF	ON	ON
Q712	OFF	ON	OFF	OFF

-12 Vdc. When the input peak signal is of sufficient amplitude, this bias condition is overcome and reverses the voltage between pin 4 and 5 of the amplifier IC302 causing the output pin 10 to switch from -12 Vdc to +12 Vdc. The width of the pulse generated at the output of IC302 is a function of the magnitude of the peak voltage of the signal being measured.

4.28 Resistors R313 and R314 form a voltage divider to limit the peak positive voltage appearing at the input of IC305, pin 1 to approximately 4 volts. The diode CR303 clamps the negative voltage at approximately -0.6 Vdc.

4.29 The operation of channels B, C, and D is the same as that described for channel A in the previous paragraph except that the sensitivity of the input amplifiers varies with the setting of the INCREMENT control switch, S-5. This sensitivity is varied by changing the ratio of the resistor values in the amplifier negative feedback loop. The INCREMENT switch, deck 4 controls the gain of channel B, deck 2 controls the gain of channel C, and deck 1 controls the gain of channel D. Deck 5 is a 3dB step attenuator with a total attenuation of 9dB common to all four impulses channels.

4.30 BLANKING INTERVAL AND GATING LOGIC (See Fig. 7-6)

4.31 Intergrated circuit IC308 and transistors Q305 and Q306 constitute the inhibit circuit and controls the blanking period immediately following an impulse "hit".

4.32 The inhibit circuit is common to all four channels but is activated by channel A only and occurs when the junction of resistors R313 and R314 goes from low to high. This positive voltage is connected to pin 4 of IC308 through R318 and causes pin 2 of IC308 to go from low to high, thus placing a positive charge on the timming capacitor connected to pin 2. This marks the begining of one blanking interval. The capacitor discharges through the resistor series combination, R1, R319 and R320 connected to the base of transistor Q306. The base current holds transistor Q306 saturated and effectively keeps the input, pin 4 of IC308 at near ground potential during the discharge period. In addition, the capacitor is connected to pin 5 of IC308 and holds the circuit in the ON condition until the capacitor has discharged sufficiently to release it. This marks the end of one blanking interval.

4.33 If the period of the impulse "hit" exceeds the period of the blanking interval, the inhibit circuit will recycle. The BLANKING INTERVAL RANGE switch S-7 selects the timming capacitor and the BLANKING INTERVAL VERNIER potentiometer, R1 varies the discharge time.

4.34 Normally, pins 2 and 13 of the NAND gate IC305 are both at a logical 1. Pin 1 is connected to the junction of resistors R313 and R314 and is at ground potential until an impulse "hit" causes this point to go to a logical 1. The output pin 12 of IC305 goes from high to low and clocks the input, pin 1 of flip-flop IC307. The $\overline{Q}$ pin 5 of IC307 goes from high to low applying a ground to pin 13 of IC305 effectively "closing" the gate. The flip-flop continues to hold the gate closed until it is "cleared" by a pulse originating from the blanking interval inhibit circuit. Channels B, C and D operate in the same manner.

4.35 At the end of the blanking interval period, the negative high to low transition from pin 2 of IC308 is differentiated by two seperate circuits. The differentiated pulse applied to transistor Q301 causes a "clear"

pulse to be generated and appears at the collector of transistor Q302. The collector of Q302 is connected to the four flip-flops, pins 3 and 13 of IC306 and IC307 and the "clear" pulse resets the $\overline{Q}$ outputs pins 5 and 10 to a logical 1.

4.36 The second differentiated pulse applied to the base of Q303 causes a second pulse to be generated and appears at the collector of Q304. This collector of Q304 is connected to the four gates, pin 2 of IC305 and pins 2, 5 and 10 of IC304. This pulse holds the gates closed during that period when the flip-flop is reset by the "clear" pulse.

4.37 CHANNEL COUNTERS-GATE MATRIX & READOUT SECTION (See Fig 7-8)

4.38 The high to low transistions appearing at the $\overline{Q}$ outputs of the dual flip-flops IC306 and IC307 are applied to the inputs pin 11, of each respective decade counters, and the binary information for each channel is applied to the gate matrix.

4.39 Decade counters IC501 through IC504 and gates IC505 through IC508 are associated with channel A. Decade counters IC509 through IC512 and gates IC513 through IC516 are associated with channel B. IC517 through IC520 and IC521 through IC524 associated with channel C and decade counters IC525 through IC528 and gates IC529 through IC532 are associated with channel D.

4.40 All binary information accumulated is retained until manually reset to zero by the RESET control S-11. The SELECTOR switch S-4 places a ground on all the gates in the gate matrix except those gates associated with the channel selected and allows only that binary information to appear at the input of the latches IC537 through IC540.

4.41 When in the IMPULSE mode, the transfer latches are held at a logical 1 via switches S-4 (deck 2A, deck 2B) and switch S-10 when in the DISPLAY CONTINUOUS POSITION. When S-10 is in the HOLD DISPLAY position the transfer line is grounded.

4.42 The binary information present at the output of the latches is applied to the decoder drivers IC801 through IC804. The decoder drivers convert the binary information to digital information and is displayed by the digital readout tubes V 801 through V 804.

4.43 TIMER AND RESET LOGIC (See Fig 7-9)

4.44 When in the IMPULSE mode, the reset pulse to the decade counters associated with the four impulse channels is generated by a one-shot multivibrator. Two NOR gates in IC1001 are used for the multivibrator A single pulse is generated when +5 volts is applied to C1003 via S-11 when activated. This pulse is applied to the base of the buffer transistor stage Q1001 via resistor R1006. With the RESET switch in the OFF position, a continuous ground is applied to the base of transistor Q1001. This turns off transistor Q1001 and allows the collector to be at +5 volts. The collector is connected to pins 2 and 3 of all the decade counters associated with the impulse channels and holds them in a reset condition until S-11 is released.

4.45 The other two gates in IC1001 are used as a switch circuit providing logic inversion and transient suppression. The output pin 2 is at a positive voltage when the timer is in the off position. This positive voltage at pin 2 is connected to the base of Q304 and holds this transistor on. The collector is then near ground potential and holds the channel gates

IC304 and IC305 closed until the timer is set. When the timer contacts are closed, the output, pin 2 goes to ground and allows the collector of the transistor Q304 to go to a logical 1 allowing the gates IC304 and IC305 to transfer information. At the end of a timming period determined by the timer the gates are again closed.

4.46 POWER SUPPLY (See Fig 7-10)

4.47 The power transformer T1, will operate from 115 Vac or 230 Vac, 50Hz-400Hz. The switch S-2 selects the desired operating voltage. The +190 Vdc is derived from a full wave bridge rectifier circuit., CR608, and the RC pi-filter network, resistor R605 and capacitor C607 and C608. The bridge rectifier package CR607 provide both unregulated voltages for the +12 V buss and the -12 V buss.

4.48 The +12 Vdc is derived from a voltage regulator circuit utilizing a temperature compensated zener diode CR606, as a voltage reference. The intergrated circuit IC602 is a d.c. amplifier and drives the series pass transistor Q605. The negative feedback is taken from the voltage divider network, resistors R613, R614 and R615. The potentiometer, R614 is used as an adjustment for setting the d.c. voltage to +12 volts. Resistor R601 and capacitor C602 and C603 provide the filtering for the unregulated positive voltage.

4.49 The -12 Vdc is derived from a similar regulator circuit using the +12 Vdc as a voltage reference. The intergrated circuit IC601 is a d.c. amplifier driving the series pass trasnsitor Q606. The negative feedback is taken from the voltage divider resistors R610, R611 and R612. The potentiometer R611 is used as a means for adjusting the d.c. voltage to -12 volts. The voltage at pin 4 of IC601 is zero volts to ground only when the dc voltage at the opposite ends of the voltage divider, R610, R611 and R612 are equal and opposite.

4.50 The unregulated voltage for the +5 V buss is derived from a full wave recitfier circuit, CR601 and CR602 Filtering is provided by capacitor C1. The series pass transistor Q and transistor Q602 form a Darlington circuit. Negative feedback is taken from the voltage divider resistors R606, R607, R608 and diodes CR603 and CR604. This divider is referenced to the -12 volt buss and potentiometer R606 is used to adjust the dc voltage to +5 volts. The transistor Q601 in the negative feedback path regulates the dc voltage on the base of Q602.

4.51 Transistor Q603 and SCR Q604 provide over-voltage protection.

SECTION 5

MAINTENANCE AND CALIBRATION

5.1 MAINTENANCE. The schematics, block diagram and printed circuit board diagrams identify circuit components. Waveforms and voltages appear on the schematic diagrams. Signal flow diagrams associated with the circuit noise mode circuits appear in Section 4. Components are identified by letter symbols according to the following convention:

C	capacitor
CR	diode
E	printed circuit board
IC	integrated circuit
J	jack or connector
L	Inductor
Q	Transistor
R	resistor
RY	solenoid - relays
S	switch
T	transformer

5.2 MALFUNCTIONS. In the event of a malfunction ensure that:

a. The power cord is properly connected to available commercial power

b. All external line plugs are properly wired and inserted in the correct jacks.

c. All switches and controls are set in accordance with the OPERATION section of this **manual.**

d. The test being performed is within the specification limits of the instrument.

5.3 When it has been determined that a malfunction does exist, some attempt at interpreting the symptoms should be made prior to removing the set from the case. (See Table Below).

5.4 To remove the set from the case. proceed as follows:

a. Switch off power to the set and remove power cord.

b. Loosen four captive screws marked with arrow heads on front panel.

c. Carefully withdraw set from the case.

d. Reconnect power cord and switch on power when needed.

CAUTION:

Power line voltages of 115 Vac and / or 230 Vac in addition to +190 Vdc are present in this set and appear in various sections of the unit.

5.5 TEST EQUIPMENT REQUIRED.

EQUIPMENT	USE
NEC Model 2000, Triplett Model 680 NA or equivalent	To measure dc Volts.
NEC Model 2000, Triplett Model 630 NA, Hewlett-Packard Model 400 series or equivalent	To measure ac Volts. (High Level).
NEC Model 2000, TTS4C or Hewlett-Packard 400 series	To measure relative dB and/or low level ac Volts,
Tektronix Oscilloscope Models 535, 541A or 561B or equivalent	To observe waveforms.
NEC TTS 4C or TTS 43A or equivalent.	Calibrated Signal Source.

5.6 CALIBRATION. The Model 58B has been calibrated at the factory before shipment. Re-calibration should only be performed if component parts are replaced because of a malfunction. Only the circuit directly involved with the component replacement need be re-calibrated.

5.7 CIRCUIT NOISE CHANNEL CALIBRATION CHECK.

a. Set-up Model 58B front panel controls as follows:

PUSHBUTTONS	600 ohms
	TERM
	BAL-XFMR
NETWORK	C-MSG
SELECTOR	CIRCUIT NOISE
MINIMUM LEVEL	70 dBrn
POWER	ON

b. Connect a 1kHz signal with a level of -10 dBm from a 600 ohm source to the line input of the Model 58B. The Model 58B should display 80 dBrn $\pm$0.3 dB.

5.8 CIRCUIT NOISE CHANNEL CALIBRATION: GENERAL.

If it is found necessary to recalibrate, first determine in what section the error exists.

a. With conditions outlined in par. 5.7 (a) decrease input level to -20 dBm.

b. Refer to block diagram and use indicated levels for reference.

c. If the error is found to exist at the input of the 47 dB amplifier, IC901, then the problem is common to all channels. This would indicate that the amplifier gain control R219 associated with the buffer amplifier or the amplifier gain control R210 associated with the C-MSG Amplifier are out of adjustment.

d. Switch to FLAT NETWORK. If error still exists, adjust R219. If error no longer exists, R210 needs adjustment.

e. If error is found to exist at the output of the 47 dBAmplifier, IC901, this would indicate that the Amplifier Gain Control R905 needs adjustment.

f. If the level at the output of amplifier IC901 is correct measure the dc voltage at the output of the AC-DC converter. This should be -1.5 Volts +0, -5%. Adjust dc gain control R929 associated with the dc amplifier IC902 if this voltage is incorrect.

5.9 DC-LOG CONVERTER CALIBRATION.

a. Set-up Model 58B front panel controls as in paragraph 5.7 (a)

b. Connect a 1kHz signal from a 600 ohm source to the line input of the Model 58B.

c. Adjust input level to read exactly 70 dBrn on Model 58B.

d. Increase input level by 12 dB in 1 dB steps and note tracking accuracy. Error, if any, should remain within $\pm$0.1 dB.

5.10 If tracking deviates from that specified in par. 5.9 proceed as follows:

a. IMPORTANT: Power must be off and sufficient time allowed to assure that the +190 volt dc buss has deteriated before proceeding.

b. Locate printed circuit board 7, E95500. Remove it from the card cage and place on extender card.

c. Re-apply power to Model 58B, and with conditions as in par. 5.9 (c) measure the dc voltage at TP 7.5.

NOTE

This voltage must be measured with a high input impedance dc voltmeter. Use NEC Model 2000 or equivilent. This voltage should be between +1.45 V and +1.5 Vdc. If not adjust R706.

ERRATA

Paragraph 5.11 (b) should read:

b. Connect a 1kHz signal with a level of -53 dBm from a 600 ohm source to the line input of the Model 58B.

d. Readjust input signal level to read exactly 70 dBrn and then increase input level by exactly 10 dB. If necessary, adjust 10 dB cal. control R715 to read 80 dBrn ±0.1 dB.

e. Decrease input level by 5 dB. If necessary, adjust SLOPE control R713 to read 75 dBrn ±0.1 dB.

f. Repeat steps (d) and (e) for desired accuracy.

5.11 IMPULSE CHANNEL CALIBRATION CHECK.

a. Set up Model 58B front panel controls as follows:

PUSHBUTTONS	600 ohms
	TERM
	BAL-XFMR
NETWORK	C-MSG
SELECTOR	Impulse channel being checked
MINIMUM LEVEL	40dBrn
INCREMENT	0-2-4-6 dBrn
TIMER	Continuous position
BLANKING	Set for 10PPS

b. Connect a 1kHz signal with a level of -53 dBm from a 600 ohm source to the line input of the Model 58B.

c. Set SELECTOR to channel A and adjust input signal level for visual periodic count accumulation at threshold. Resulting input signal level should be within ±0.5 dB of -53 dBm.

d. Check channels B, C, and D in the same manner with input signal levels of -51 dBm, -49 dBm and -47 dBm respectively. All should be within ±0.5 dB accuracy.

5.12 If one or more channels need to be recalibrated, proceed as follows:

a. If channel A needs to be recalibrated, remove printed circuit board 3, E95501, from card cage and place on card extender. Use short clip leads to establish connection between disconnected cable and printed circuit board input terminals.

CAUTION

The case of series pass transistor Q1 is at +9 Vdc any mometary short will open 3A fuse F-2.

b. With power reapplied to the Model 58B and same conditions existing as in par. 5.11 (b) and (c), place SELECTOR switch to channel A and adjust SENS. CAL. control R316 for visual periodic count accumulation.

c. Decrease input level by 0.2 dB. Count accumulation should stop. Increase input level by 0.4 dB and a full count rate of 10 PPS should be observed.

5.13 If the amplifier intergrated circuit IC301 has been replaced, the BALANCE control R302 may require re-adjustment to insure equal channel sensitivity to both polarities of the input signal, proceed as follows:

a. Connect oscilloscope to TP 3.3 located on printed circuit board 3. Adjust oscilloscope for positive internal triggering with horizontal time base set for 0.1 ms/cm.

b. Increase input signal level to -52 dBm and adjust oscilloscope for correct horizontal triggering.

c. Observe waveform and adjust BALANCE control R302 for a recurring rectangular pulse every 0.5ms. This is an indication that the channel A detector is triggering on both polarities of the input signal.

d. Decrease input level to -53 dBm and adjust SENS CAL. control R316 for visual periodic count accumulation.

e. At this threshold level, only one will be observed. Increasing input level by 0.2 or 0.3 dB should result in a pulse every 0.5 ms. Correct adjustment of the BALANCE control is indicated when triggering of both polarities of the input signal occurs within 0.5 dB of threshold.

5.14 Impulse channels B, C, and D are similar in operation to channel A. Use the same calibration instructions outlined for channel A observing the correct threshold levels relative to each channel.

5.15 TO CHECK WEIGHTING NETWORK LEVEL EQUALIZATION.

a. Set-up Model 58B front panel controls as follows:

PUSHBUTTONS	600 ohms
	TERM
	BAL.-XFMR
NETWORK	10.2-51kHz
SELECTOR	CIRCUIT NOISE
MINIMUM LEVEL	70dBrn
POWER	ON

b. Connect a 25kHz signal with a level of -10 dBm from a 600 ohm source to the line input of the Model 58B. The Model 58B should read 80dBrn $\pm$0.3 dBm.

c. Change input signal frequency to 1kHz at a signal level of -10 dBm.

d. Switch NETWORK control to both C-MSG and FLAT. Set should read same level $\pm$0.1 dB as that indicated when in the 10.2-51kHz NETWORK.

5.16 If re-calibration is found to be necessary proceed as follows:

a. Locate printed circuit board 2, E95510 and remove from card cage. Place on extender card.

b. With conditions outlined in par. 5.15 (a) and (b), recalibrate by adjusting R210 for C-MSG weighting level correction and/or R216 for FLAT weighting level correction.

5.17 Input balance controls, C104, C105, C106 R121 and R122 are factory adjustments. Replacement of the input amplifier IC101 may require re-adjustment of these controls. It is recommended that the input module section or entire set be returned to the factory if the Common Mode Rejection is believed to have deteriated.

1. PC 5 E95502
2. T2
3. TB1
4. HOLD COIL
5. PC 2 E95510
6. PC 1 E-14-058-20-032
7. C2
8. JACK BLOCK
9. PC 11 E95504
10. PC 7 E95500
11. PC 9 E95464
12. PC 3 E95501
13. PC 4 E95499
14. S4
15. S 5
16. J28
17. PC 8 E95496
18. S7
19. S10
20. S 8
21. S11
22. S12
23. C1
24. F2
25. Q1
26. PC 10 E95498
27. F1
28. PC 12 E95284
29. PC 6 E95480
30. HANDLE
31. PC 1A E-14-058-20-038

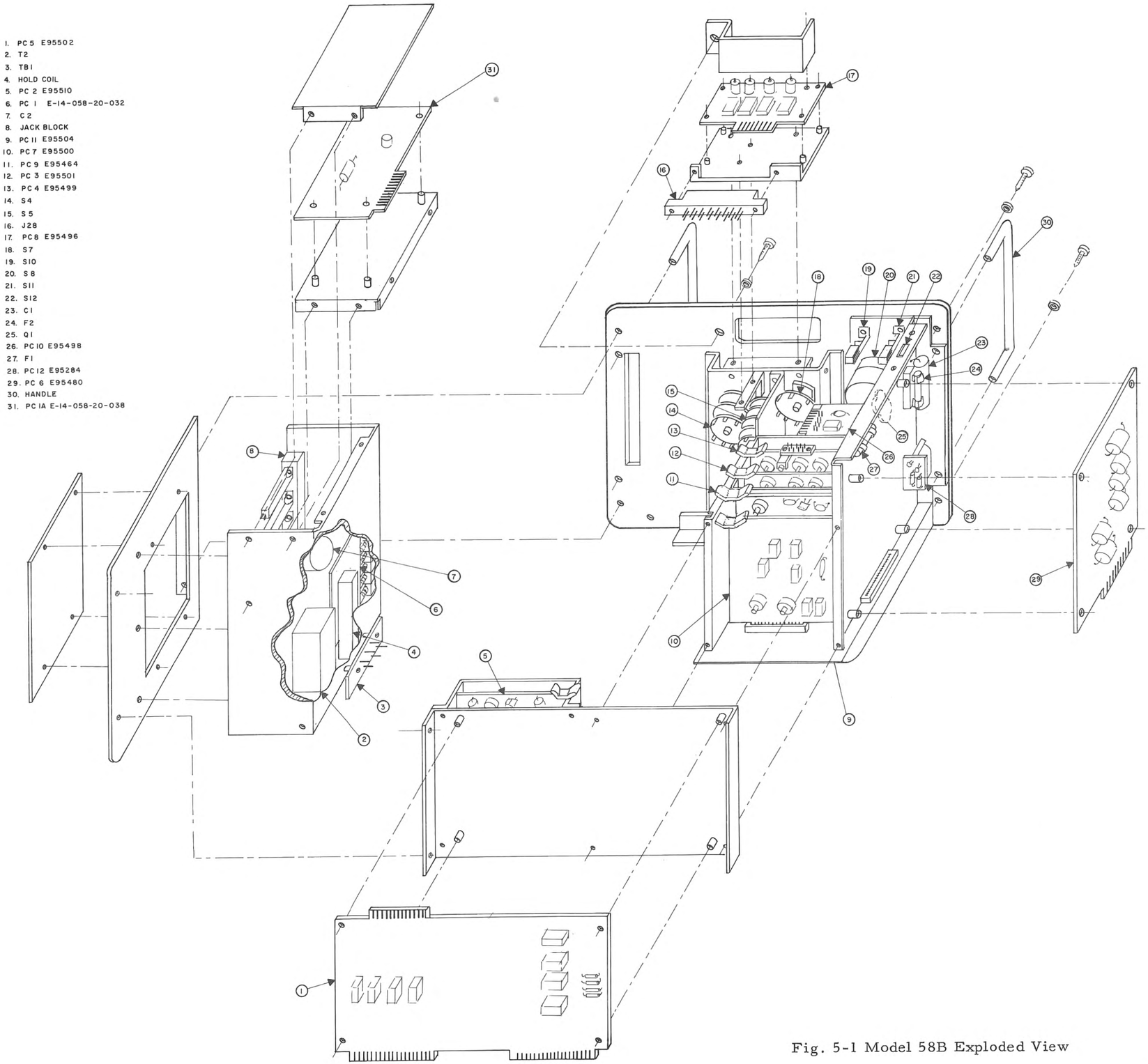

Fig. 5-1 Model 58B Exploded View

SECTION 6

ELECTRONIC PARTS LIST

6.1 INTRODUCTION. The following pages contain the parts list for the Model 58B Impulse counter and Noise Measuring Set.

6.2 FSCM Code Numbers. This is the Federal Supply Code of Manufacturers as issued October 1969. A list of codes and their respective manufacturers is given on page 6-2.

LIST OF MANUFACTURERS

Code No.	MANUFACTURER
01121	Allen-Bradley, Milwaukee, Wis. 53204
01295	Texas Instruments Inc. Semiconductor Div., Dallas, Texas 75231
05397	Union Carbide Corp., N.Y., N. Y. 10017
05844	Callins Industries Inc., Greenfield, Tenn. 38230
06107	National Electronics Calif., Hollywood, Calif. 90024
06486	IRC Division of TRW, Lynn, Mass. 01905
06819	Northeast Electronics Corp., Concord, N.H. 03301
07716	IRC Division of TRW Inc., Burlington, Iwoa 52601
09353	C&K Components Inc. Newton, Mass. 02158
12065	Transitron Electronics Corp., Boston, Mass. 02128
12954	Dickson Electronics Corp., Scottsdale, Ariz. 85252
13606	Sprague Electric Co. Transistor Div., Concord, N.H. 03301
15873	Motorola Inc., Arcade, N.J. 14009
16352	Computer Diode Corp., So. Fairlawn, N.J. 07410
17117	Electronic Moulding Corp., Pawtucket, RI. 02860
17538	Precision Electronics, Mansfield, Mass. 02050
18324	Signetics Corp., Sunnyvale, Calif. 94086
24655	General Radio, Concord, Mass. 01781
44655	Ohmite Mfg. Co., Skokie, Ill. 60076
49671	RCA Corp., N.Y., N. Y. 10020
71450	CTS Corp., Elkhart, Ind. 46514
71590	Centralab, Milwaukee, Wis. 53201
72765	Drake Manufacturing, Harwood, Heights, Ill. 60656
72982	Erie Technological Products, Erie, Pa. 16512
75915	Littelfuse Inc., Des Planes, Ill. 60016
76493	Miller JW Company, Compton, Calif. 90024
79919	Rhodes MH Inc., Hartford, Conn. 06101
80368	Sylvania Electric Inc., N.Y., N. Y. 10017
81095	Triad Transformer Corp., Venice, Calif. 90293
81483	International Rectifier Corp., Segundo, Calif. 90245
82389	Switchcraft Inc., Chicago, Ill. 60630
83330	Smith Herman H. Inc., Brooklyn, N. Y. 11207
83612	Kidde Mfg. Co., Bloomfield, N.J.
86632	Newton Engineering, Newton, Mass. 02161
99800	Delvan Electronics Corp., Auroa, N. Y. 14052

PC Bd. E14-058-20-032

Input Circuit & Impedance

Ref Desig.	Description	Manufacturer (FSCM Code #))	Part Number
R101 and R102	R: 110Ω ½W 5%	01121	EB
R103	R: 499Ω 1/8W 1%	07716	CEATO
R104	R: 39.2K 1/8W 1%	07716	CEATO
R105	R: 20.5K 1/8W 1%	07716	CEATO
R106	R: 487Ω ½W 1%	07716	CECTO
R107	R: 316Ω ½W 1%	07716	CECTO
R108	R: 75Ω ½W 1%	07716	CECTO
R109	R: 68.1Ω ½W 1%	07716	CECTO
R110	R: 20.5K 1/8W 1%	07716	CEATO
R111	R: 487Ω ½W 1%	07716	CECTO
R112	R: 316Ω ½W 1%	07716	CECTO
R113	R: 75Ω ½W 1%	07716	CECTO
R114	R: 68.1Ω ½W 1%	07716	CECTO
C102	C: 22μF 150V 10%	13606	109D226X9150T2
C103	C: 22μF 150V 10%	13606	109D226X9150T2

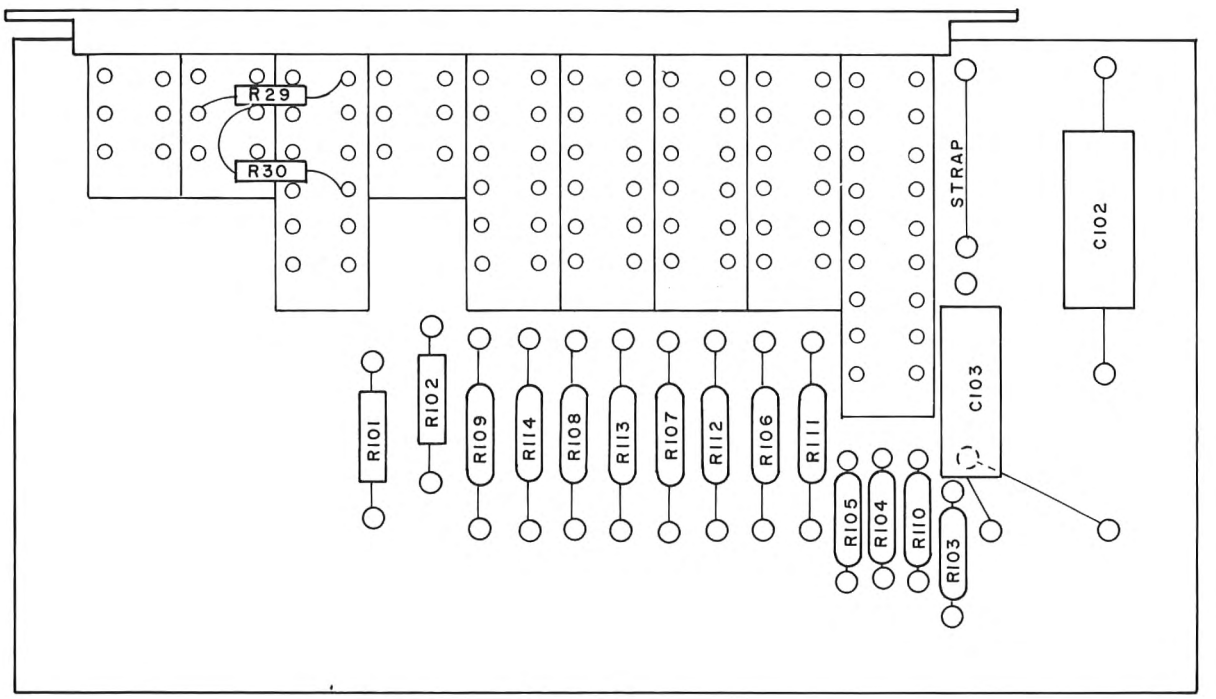

Fig. 6-1 Component location E14-058-20-032

PC Bd. E14-058-20-038

Input Amplifier

Ref Desig.	Description	Manufacturer (FSCM Code #)	Part Number
R115	R: 12.4K 1/8W 1%	07716	CEAT9
R116	R: 12.4K 1/8W 1%	07716	CEAT9
R117	R: 124K 1/8W 1%	07716	CEAT9
R118	R: 4059Ω 1/8W 1%	07716	CEAT9
R119	R: 3784Ω 1/8W 1%	07716	CEAT9
R120	R: 200Ω 1/8W 1%	07716	CEAT9
R121	Pot: 200Ω	71450	UPE200RE-1
R122	Pot: 2K	71450	UPE-200RE-1
R123	R: 2K 1/8W 1%	07716	CEAT9
R124	R: 121K 1/8W 1%	07716	CEAT9
R125	R: 680Ω $\frac{1}{4}$W 10%	01121	CB
R126	R: 1500Ω $\frac{1}{4}$W 10%	01121	CB
R127	R: 1 Meg $\frac{1}{4}$W 10%	01121	CB
R128	R: 1800Ω $\frac{1}{4}$W 10%	01121	CB
R129	R: 600Ω 1/8W 1%	07716	CEATO
R130	R: 630.9Ω 1/8W 1%	07716	CEATO
R131	R: 1262Ω 1/8W 1%	07716	CEATO
R132	R: 1540Ω 1/8W 1%	07716	CEATO
R133	R: 12.25K 1/8W 1%	07716	CEATO
R134	R: 1150Ω 1/8W 1%	07716	CEATO
R135	R: 976Ω 1/8W 1%	07716	CEATO
R136	R: 27Ω 1/4W 10%	01121	CB
R137	R: 27Ω 1/4W 10%	01121	CB
C101	C: 1μF 25V	13606	5C13
C104	C: 1.5-8pf NPO variable	72982	539-002COPO98R
C105 and C106	C: 1.5-8pf NPO variable	72982	539-002COPO98R
C107	C: 680pf 1kV 10%	71590	DD-681
C108	C: 0.001μF 1kV 10%	71590	DD 102
C109	C: 22pf 1kV 10%	71590	DD-220
C110	C: 22μF 6V 10%	05397	K22W6K
C111 and C112	C: 0.47μF 25V	13606	5C11
C113 and C114	C: 50μF 15V	13606	TE1160
C115	C: 1.0μF 25V	13606	5C13
C116	C: 3.9pf NPO	13606	10TCCV39
CR101, CR102	Diodes Silicon	12065	1N4148
Q101	FET Transistor	15873	MPF103
Q102	Transistor: NPN	15873	2N3903
IC101	Integrated circuit	01295	SN72709
RY101-105	Relays: reed	83612	24MC1C

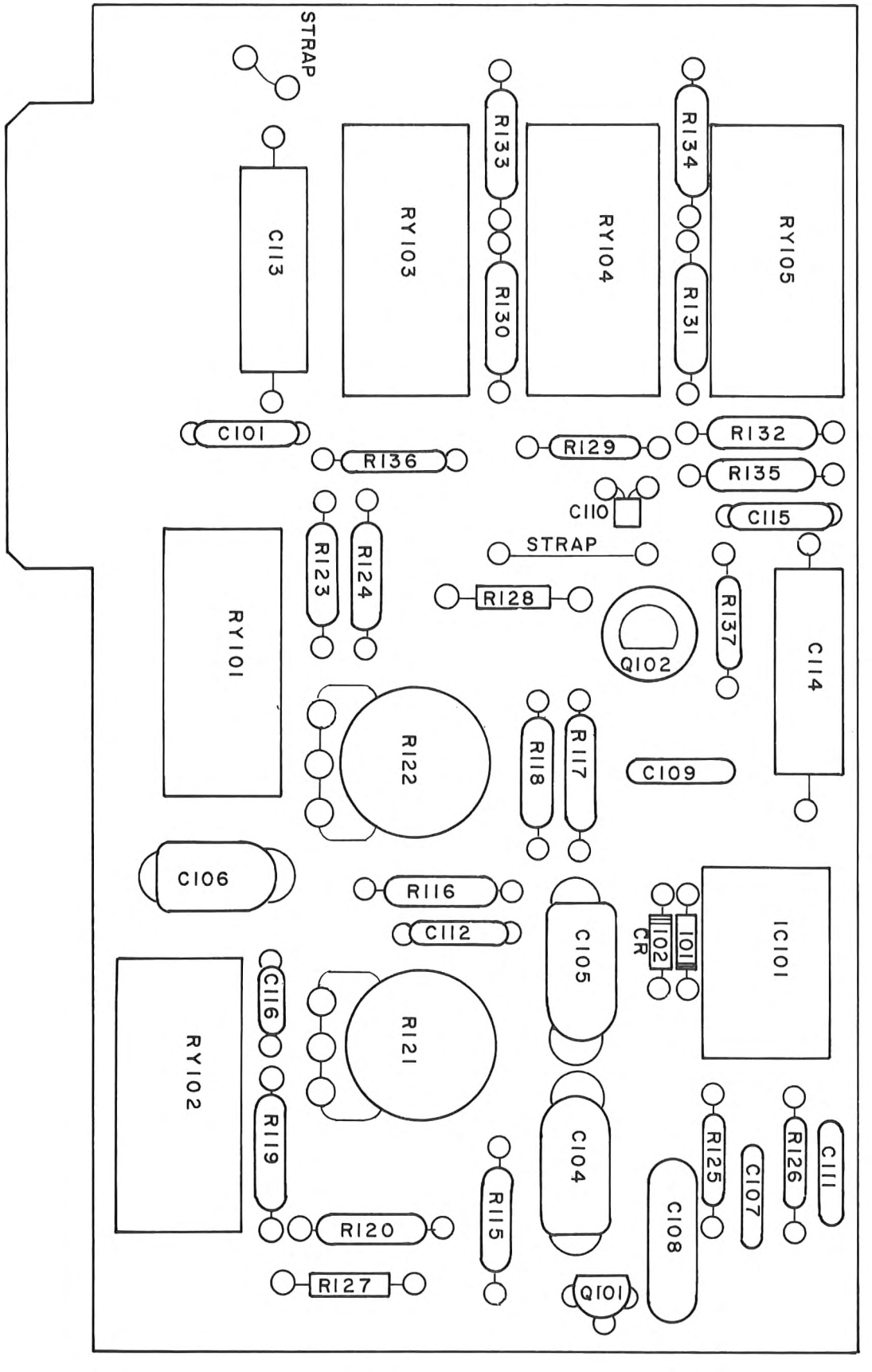

Fig. 6-2 Component location E14-058-20-038

PC Bd. E95510
WTG and Buffer Amplifier

Ref Desig.	Description	Manufacturer (FSCM Code #)	Part Number
C201	C: 0.2μF 75V 10%	13606	225P
C202	C: 1.0μF 35V 10%	05397	K2W35K
C203	C: 0.2μF 75V 10%	13606	225P
C204	C: 0.15μF 75V 10%	13606	225P
C205	C: 0.25μF 75V 10%	13606	225P
C206	C: 0.2μF 75V 10%	13606	225P
C207	C: 2.2μF 35V 10%	05397	K2R2W35K
C208 thru 211	C: 22μF 5V 10%	05397	K22W6K
C212, 213	C: 0.03μF 100V	13606	225PW
C214, 215	C: 0.006μF 100V	13606	225PW
C216	C: 22μF 6V 10%	05397	K22W6K
C217	C: 0.039μF 100V	13606	225PW
C218, 219	C: 1.0μF 25V	13606	5C13
C220	C: 510pf 1Kv 10%	71590	DD-511
C221	C: 22pf 1Kv 10%	71590	DD-220
C222	C: 22μF 6V 10%	05397	K22W6K
C223	C: 100μF 15V	13606	TE 1162
C224	C: 0.47μF 25V	13606	5C11
C225	C: 300μF 3V	05844	APD-081
C226	C: 0.47μF 25V	13606	5C11
C227, 228	C: 100μF 15V	13606	TE 1162
Q201, 203	Transistors: NPN	15873	2N3903
Q202	Transistor: PNP	15873	2N3905
IC201	Integrated circuit	01295	SN72709
L201	Inductor toroid 150 MH	81095	EA 150
L202, 203	Inductor toroid 30 MH	81095	EA 030
L204	Inductor 7500 MH	99800	2500-70
L205	Inductor 2700 MH	99800	2500-48
CR201-206	Diodes silicon	12065	1N4148
R201	R: 681Ω 1/8W 1%	07716	CEATO
R202	R: 619Ω 1/8W 1%	07716	CEATO
R203	R: 85Ω 1/8W 1%	07716	CEATO
R204	R: 1800Ω 1/8W 1%	07716	CEATO
R205	R: 183.7Ω 1/8W 1%	07716	CEATO
R206	R: 619Ω 1/8W 1%	07716	CEATO
R207	R: 22K $\frac{1}{4}$W 10%	01121	CB
R208	R: 330K $\frac{1}{4}$W 10%	01121	CB
R209	R: 12K $\frac{1}{4}$W 10%	01121	CB
R210	Pot: 500Ω	71450	UPE200RE-1
R211	R: 330Ω $\frac{1}{4}$W 10%	01121	CB
R212	R: 470Ω $\frac{1}{4}$W 10%	01121	CB
R213	R: 680Ω $\frac{1}{4}$W 10%	01121	CB
R214	R: 820Ω $\frac{1}{4}$W 10%	01121	CB
R215	R: 1180Ω 1/8W 1%	07716	CEATO
R216	Pot: 20K	71450	UPE200RE-1
R217	R: 100Ω $\frac{1}{4}$W 10%	01121	CB
R218	R: 2.49K 1/8W 1%	07716	CEATO
R219	Pot: 5K	71450	UPE 200RE-1
R220	R: 4.02K 1/8W 1%	07716	CEATO
R221	R: 1500Ω $\frac{1}{4}$W 10%	01121	CB
R222	R: 3.9K $\frac{1}{4}$W 10%	01121	CB
R223	R: 56Ω $\frac{1}{4}$W 10%	01121	CB
R224	R: 100Ω $\frac{1}{4}$W 10%	01121	CB
R225	R: 33K $\frac{1}{4}$W 10%	01121	CB

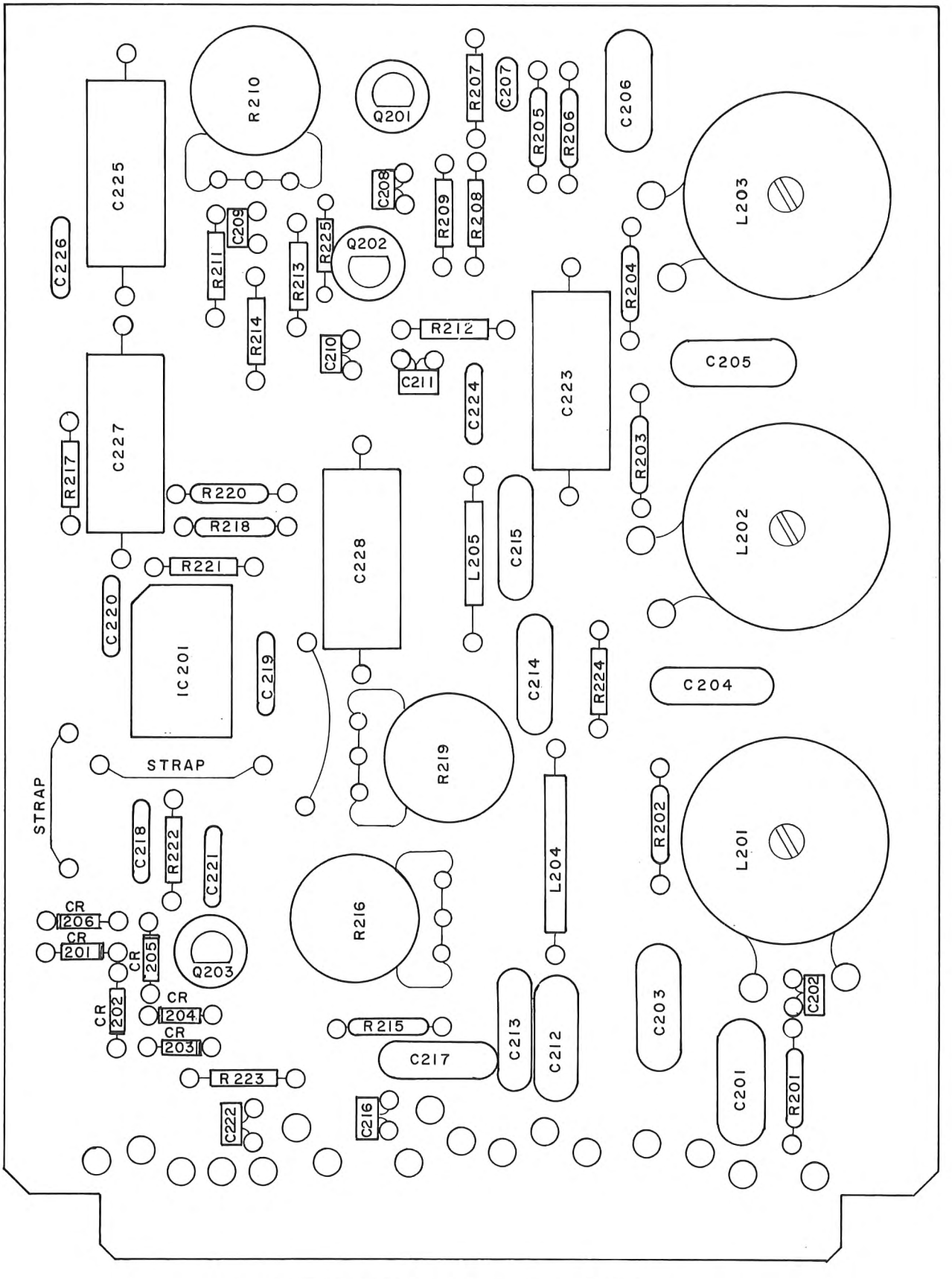

Fig. 6-3 Component location E95510

PC Bd. E95501
Channel A & Inhibit Circuit

Ref Desig.	Description	Manufacturer (FSCM Code #)	Part Number
R301, 303	R: 10K ½W 10%	01121	EB
R302	R: 10K pot	71450	UPE200RE-1
R304	R: 1300Ω 1/8W 1%	07716	CEATO
R305	R: 1500Ω ½W 10%	01121	EB
R306	R: 40.2K 1/8W 1%	07716	CEATO
R307, 308	R: 22K ½W 10%	01121	EB
R309	R: 3900Ω ½W 5%	01121	EB
R310, 311	R: 1K ½W 10%	01121	EB
R312	R: 560K ½W 10%	01121	EB
R313	R: 3600Ω ½W 5%	01121	EB
R314	R: 3900Ω ½W 5%	01121	EB
R315	R: 360Ω ½W 5%	01121	EB
R316	R: 1K pot	71450	UPE200RE-1
R317	R: 1K ½W 10%	01121	EB
R318	R: 3300Ω ½W 10%	01121	EB
R319	R: 100Ω ½W 10%	01121	EB
R320	Pot: 1K	71450	UPE200RE-1
R321	R: 510Ω ½W 5%	01121	EB
R322	R: 10K ½W 10%	01121	EB
R323	R: 91K ½W 5%	01121	EB
R324	R: 10K ½W 10%	01121	EB
R325	R: 91K ½W 5%	01121	EB
R326, 327	R: 10K ½W 10%	01121	EB
R328	R: 510Ω ½W 5%	01121	EB
R329	R: 100Ω ½W 10%	01121	EB
R330	R: 1 Meg ½W 10%	01121	EB
R331	R: 10K ½W 10%	01121	EB
R332	R: 5.1K ½W 5%	01121	EB
C301	C: 1μF 25V	13606	5C13
C302	C: 0.47μF 25V	13606	5C11
C303	C: 100pf 1Kv 10%	71950	DD 101
C304	C: 3.3pf 1Kv ±0.5pF	71590	DD 3R3
C305	C: 0.47μF 25V	13606	5C11
C306	C: 5μF 15V	13606	TE 1152
C307	C: 330pf 1Kv 10%	71590	DD 331
C308, 309	C: 0.47μF 25V	13606	5C11
C310	C: 150pf 1Kv 10%	71590	DD 151
C311	C: 33pf 1Kv 10%	71590	DD 330
C312	C: 0.47μF 25V	13606	5C11
C313	C: 2.2μF 35V 10%	05397	K2R2W35K
C314	C: sel val	13606	225P
C315	C: 0.22μF 50V 10%	05397	KR22W50K
C316	C: sel val	13606	225P
C317	C: 22μF 6V 10%	05397	K22W6K
C318	C: sel val		
C319	C: 0.022μF 100V 10%	13606	225PW
C320	C: sel val		
C321	C: 22μF 6V 10%	05397	K22W6K
C322	C: 150pf 1Kv 10%	71590	DD 151

Ref Desig.	Description	Manufacturer (FSCM Code No.)	Part Number
Q301-306	Transistors: NPN	15873	2N3903
CR301-305	Diodes Silicon	12065	1N4148
CR306	Diode Germanium	12065	1N198
IC301-302	Integrated circuit	01295	SN72709
IC303	Integrated circuit	49671	CA3019
IC304,305	Integrated circuit	01295	SN7410N
IC306,307	Integrated circuit	18324	SP322B
IC308	Integrated circuit	18324	SP380A
J17 and J18	Pin Jack	83330	499

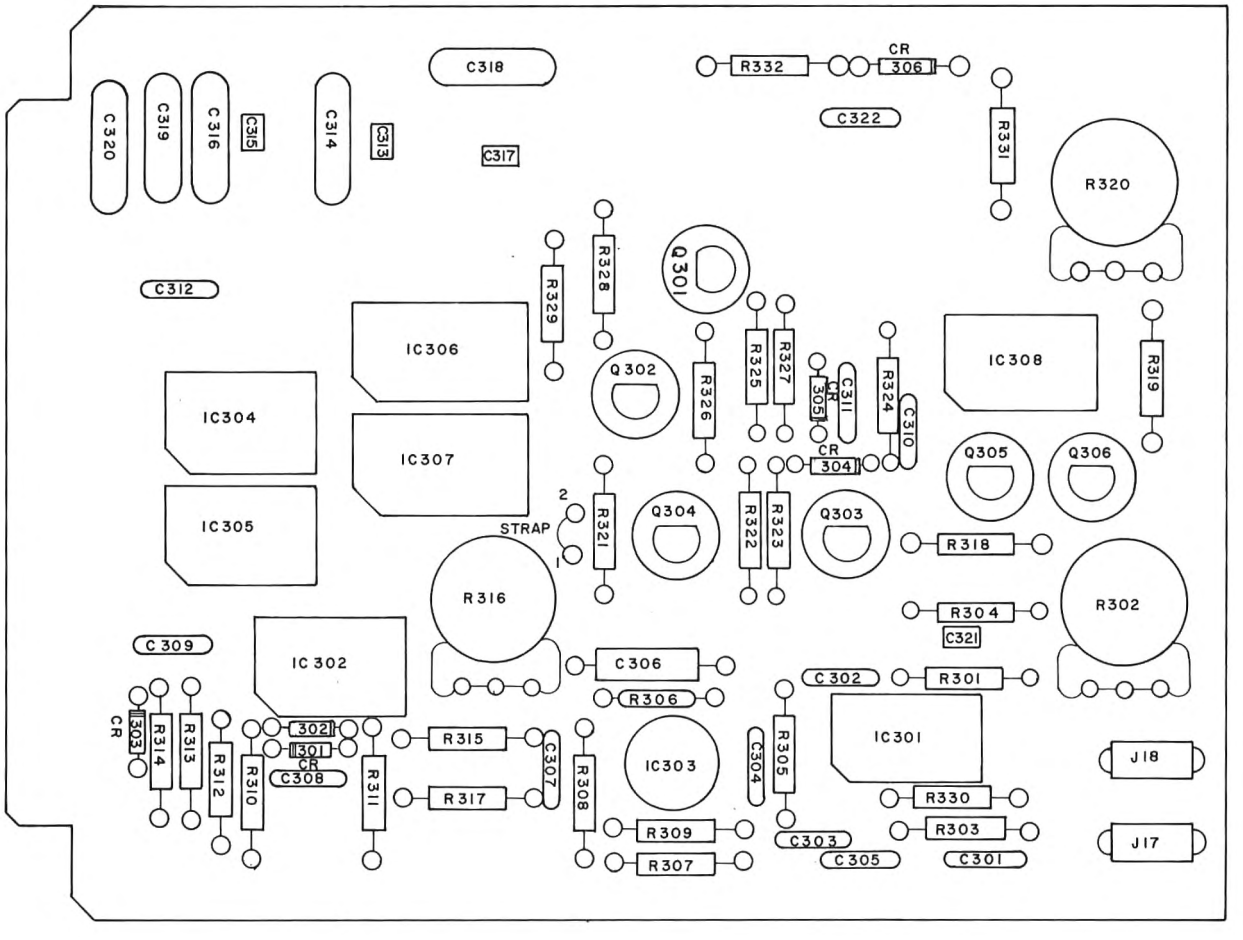

Fig. 6-4 Component location E95501

PC Bd. E95499

Channel A, B and C Level Detector Circuit

Ref Desig.	Description	Manufacturer (FSCM Code No.)	Part Number
R401	R: 10K ½W 10%	01121	EB
R402	Pot: 10K	71450	UPE200RE-1
R403	R: 10K ½W 10%	01121	EB
R404	R: 1500Ω ½W 10%	01121	EB
R405	R: 40.2K 1/8W 1%	07716	CEATO
R406, 407	R: 22K ½W 10%	01121	EB
R408	R: 3900Ω ½W 5%	01121	EB
R409, 410	R: 1K ½W 10%	01121	EB
R411	R: 560K ½W 10%	01121	EB
R412	R: 6800Ω ½W 5%	01121	EB
R413	R: 3900Ω ½W 5%	01121	EB
R414	R: 360Ω ½W 5%	01121	EB
R415	R: 1K pot	71450	UPE200RE-1
R416	R: 1K ½W 10%	01121	EB
R417	R: 10K ½W 10%	01121	EB
R418	R: 10K pot	71450	UPE200RE-1
R419	R: 10K ½W 10%	01121	EB
R420	R: 1500Ω ½W 10%	01121	EB
R421	R: 40.2K 1/8W 1%	07716	CEATO
R422, 423	R: 22K ½W 10%	01121	EB
R424	R: 3900Ω ½W 5%	01121	EB
R425, 426	R: 1K ½W 10%	01121	EB
R427	R: 560K ½W 10%	01121	EB
R428	R: 6800Ω ½W 5%	01121	EB
R429	R: 3900Ω ½W 5%	01121	EB
R430	R: 360Ω ½W 5%	01121	EB
R431	Pot: 1K	71450	UPE 200RE-1
R432	R: 1K ½W 10%	01121	EB
R433	R: 10K ½W 10%	01121	EB
R434	R: 10K pot	71450	UPE200RE-1
R435	R: 10K ½W 10%	01121	EB
R436	R: 1500Ω ½W 10%	01121	EB
R437	R: 40.2K 1/8W 1%	07716	CEATO
R438, 439	R: 22K ½W 10%	01121	EB
R440	R: 3900Ω ½W 5%	01121	EB
R441, 442	R: 1K ½W 10%	01121	EB
R443	R: 560K ½W 10%	01121	EB
R444	R: 6800Ω ½W 5%	01121	EB
R445	R: 3900Ω ½W 5%	01121	EB
R446	R: 360Ω ½W 5%	01121	EB
R447	Pot: 1K	71450	UPE200RE-1
R448	R: 1K ½W 10%	01121	EB
R449-451	R: 1 Meg ½W 10%	01121	EB
C401	C: 1μF 25V	13606	5C13
C402	C: 0.47μF 25V	13606	5C11
C403	C: 100pf 1Kv 10%	71590	DD 101
C404	C: 3.3pf 1Kv ±0.5pF	71590	DD 3R3
C405	C: 0.47μF 25V	13606	5C11
C406	C: 5μF 15V	13606	TE 1152
C407	C: 150pf 1Kv 10%	71590	DD 151

E95499 (cont.)

Ref Desig.	Description	Manufacturer (FSCM Code #)	Parts Number
C408, 409	C: 0.47μF 25V	13606	5C11
C410	C: 1μF 25V	13606	5C13
C411	C: 0.47 μF 25V	13606	5C11
C412	C: 100pf 1Kv 10%	71590	DD 101
C413	C: 3.3pf 1K ± 0.5pF	71590	DD 3R3
C414	C: 0.47μF 25V	13606	5C11
C415	C: 5μF 15V	13606	TE 1152
C416	C: 150pf 1Kv 10%	71590	DD 151
C417, 418	C: 0.47μF 25V	13606	5C11
C419	C: 1μF 25V	13606	5C13
C420	C: 0.47μF 25V	13606	5C11
C421	C: 100pf 1Kv 10%	71590	DD 101
C422	C: 3.3pf 1Kv ±0.5pF	71590	DD 3R3
C423	C: 0.47μF 25V	13606	5C11
C424	C: 5μF 15V	13606	TE 1152
C425	C: 150pf 1Kv 10%	71590	DD 151
C426, 427	C: 0.47μF 25V	13606	5C11
C428-430	C: 22μF 6V 10%	05397	K22W6K
CR401-409	Diodes Silicon	12065	1N4148
IC401-406	Integrated circuits	01295	SN72709
IC407-409	Integrated circuits	49671	CA3019

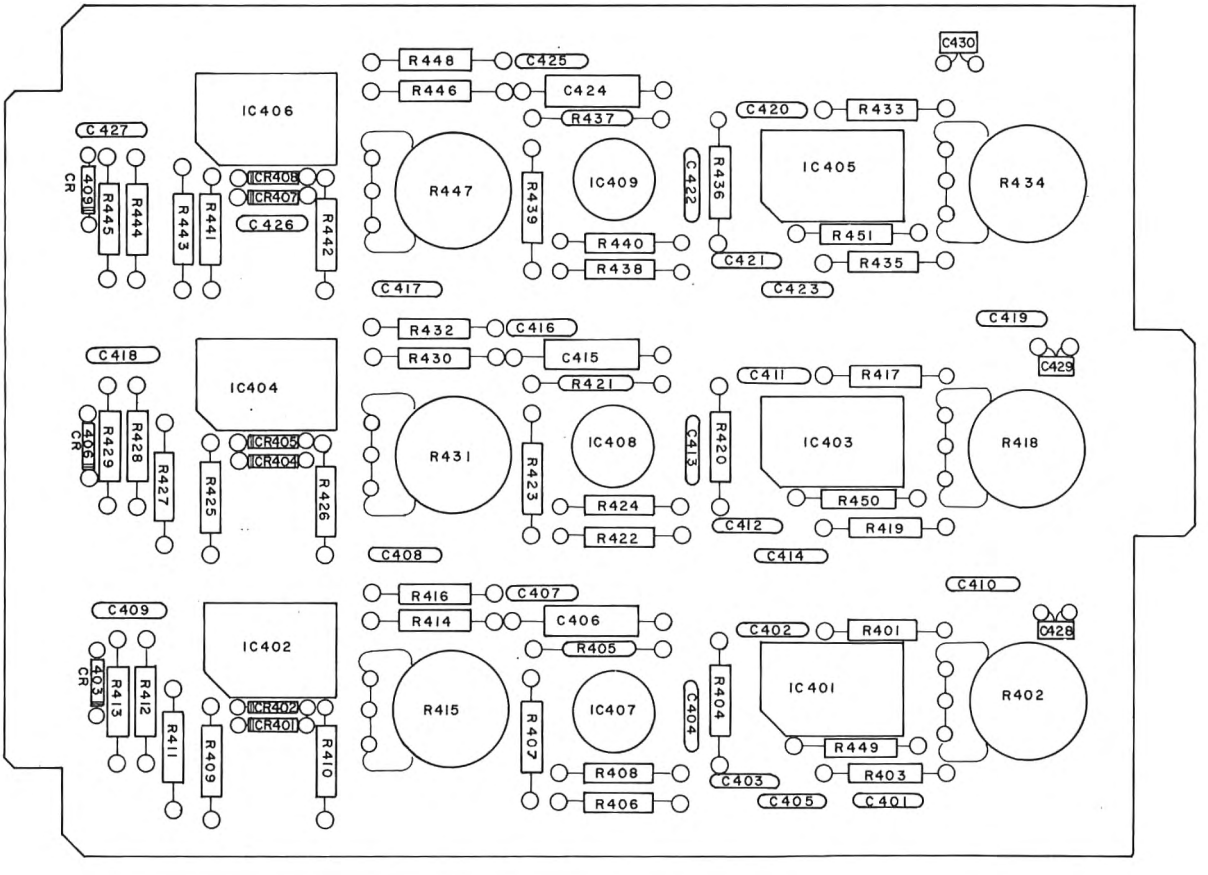

Fig. 6-5 Component location E95499

PC Bd. E95502
Logic & Gate Matrix

R501 thru R515	R: 8200Ω ½W 10%	01121	EB
R516	R: 8.2K ½W 10%	01121	EB
R517	R: 560Ω ½W 10%	01121	EB
R518 thru 522	R: 10K ½W 10%	01121	EB
C501 thru 503	C: 0.01μF 50V	71590	CK 103
C504, 505	C: 100μF 15V	13606	TE 1162
C506, 507	C: 0.01μF 50V	71590	CK 103
CR501, 502	Diodes Germanium	12065	1N198
IC501 thru 504	Integrated circuits	01295	SN7490N
IC505 thru 508	Integrated circuits	13606	USN7401A
IC509 thru 512	Integrated circuits	01295	SN7490N
IC513 thru 516	Integrated circuits	13606	USN7401A
IC517 thru 520	Integrated circuits	01295	SN7490N
IC521 thru 524	Integrated circuits	13606	USN7401A
IC525 thru 528	Integrated circuits	01295	SN7490N
IC529 thru 534	Integrated circuits	13606	USN7401A
IC535	Integrated circuit	01295	SN7482N
IC536	Integrated circuit	01295	SN7401N
IC537 thru 540	Integrated circuits	01295	SN7475N

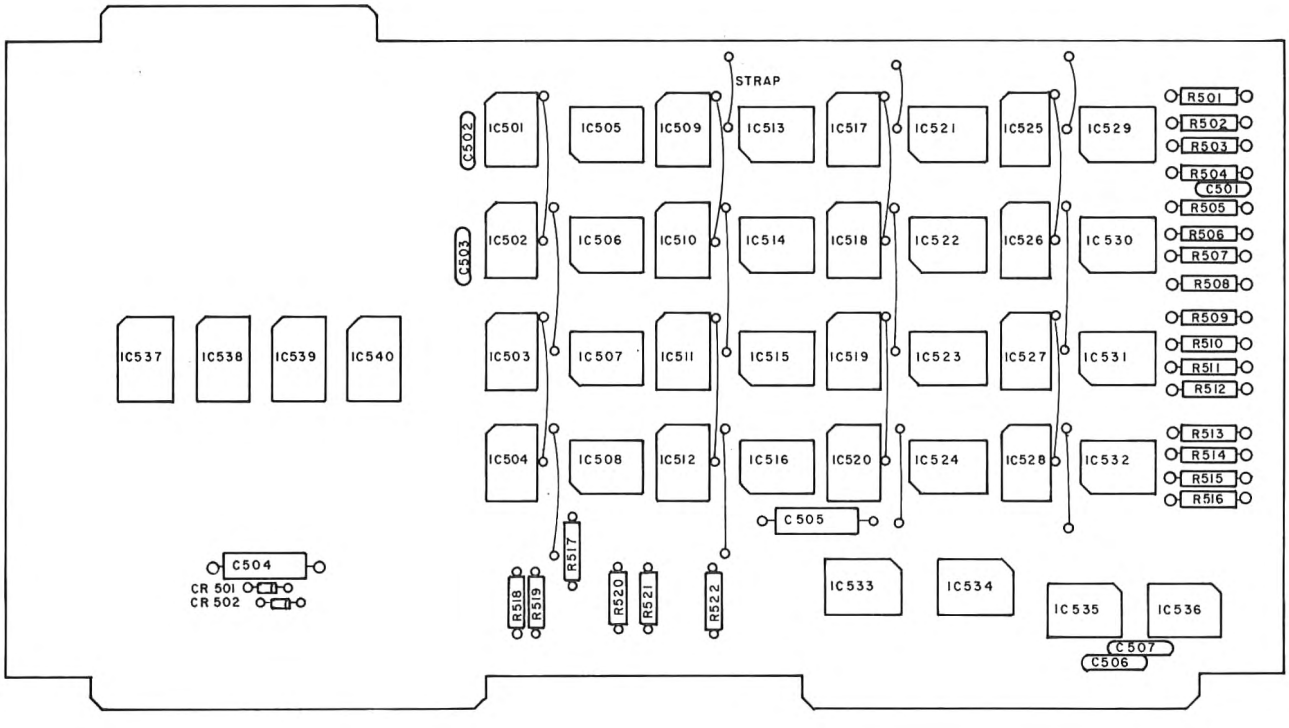

Fig. 6-6 Component location E95502

PC Bd. E95480
Power Supply

Ref Desig.	Description	Manufacturer (FSCM Code No.)	Part Number
R601	R: 15Ω ½W 10%	01121	EB
R602	R: 30Ω ½W 5%	01121	GB
R603, 604	R: 620Ω ½W 5%	01121	EB
R605	R: 700Ω 1W 5%	13606	239E7015
R606	Pot: 1K	71450	UPE200RE-1
R607	R: 3.83K 1/8W 1%	07716	CEATO
R608	R: 11.80K 1/8W 1%	07716	CEATO
R609	R: 1K ½W 10%	01121	EB
R610	R: 12.1K 1/8W 1%	07716	CEATO
R611	Pot: 2K	71450	UPE200RE-1
R612	R: 12.1K 1/8W 1%	07716	CEATO
R613	R: 4.53K 1/8W 1%	07716	CEATO
R614	R: Pot: 2K	71450	UPE200RE-1
R615	R: 5.49K 1/8W 1%	07716	CEATO
R616	R: 1500Ω ½W 10%	01121	EB
R617	R: 2K ½W 5%	01121	EB
R618	R: 1500Ω ½W 10%	01121	EB
R619	R: 1K ½W 10%	01121	EB
R620, 621	R: 470Ω ½W 5%	01121	EB
R622	R: 200Ω ½W 5%	01121	EB
R623	R: 100K ½W 10%	01121	EB
C602 thru 605	C: 250μF 50V	13606	39D257G050HE4
C606	C: 100μF 15V	13606	TE1162
C607, 608	C: 50μF 250V	13606	39D506F250JE4
C609 thru 611	C: 200μF 15V	05844	APD104
C612	C: 200pf 1 Kv 10%	71590	DD 201
C613	C: .005μF 1Kv	71590	DD502
C614	C: 200pf 1Kv 10%	71590	DD 201
C615	C: .005μF 1Kv	71590	DD 502
C616	C: 1μF 25V	13606	5C13
CR601, 602	Diode, rectifiers, Silicon	81483	5A1
CR603, 604	Diode, Silicon	12065	1N4148
CR605	Diode, zener 5.1V 5%	12954	1N751A
CR606	Diode, zener 6.2V 5%	15873	1N823
CR607	Diode Bridge	07716	NSS3058A
CR608	Diode Bridge	07716	NSS3064A
CR609	Diode, zener 24V 5%	16352	1N970B
Q601, 602	Transistors NPN	15873	MPS6515
Q603	Transistor NPN	15873	2N3903
Q604	Silicon controlled rectifier	06486	2N1595
Q605	Transistor: NPN	01295	TIP 29
Q606	Transistor: PNP	01295	TIP 30
IC601, 602	Integrated circuits	01295	SN72709

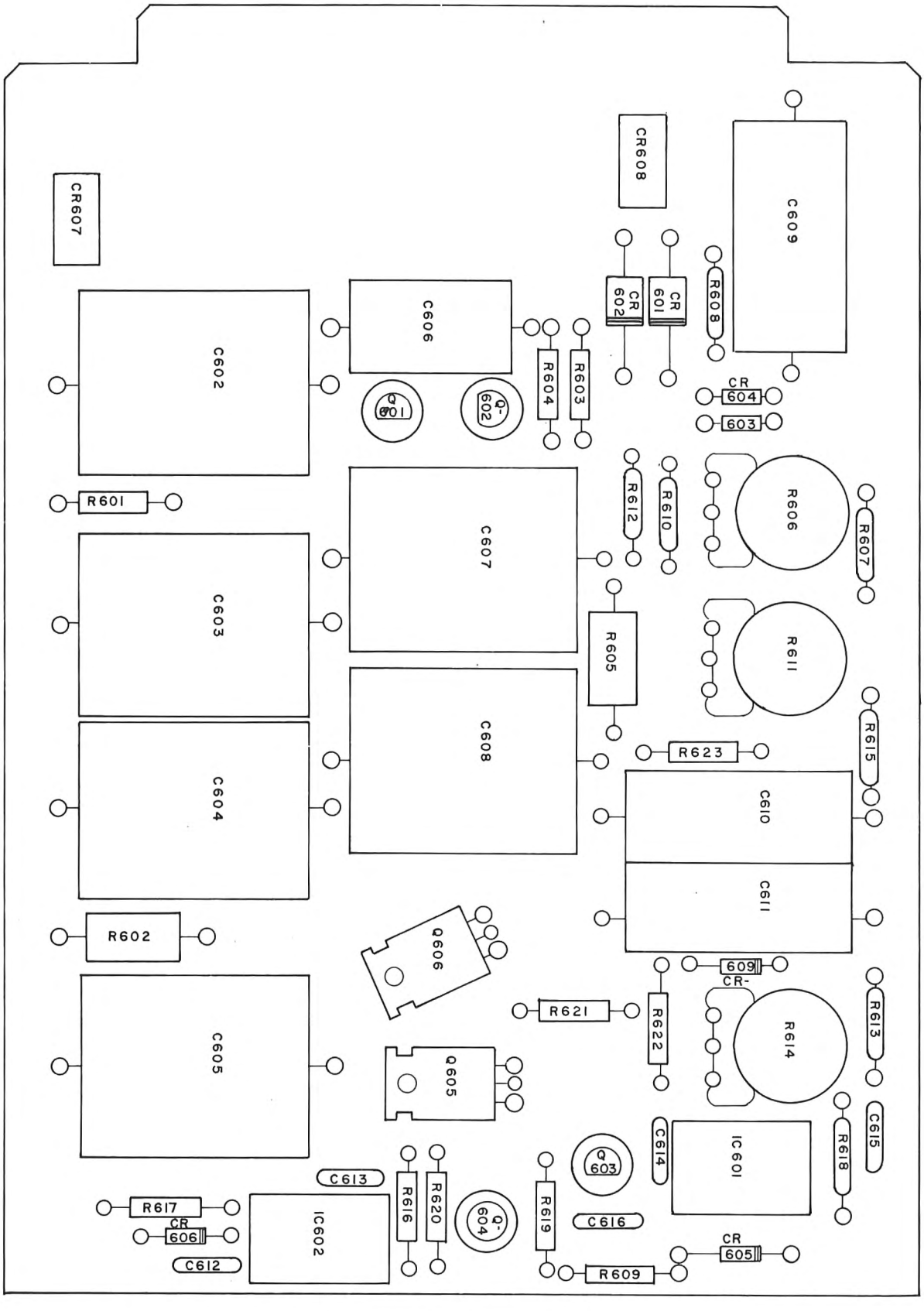

Fig. 6-7 Component location E95480

PC Bd. E95500

DC-LOG Converter and Control Logic.

Ref Desig.	Description	Manufacturer (FSCM Code No.)	Part Number
R701	R: 510Ω ½W 5%	01121	EB
R702, 703	R: 12K ½W 10%	01121	EB
R704	R: 510Ω ½W 5%	01121	EB
R705	R: 1.18K 1/8W 1%	07716	CEATO
R706	Pot: 1K	71450	UPE200RE-1
R707	R: 9.76K 1/8W 1%	07716	CEATO
R708	R: 10K ½W 10%	01121	EB
R709	R: 330Ω ½W 10%	01121	EB
R710	R: 10K ½W 10%	01121	EB
R711	R: 22K 1/8W 1%	07716	CEATO
R712	R: 47.5K 1/8W 1%	07716	CEATO
R713	Pot: 100K	71450	UPE200RE-1
R714	R: 10K 1/8W 1%	07716	CEATO
R715	Pot: 20K	71450	UPE200RE-1
R716	R: 470K ½W 10%	01121	EB
R717	R: 22K 1/8W %	07716	CEATO
R718	R: 150.0Ω ½W 10%	01121	EB
R719	R: 10Ω ½W 10%	01121	EB
R720	R: 12Ω ½W 5%	01121	EB
R721	R: 100K ½W 10%	01121	EB
R722	R: 10K ½W 10%	01121	EB
R723	R: 100K ½W 10%	01121	EB
R724	R: 20K ½W 5%	01121	EB
R725	R: 3.3K ½W 10%	01121	EB
R726	R: 20K 5W 5%	13606	243E2035
R727 thru R732	R: 10K ½W 10%	01121	EB
R733, 734	R: sel val	01121	EB
R735	R: 100K ½W 10%	01121	EB
R736	R: 10K ½W 10%	01121	EB
R737	R: 100Ω ½W 10%	01121	EB
C701	C: 0.01μF 50V	71590	CK 103
C702, 703	C: 0.12μF 75V	13606	225PZ
C704, 705	C: 0.015μF 100V	13606	225PW
C706	C: 10μF 20V	13606	150D106X9020B2
C707	C: 3.3pf 1Kv ±0.5 pf	71590	DD 3R3
C708	C: 0.01μF 50V	71590	CK 103
C709	C: 510pf 1Kv 10%	71590	DD 511
C710	C: 10pf 1Kv 10%	71590	DD 100
C711	C: 150pf 1Kv 10%	71590	DD 151
C712	C: 0.0047μF 100V	13606	225P
C713, 714	C: 0.01μF 50V	71590	CK 103
C715	C: 150pf 1Kv 10%	71590	DD 151
C716	C: 0.01μF 50V	71590	CK 103
C717	C: 22pf 1Kv 10%	71590	DD 220
C718	C: 680pf 1Kv 10%	71590	DD 681
C719	C: 0.001μF 1Kv 10%	71590	DD 102
C720	C: 0.01μF 50V	71590	CK 103
C721	C: 1.0μF 25V	13606	5C13
CR701 thru 707	Diodes Silicon	12065	1N4148
Q701 thru Q704	Transistors NPN	15873	2N3903
Q705, 706	Transistors: FET	15873	MPF152

E95500 (cont.)

Ref Desig.	Description	Manufacturer (FSCM Code No.)	Part Number
Q707 thru 709	Transistors: NPN	49671	40327
Q710	Transistor: NPN	15873	2N3903
Q711	Transistor: NPN	49671	40327
Q712	Transistor: NPN	15873	2N3903
IC701, 702	Integrated circuits	01295	SN7490N
IC703	Integrated circuits	18324	SP380A
IC704	Integrated circuit	01295	SN7472N
IC705	Integrated circuit	01295	SN7473N
IC706, 707	Integrated circuits	01295	SN72709

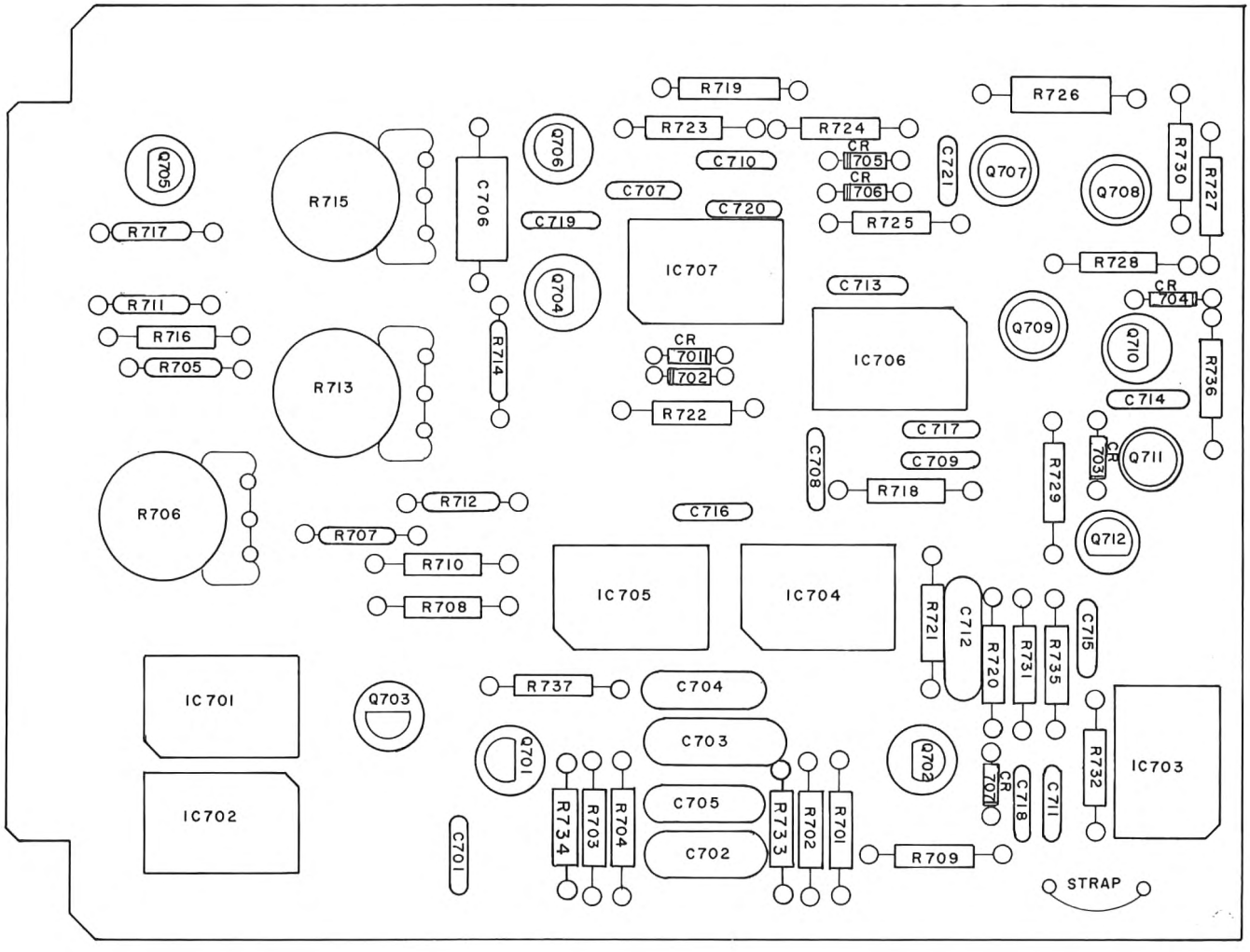

Fig. 6-8 Component location E95500

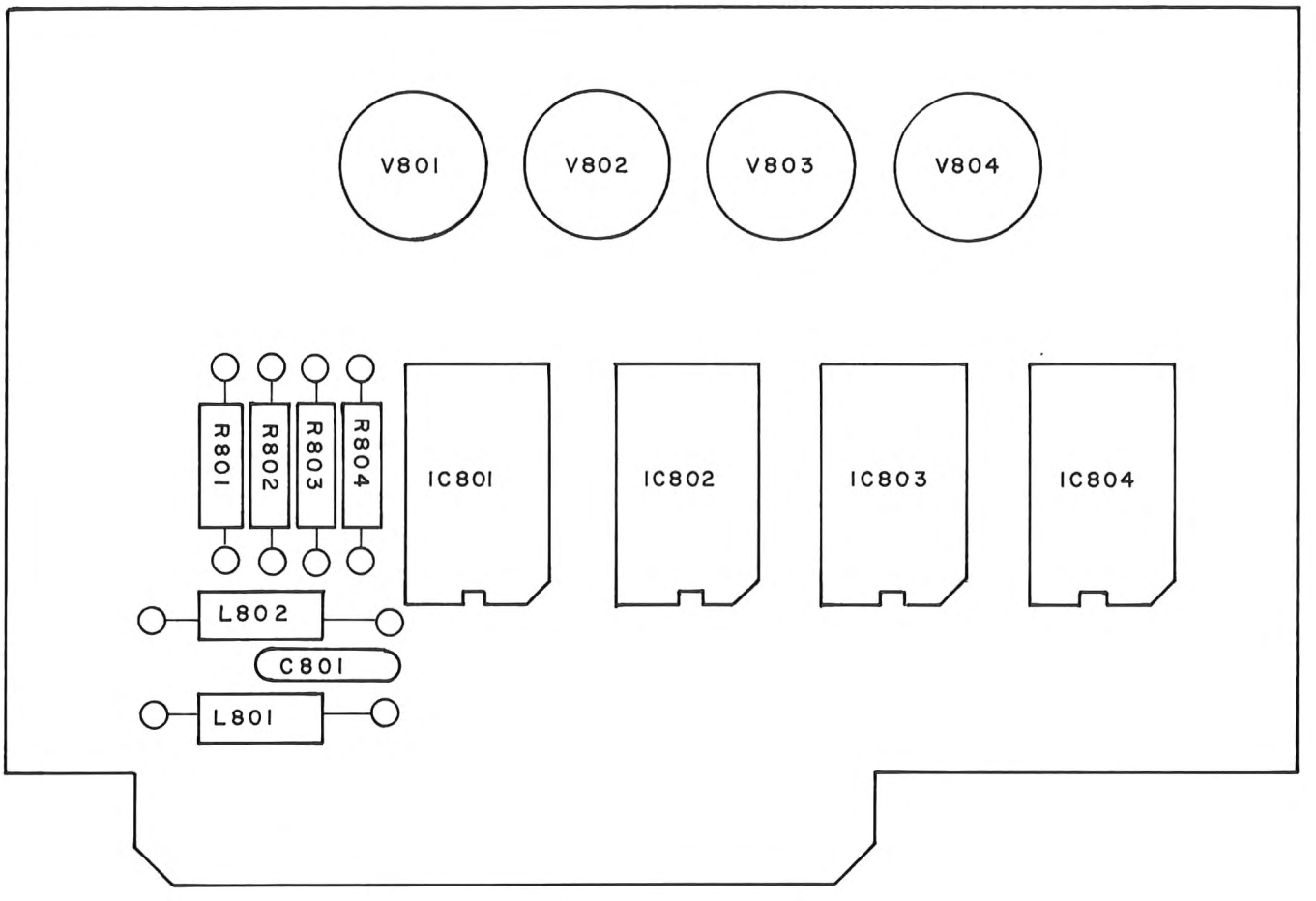

Fig. 6-9 Component location E95496

PC Bd. E95496
Decoder-Driver and Readout

R801	R: 15K 1W 10%	01121	GB
R802 thru 804	R: 10K ½W 10%	01121	EB
C801	C: 0.005μF 1Kv	71590	DD 502
L801, 802	Inductor: 100MH	76493	9350-08
IC801 thru 804	Integrated circuits	01295	SN7441AN
V801 thru 804	Numerical Readout Tubes	06107	NL-950

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PC Bd. E95464 AC-DC Converter

Ref Desig.	Description	Manufacturer (FSCM Code #)	Part Number
R901	R: 1K ½W 10%	01121	EB
R902	R: 270K ½W 10%	01121	EB
R903	R: 390K ½W 10%	01121	EB
R904	R: 1500Ω ½W 10%	01121	EB
R905	Pot: 1 Meg	71450	UPE200RE-1
R906	R: 4.7K ½W 10%	01121	EB
R907	R: 680Ω ½W 5%	01121	EB
R908	R: 150K ½W 5%	01121	EB
R909	R: 270Ω ½W 10%	01121	EB
R910	R: 68K ½W 5%	01121	EB
R910A	R: selected value	01121	EB
R911	R: 22K ½W 10%	01121	EB
R912	R: 1K ½W 10%	01121	EB
R913	R: 1.2K ½W 10%	01121	EB
R914, 915	R: 1K ½W 10%	01121	EB
R916	R: 2.2K ½W 5%	01121	EB
R917	R: 390Ω ½W 10%	01121	EB
R918	R: 10K ½W 10%	01121	EB
R919, 920	R: 100K ½W 10%	01121	EB
R921, 922	R: 3.48K 1/8W 1%	07716	CEATO
R923	R: 390Ω ½W 10%	01121	EB
R924	R: 10K ½W 10%	01121	EB
R925, 926	R: 47K ½W 10%	01121	EB
R927	R: 4.12K 1/8W 1%	07716	CEATO
R927A	33K ½W 5%	01121	EB
R928	R: 100K ½W 5%	01121	EB
R929	Pot: 500K	71450	UPE200RE-1
R930	R: 150K ½W 5%	01121	EB
R931	R: 1500Ω ½W 10%	01121	EB
R932	R: 51Ω ½W 5%	01121	EB
R933	R: 4.7K ½W 10%	01121	EB
R934	R: 1800Ω ½W 5%	01121	EB
R935	R: 56Ω ½W 5%	01121	EB
R936	R: 82K ½W 5%	01121	EB
C901, 902	C: 0.47μF 25V	13606	5C11
C903	C: 100pf 1Kv 10%	71590	DD101
C904	C: 3.3pf 1Kv ±0.5pF	71590	DD3R3
C905	C: 10μf 10V 10%	05397	K10W10K
C906	C: 0.082μF 20V 20%	05397	KR082W20K
C907	C: 15μF 10V 10%	05397	K15W10K
C908	C: 10μF 10V 10%	05397	K10W10K
C909	C: 56μF 15V 10%	13606	150D566X9015R2
C910	C: 22μF 20V 10%	13606	150D226X9020B2
C911	C: 100μF 15V	13606	TE 1162
C912, thru 915	C: 10μF 20V 10%	13606	150D106X9020B2
C916, 917	C: 2.2μF 35V 10%	05397	K2R2W35K
C918	C: 510pf 1Kv 10%	71590	DD511
C919	C: 22pf 1Kv 10%	71590	DD220
C920, 921	C: 0.47μF 25V	13606	5C11
C922	C: 15μF 10V 10%	05397	K15W10K
C923	C: 100μF 15V	13606	TE1162
C924	C: 0.47μF 25V	13606	5C11
C925	C: 22μF 5V 10%	05397	K22W6K
CR901 thru 904	Diode Silicon	12065	1N4148
Q901 thru 904	Transistor : NPN	15873	MPS-6515
IC901, 902	Integrated circuit	01295	SN72709

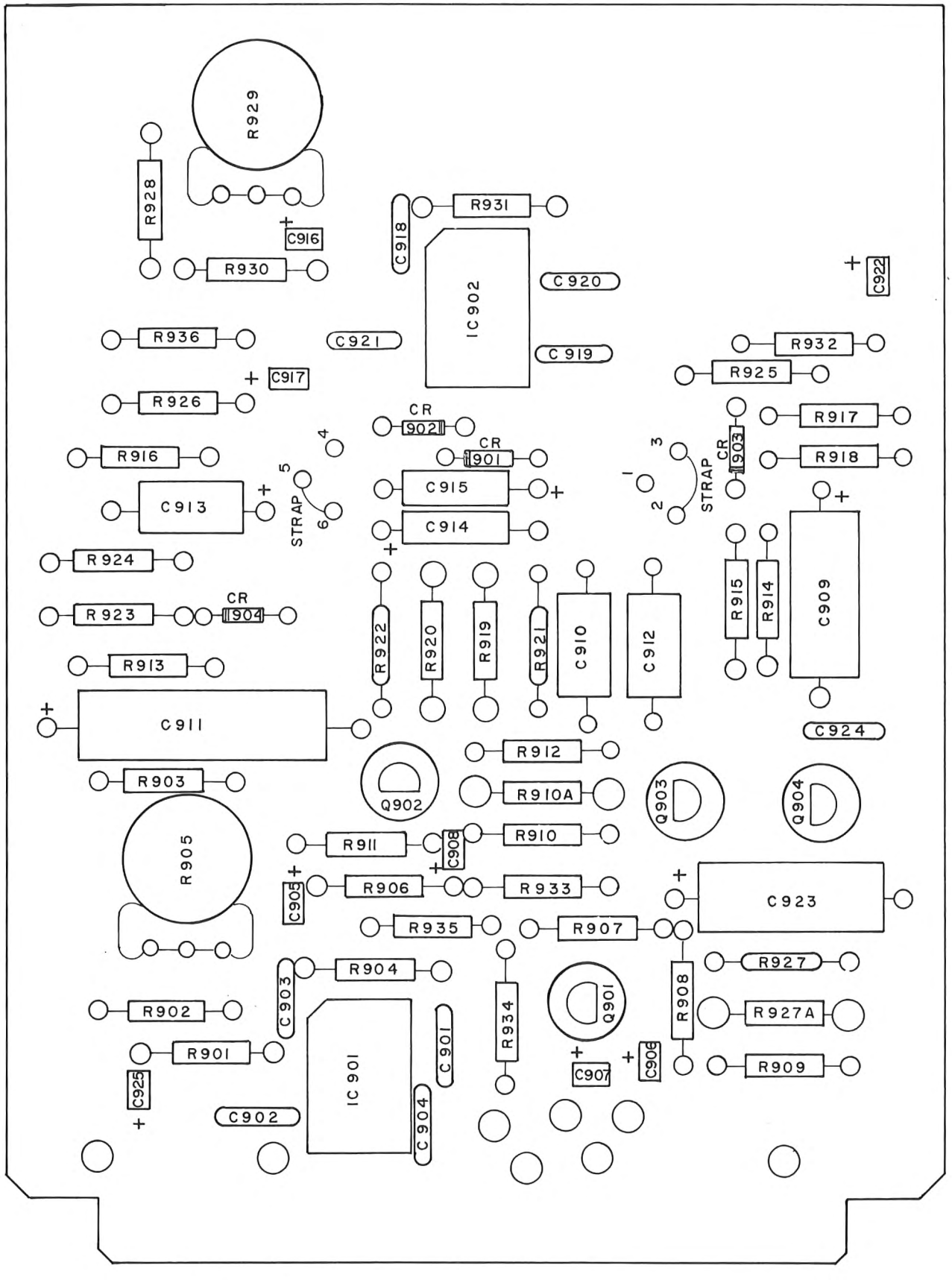


Fig. 6-10 Component location E95464

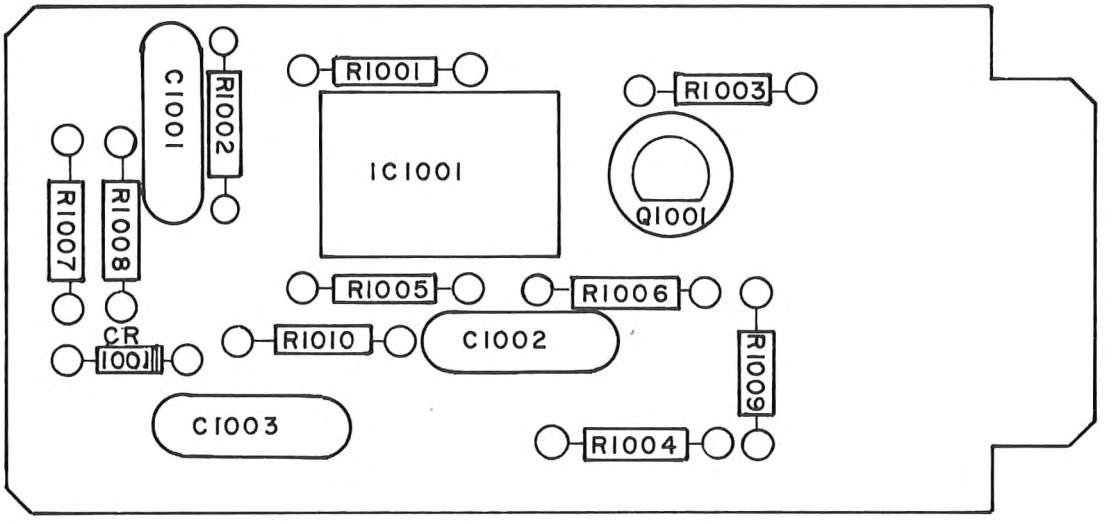


Fig. 6-11 Component location E95498

PC Bd. E95498
Reset & Inhibit Logic

R1001 thru 1004	R: 5.6K $\frac{1}{4}$W 10%	01121	CB
R1005 thru 1008	R: 10K $\frac{1}{4}$W 10%	01121	CB
R1009	R: 560Ω $\frac{1}{4}$W 10%	01121	CB
R1010	R: 2.7K $\frac{1}{4}$W 10%	01121	CB
C1001	C: 0.47μF 75V	13606	225PW
C1002	C: 0.1μF 100V	13606	225PW
C1003	C: 0.001μF 100V	13606	225PW
CR1001	Diode Silicon	12065	1N4148
Q1001	Transistor: NPN	15873	MPS 6515
IC1001	Integrated circuit	18324	SP380A

PC Bd. E95284
Line Noise Filter

C1201, 1202	C: 470pf 1Kv	71590	CE471
L1201, 1202	Inductors: 100 MH	76493	9350-08

Ref Desig.	Description	Manufacturer (FSCM Code No.)	Part Number
R1	Pot: 10K Model 4	71590	BA401-000
R2	Pot: 10K Type AB	44655	CU1031
R3	R: 410.2Ω 1/8W 1%	07716	CEATO
R4	R: 130Ω 1/8W 1%	07716	CEATO
R5	R: 41.2Ω 1/8W 1%	07716	CEATO
R6	R: 681Ω 1/8W 1%	07716	CEATO
R7	R: 215Ω 1/8W 1%	07716	CEATO
R8	R: 19.1Ω 1/8W 1%	07716	CEATO
R9	R: 68.1Ω 1/8W 1%	07716	CEATO
R10	R: 31.6Ω 1/8W 1%	07716	CEATO
R11	R: 2707.2Ω 1/8W 1%	07716	CEATO
R12	R: 3090Ω 1/8W 1%	07716	CEATO
R13	R: 7680Ω 1/8W 1%	07716	CEATO
R14	R: 2100Ω 1/8W 1%	07716	CEATO
R15	R: 1347.8 1/8W 1%	07716	CEATO
R16	R: 2320Ω 1/8W 1%	07716	CEATO
R17	R: 1666.7 1/8W 1%	07716	CEATO
R18	R: 453Ω 1/8W 1%	07716	CEATO
R19	R: 590Ω 1/8W 1%	07716	CEATO
R20	R: 294Ω 1/8W 1%	07716	CEATO
R21	R: 210Ω 1/8W 1%	07716	CEATO
R22	R: 145.2 1/8W 1%	07716	CEATO
R23	R: 357Ω 1/8W 1%	07716	CEATO
R24	R: 100Ω $\frac{1}{2}$W 10%	01121	EB
R25	R: 120K $\frac{1}{2}$W 10%	01121	EB
R26	R: 510Ω $\frac{1}{2}$W 5%	01121	EB
R27	R: 1K $\frac{1}{4}$W 10%	01121	CB
R28	R: 18K 1W 10%	01121	GB
R29	R: 15K $\frac{1}{4}$W 10%	01121	CB
R30	R: 15K $\frac{1}{4}$W 10%	01121	CB
C1	C: 4000μF 15V	13606	39D408G015JL4
C2	C: 100μF 150V	13606	D47141
C3	C: 1.0μF	13606	5C13
C4 thru C6	C: 0.47μF 25V	13606	5C11
C7	C: 0.01μF 500V	71590	ID-01
Q1	Transistor, NPN	49671	2N3055
CR1 and CR2	Diode Germanium	80368	1N198

Jacks

Ref Desig.	Description	Manufacturer (FSCM Code No.)	Part Number
J1	Jack: for 310 plug	82389	5J-1329
J2	Jack: for 309 plug	82389	5J-1193
J3	Jack: for 310 plug	82389	5J-1192
J4, J5	Jack: for 310 plug	82389	5J-1329
J6, J7	Binding post	17117	5595-175-2
J8	binding post	17117	5595-175-0
J9	Ground binding post	83330	137-SP
J10	Binding post	17117	5595-175-2
J11	Binding post	17117	5595-175-2
J12	Binding post	17117	5595-175-0
J13	Jack: monitor output	82389	12B
J14	AC receptacle	82389	AC3G
J15	Jack: for 310 plug	82389	5J-1329

Switches

S1	S: Turnbutton	82389	9S-1175
S2	S: 115-230V ac Selector (DPDT)	82389	46206LF
S3	S: Minimum Level	06819	A-1405820050
S4	S: Channel selector	06819	A-1405820051
S5	S: Increment	06819	A-1405820052
S6	S: Network	06819	A-1405820078
S7	S: Blanking Interval	06819	A-1405820079
S8	S: Timer	79919	71002J
S9	S: Power (DPDT)	09353	7201
S10	S: Display key switch	82389	41203
S11	S: Reset key switch	82389	XA-40777
S12 thru S20	S: pushbutton	71590	2KBM035100

Transformers

T1	Transformer: Power	17538	4202-021316
T2	Transformer: Input Balance	86632	NES3345D
L1	Inductor: Hold coil	06819	TN 1274

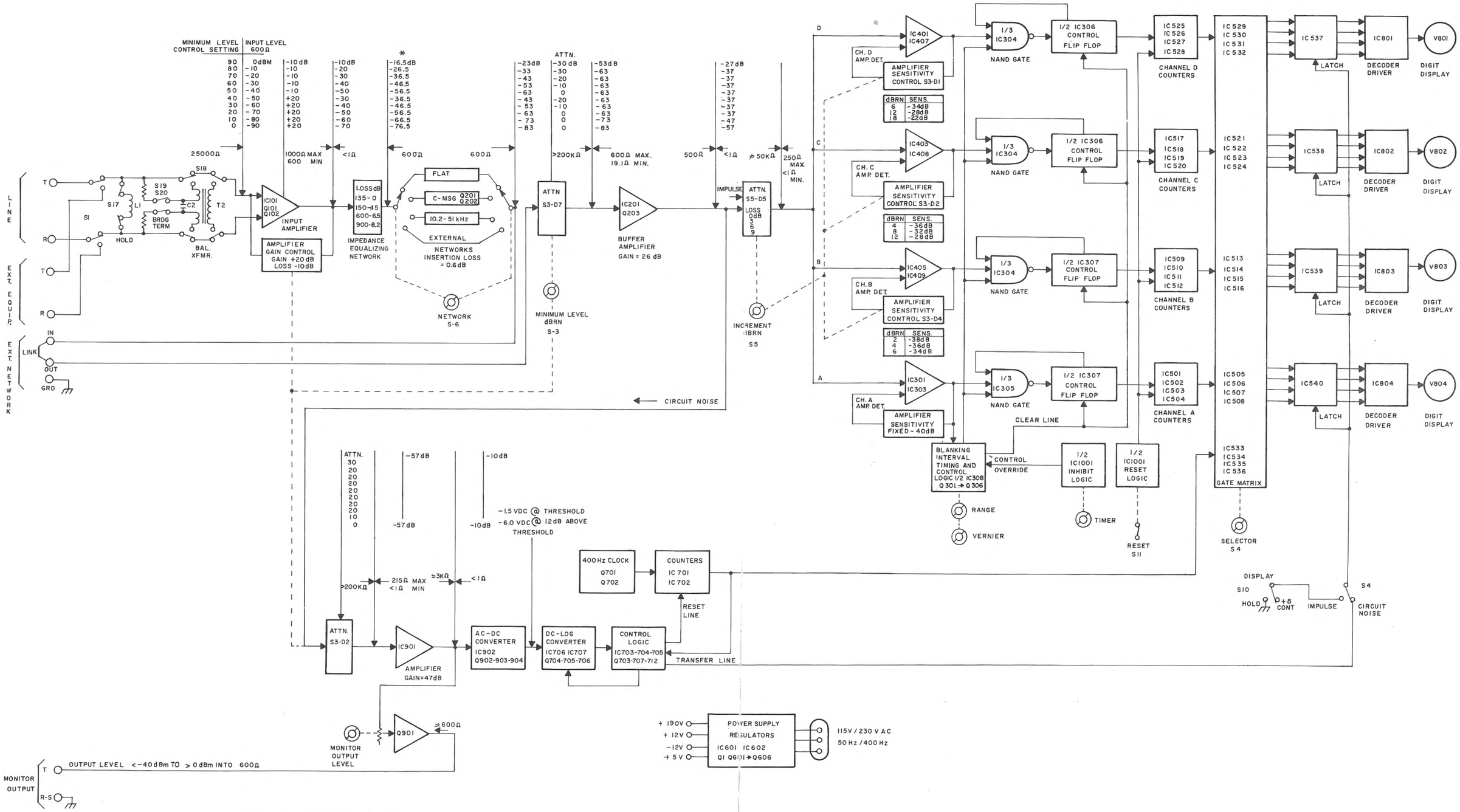
Fuses

F1	Fuse: 3/10 amp slo-blo	75915	313-300
F2	Fuse: 3 amp	75915	3AG-3A
XF2	Fuse holder	75915	357001
DS1	Pilot light	72765	HR118T-603
DS2	Over Range Indicator light	72765	HR118T-603
	Shorting link	24655	938-L

SECTION 7

SCHEMATIC DIAGRAMS

7.1 INTRODUCTION. The following pages contain the schematic diagrams for the MODEL 58B.



* DISCONNECTED FROM THE WEIGHTING NETWORKS

Fig. 7-1 Model 58B Block Diagram

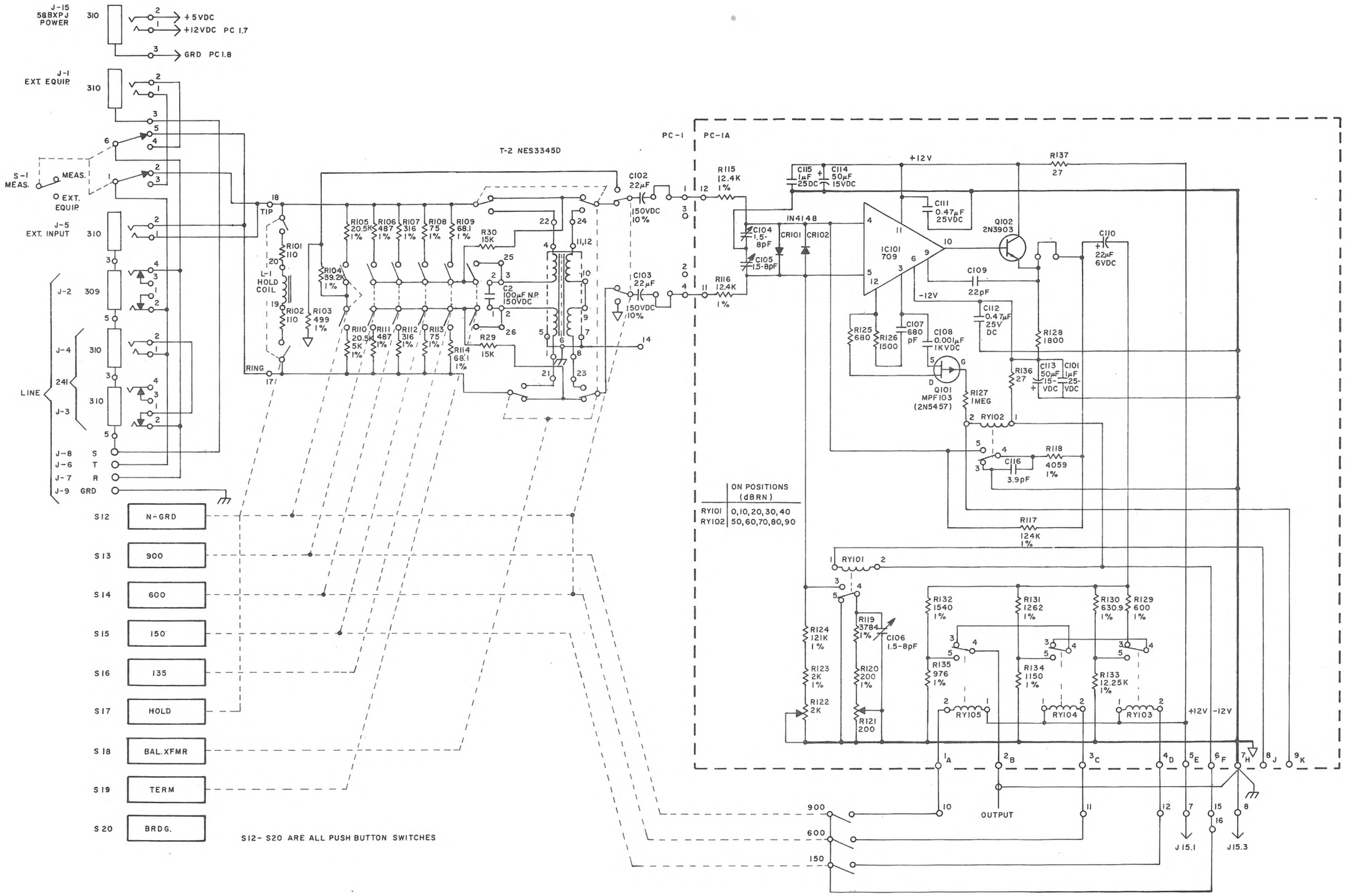


Fig. 7-2 E-14-058-20-32 and
E-14-058-20-38 Schematic Diagram

Fig. 7-2 E-14-058-20-32 and
E-14-058-20-38 Schematic Diagram

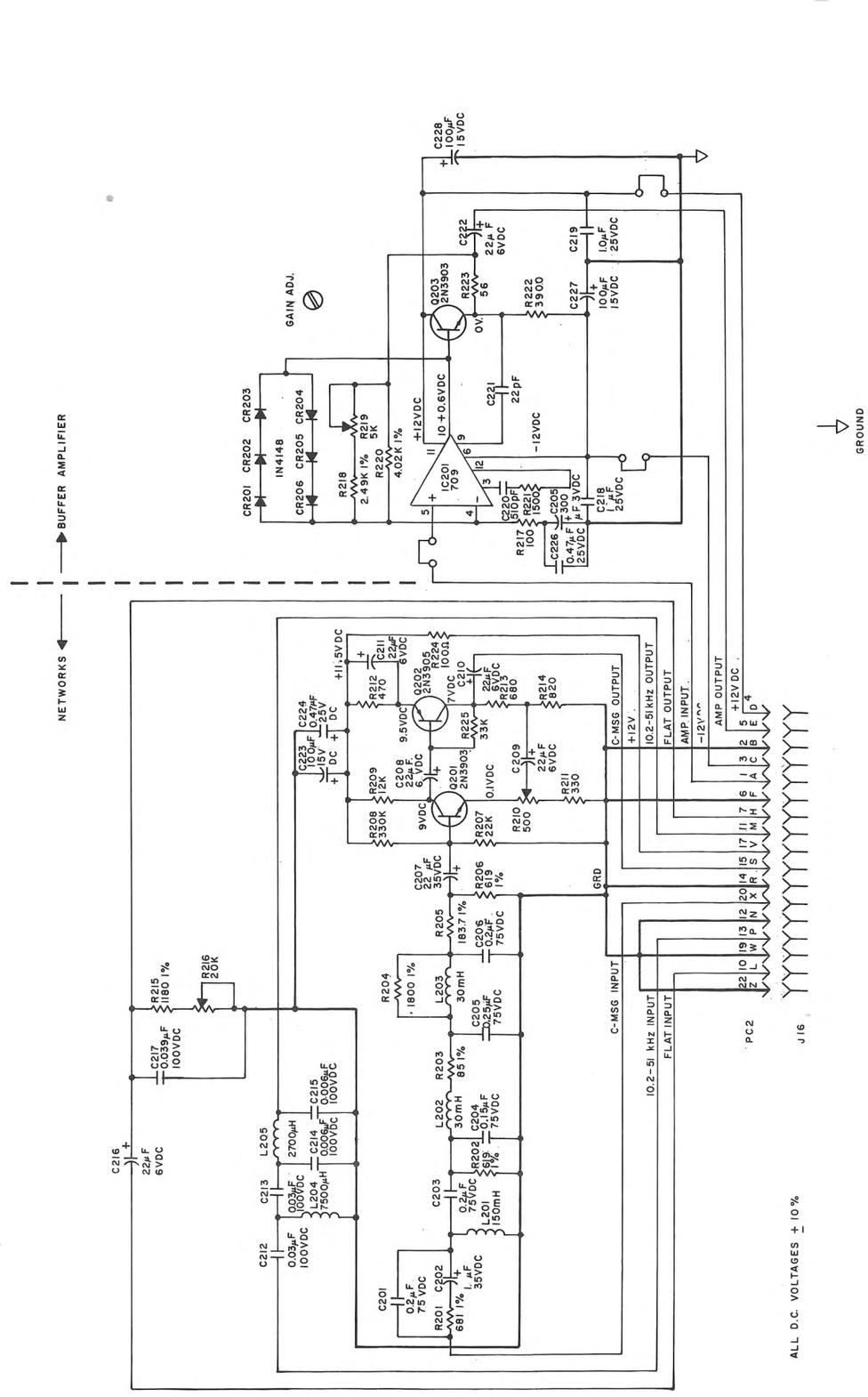


Fig. 7-3 E95510 Schematic Diagram

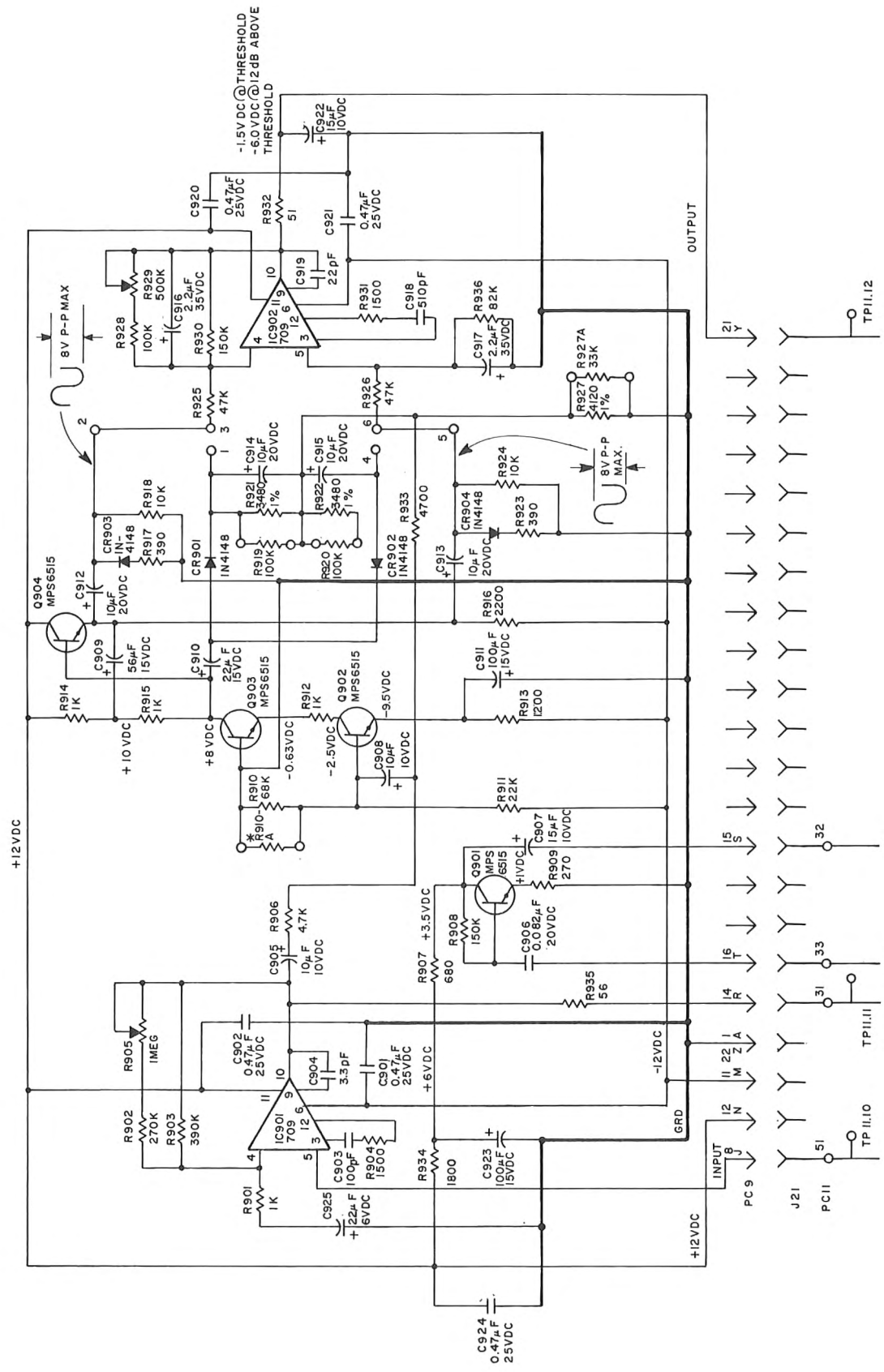


Fig. 7-4 E95464 Schematic Diagram

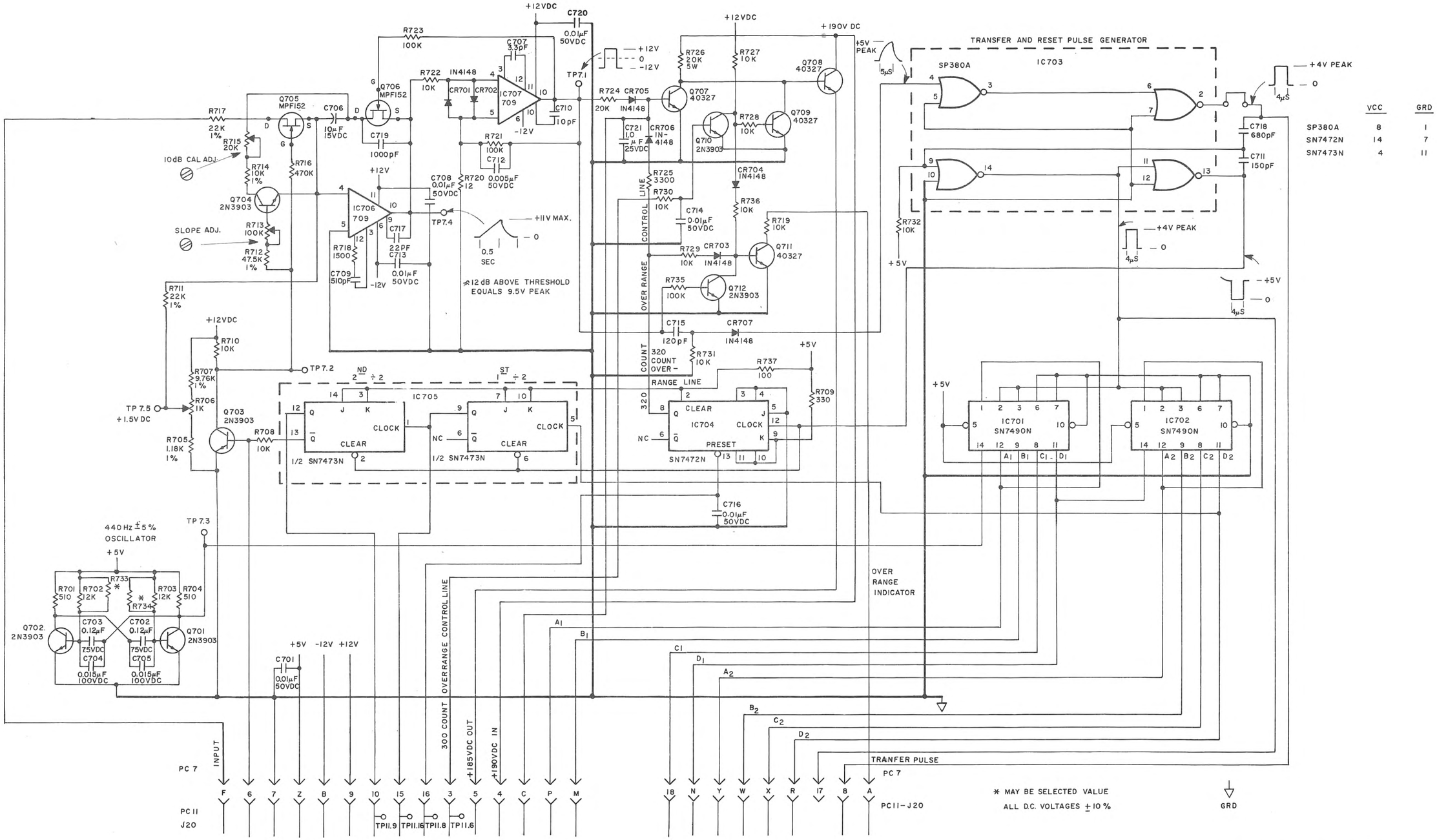


Fig. 7-5 E95500 Schematic Diagram

	V_{CC}	GND
SP 322 B	16	8
SP 380 A	8	1
SN 7410N	14	7

CHANNEL D

CHANNEL C

CHANNEL B

1/3 IC304 SN7410N

+5V

R329 100

1/2 IC306 SP322B

J CLOCK K CLEAR S_D $\overline{Q}$ Q N.C.

1/3 IC304 SN7410N

1/2 IC306 SP322B

1/3 IC304 SN7410N

1/2 IC307 SP322B

+12 VDC

WITH 1 kHz INPUT SIGNAL

≈ 3.5 V P-P @ THRESHOLD

C302 0.47μF 25VDC

BALANCE

R301 10K

R302 10K

R330 1MEG

C301 1μF 25V DC

R303 10K

C303 100pF

R305 1500

TP3.1

IC301 709

C304 3.3pF

IC303 CA3019

R308 22K

R309 3900

R311 1K

R312 560K

CR301 CR302 IN4148

IC302 709

R310 1K

R307 22K

C309 0.47μF 25VDC

+4V 0 -0.7V

TP3.3

R313 3600

+12V 0 -12V

R314 3900

CR303 IN4148

1/3 IC305 SN7410N

1/2 IC307 SP322B

C322 150pF

R332 5.1K

CR306 IN198

TP3.2

-12 VDC

C308 0.47μF 25VDC

R318 3.3K

IC308 1/2 SP380A

C312 0.47μF 25VDC

+5VDC

R306 40.2K 1%

C306 5μF 15VDC

R315 360

R316 1K

SENS. CAL

C307 330pF

R317 1K

Q305 2N3903

Q306 2N3903

R319 100

R320 1K

BLANKING INTERVAL CAL.

R323 91K

R322 10K

R321 510

Q304 2N-3903

R331 10K

+5V 0 ≈ 3μS

C310 150pF

CR304 IN4148

Q303 2N-3903

R324 10K

R328 510

R325 91K

R326 10K

Q302 2N-3903

+5V 0 ≈ 1.5μS

C311 33pF

CR305 IN4148

Q301 2N3903

R327 10K

+4V 0

+3.2V 0 -0.8V

C305 0.47μF 25VDC

C321 22μF 6VDC

R304 1300 1%

C317 22μF 6VDC C318 *

C313 2.2μF 35VDC C314 *

C315 0.22μF 35VDC C316 *

C319 0.022μF 100VDC C320 *

2/3 IC305 SN7410N

CHANNEL A AMP-DET INPUT

J17 J18

+5VDC 5 15 8 GRD 17 -12 V F 22 +12 V Y PC3

PC11-J22

TP11.2 TP11.15 TP11.4

22

* SELECTED VALUE

ALL DC VOLTAGES ±10%

4 A B C D PC3

TP11.7

PC11-J22

E 2

PC3

H M 9 16 L P I N

PC11-J22

TP11.13 TP11.1 TP11.5 TP11.3 TP11.16 TP11.9

10 R V W X

TP11.8 TP11.6

Fig. 7-6 E95501 Schematic Diagram

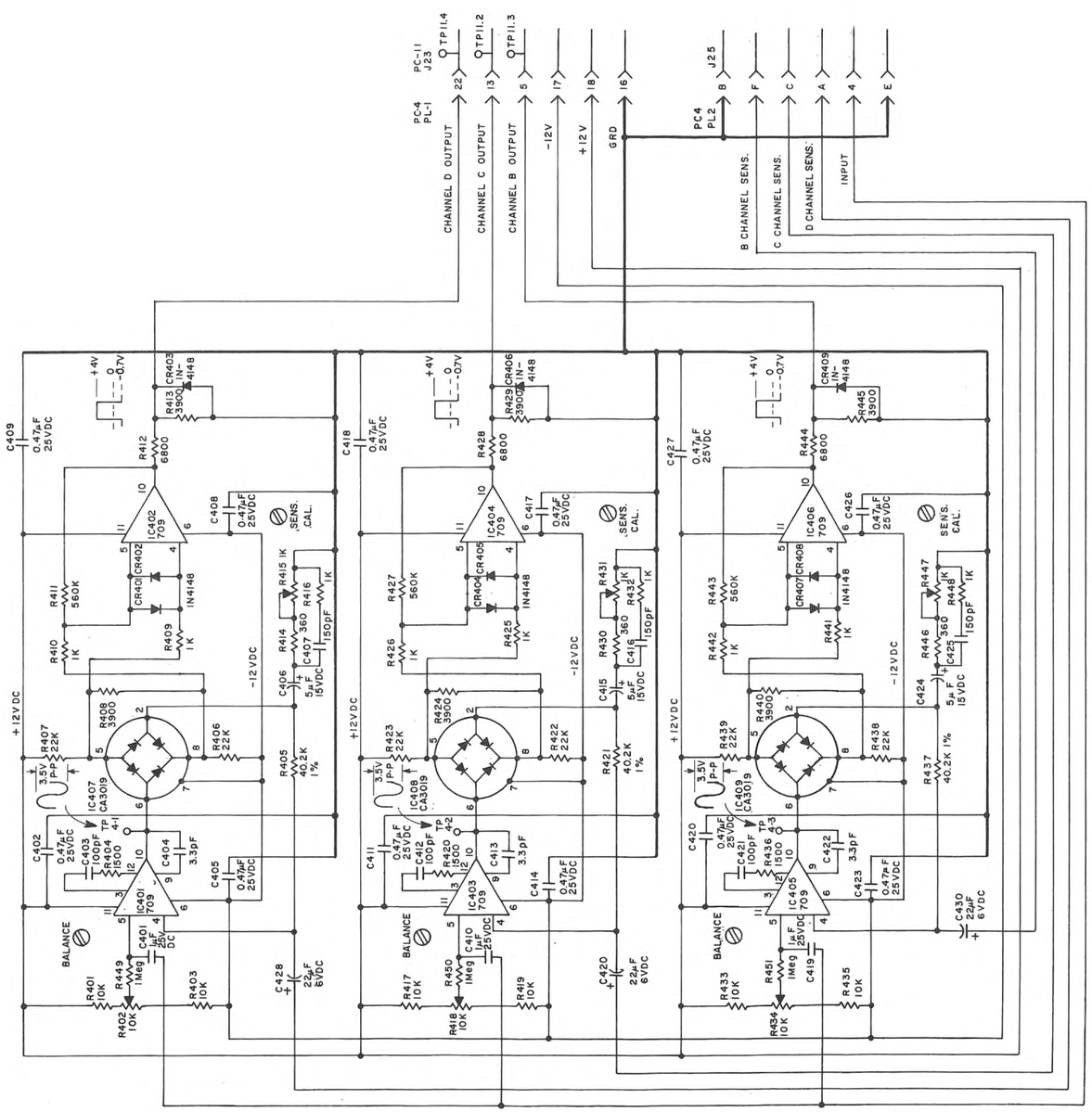


Fig. 7-6 E95501 Schematic Diagram

Fig. 7-7 E95499 Schematic Diagram

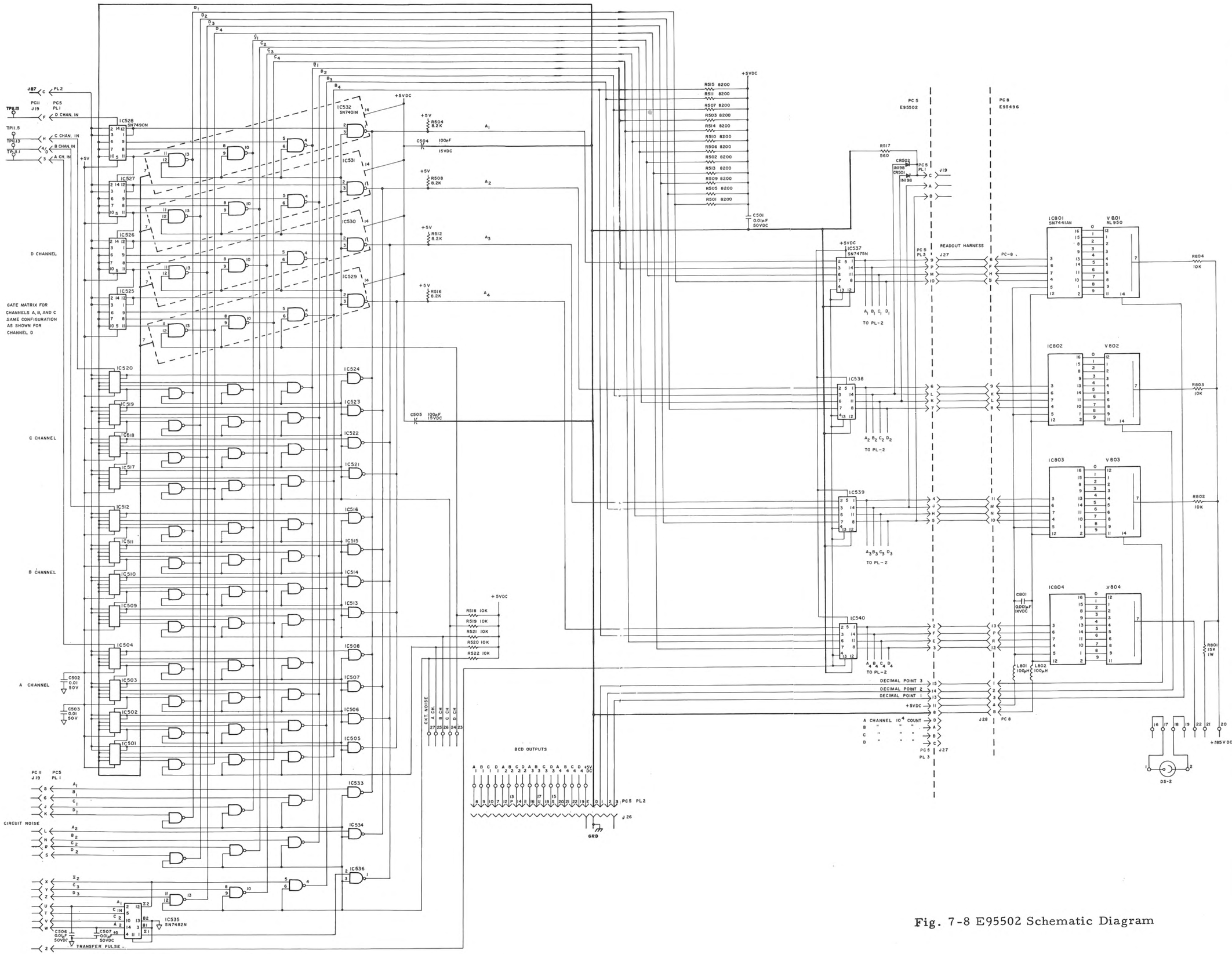


Fig. 7-8 E95502 Schematic Diagram

Fig. 7-8 E95502 Schematic Diagram

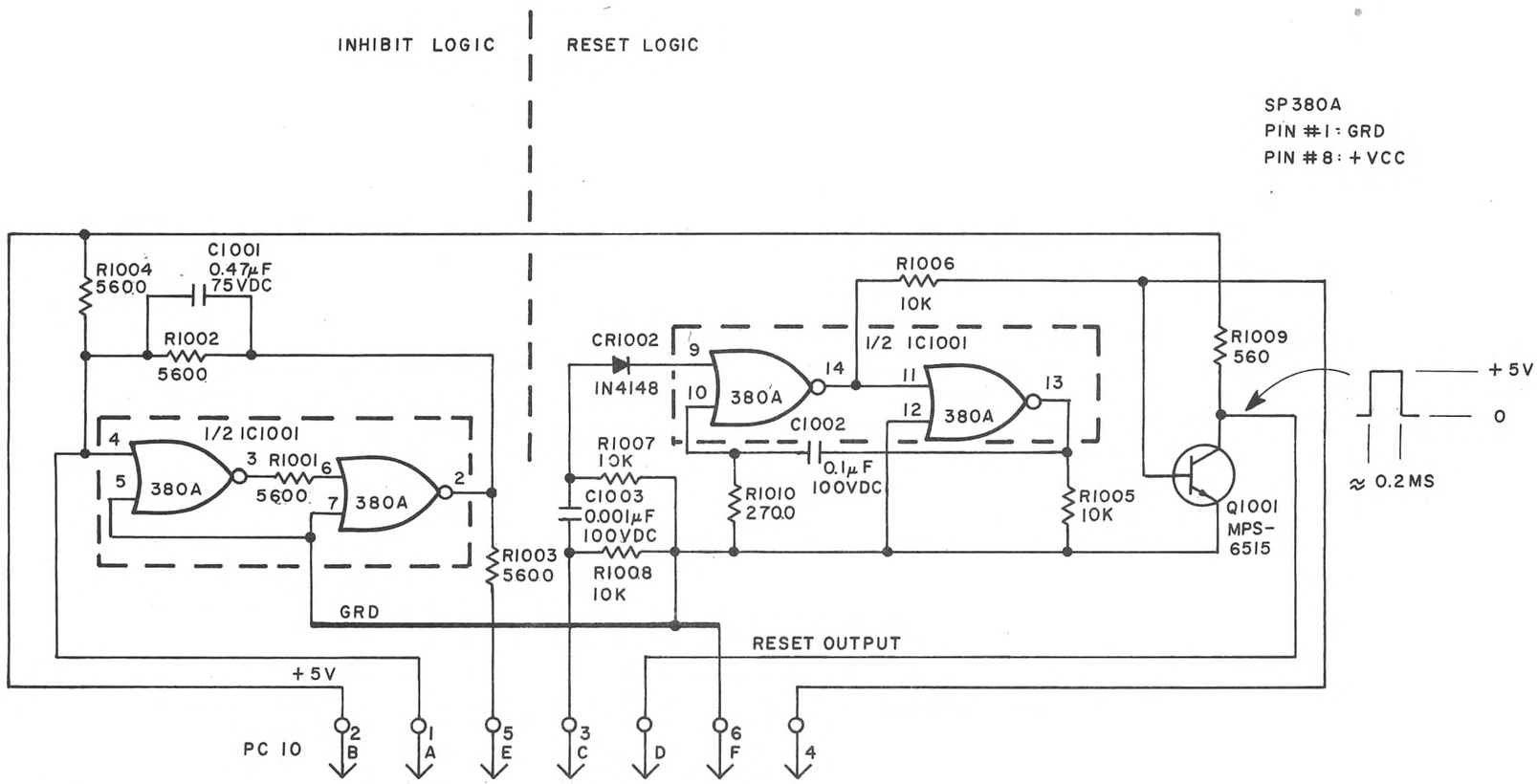
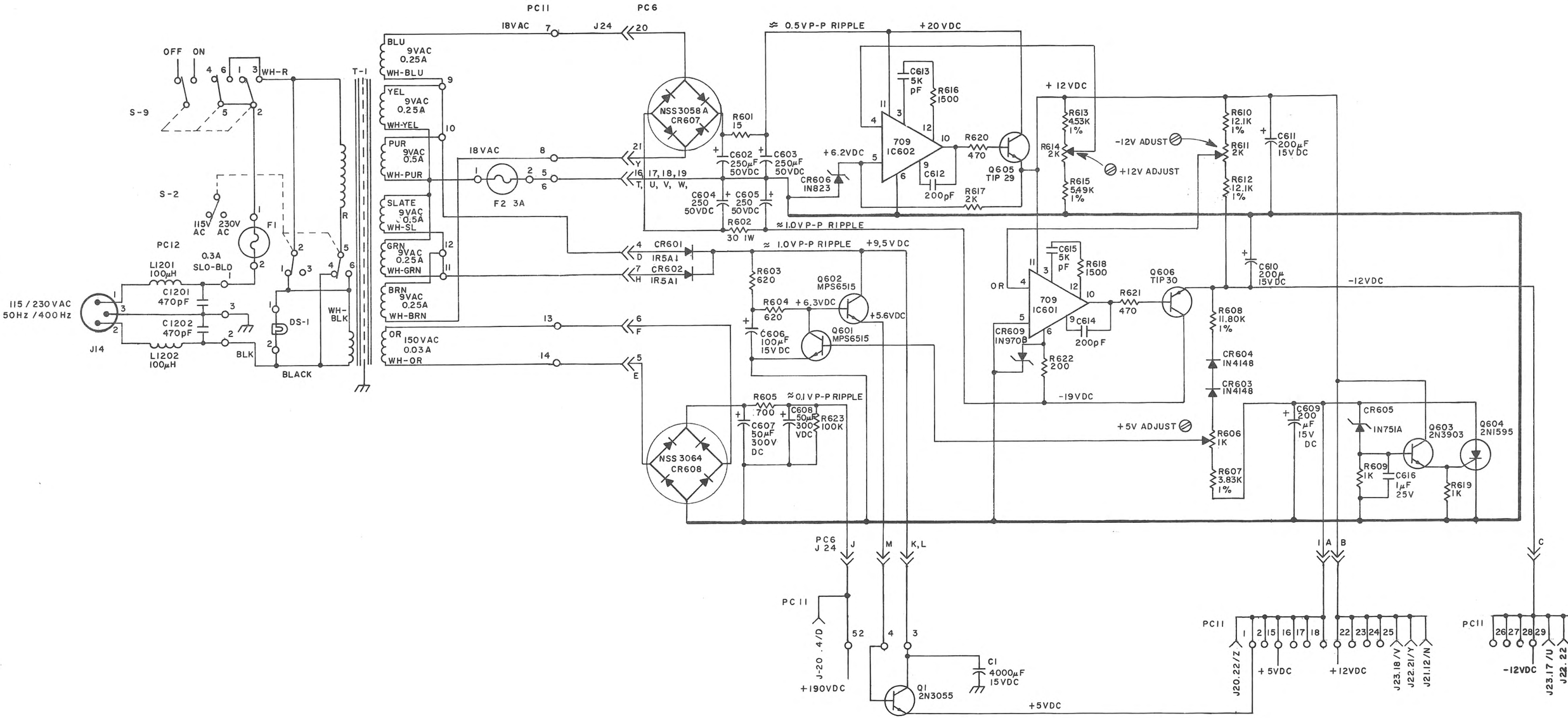


Fig. 7-9 E95498 Schematic Diagram



ALL VOLTAGES INDICATED ARE WITH 117VAC LINE VOLTAGE

Fig. 7-10 E95480 Schematic Diagram

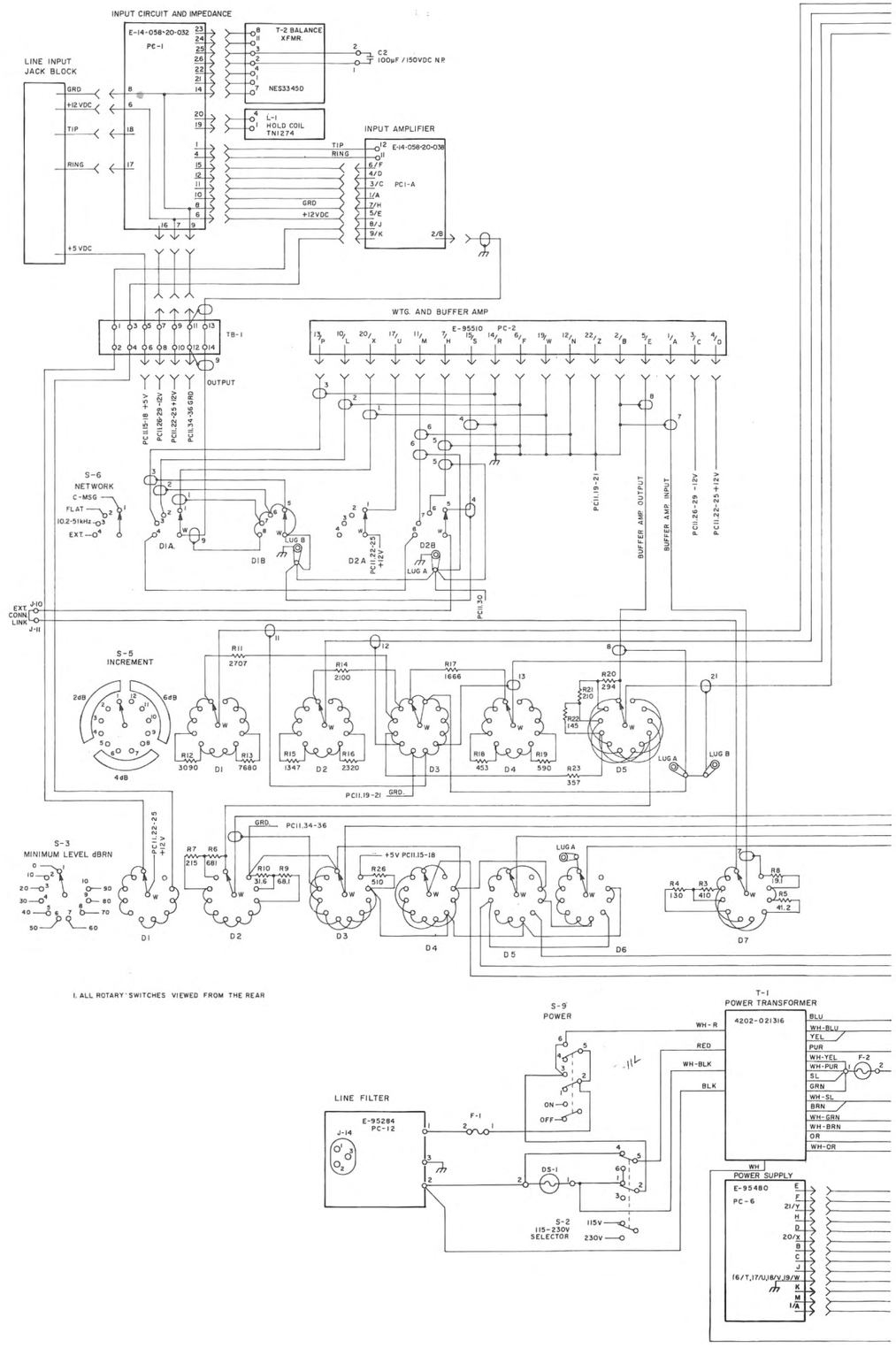


Fig. 7-10 E95480 Schematic Diagram

Fig. 7-11 Model 58B Interconnection Diagram

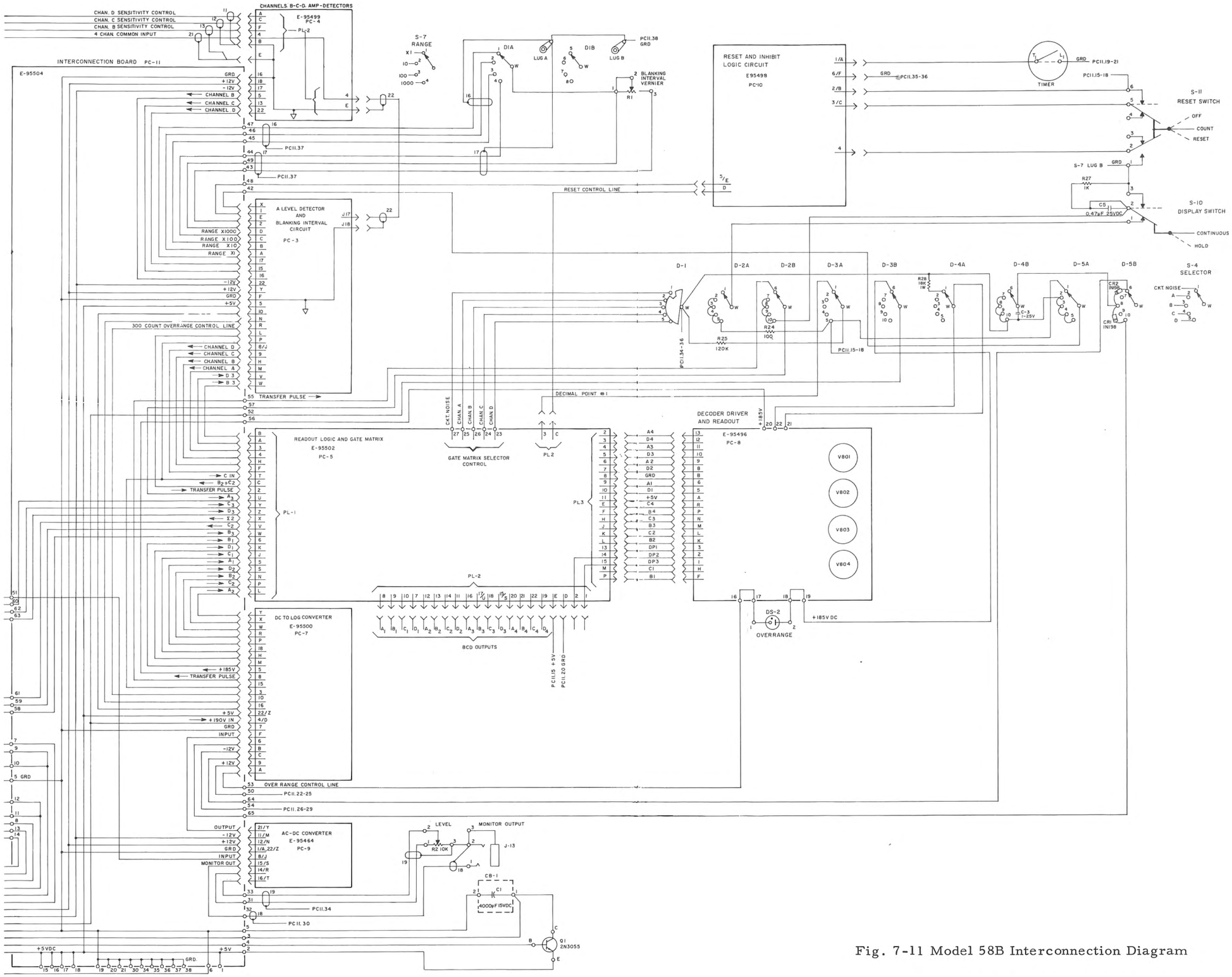


Fig. 7-11 Model 58B Interconnection Diagram