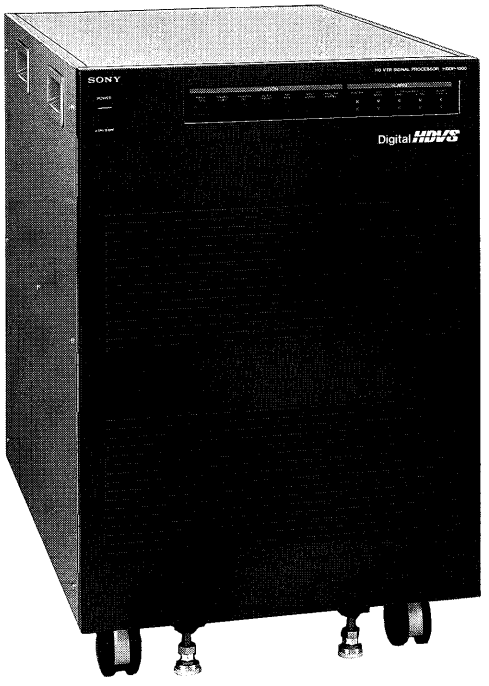
SONY

HD VTR SIGNAL PROCESSOR

HDDP-1000



Digital HDVS

MAINTENANCE MANUAL

Volume 1 1st Edition (Revised 3)

Serial No. 10001 and Higher

SAFETY CHECK-OUT

(Only for USA)

After correcting the original service problem, perform the following safety checks before releasing the set to the customer:

Check the metal trim, "metallized" knobs, screws, and all other exposed metal parts for AC leakage. Check leakage as described below.

LEAKAGE TEST

The AC leakage from any exposed metal part to earth ground and from all exposed metal parts to any exposed metal part having a return to chassis, must not exceed 3.5 mA. Leakage current can be measured by any one of three methods.

1. A commercial leakage tester, such as the Simpson 229 or RCA WT-540A. Follow the manufacturers' instructions to use these instruments.
2. A battery-operated AC milliammeter. The Data Precision 245 digital multimeter is suitable for this job.
3. Measuring the voltage drop across a resistor by means of a VOM or battery-operated AC voltmeter. The "limit" indication is 5.25V, so analog meters must have an accurate low-voltage scale. The Simpson 250 and Sanwa SH-63Trd are examples of a passive VOM that is suitable. Nearly all battery operated digital multimeters that have a 20V AC range are suitable. (See Fig. A)

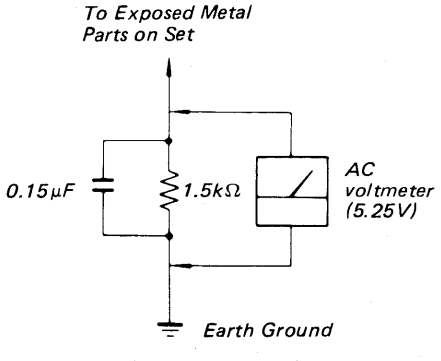


Fig. A. Using an AC voltmeter to check AC leakage.

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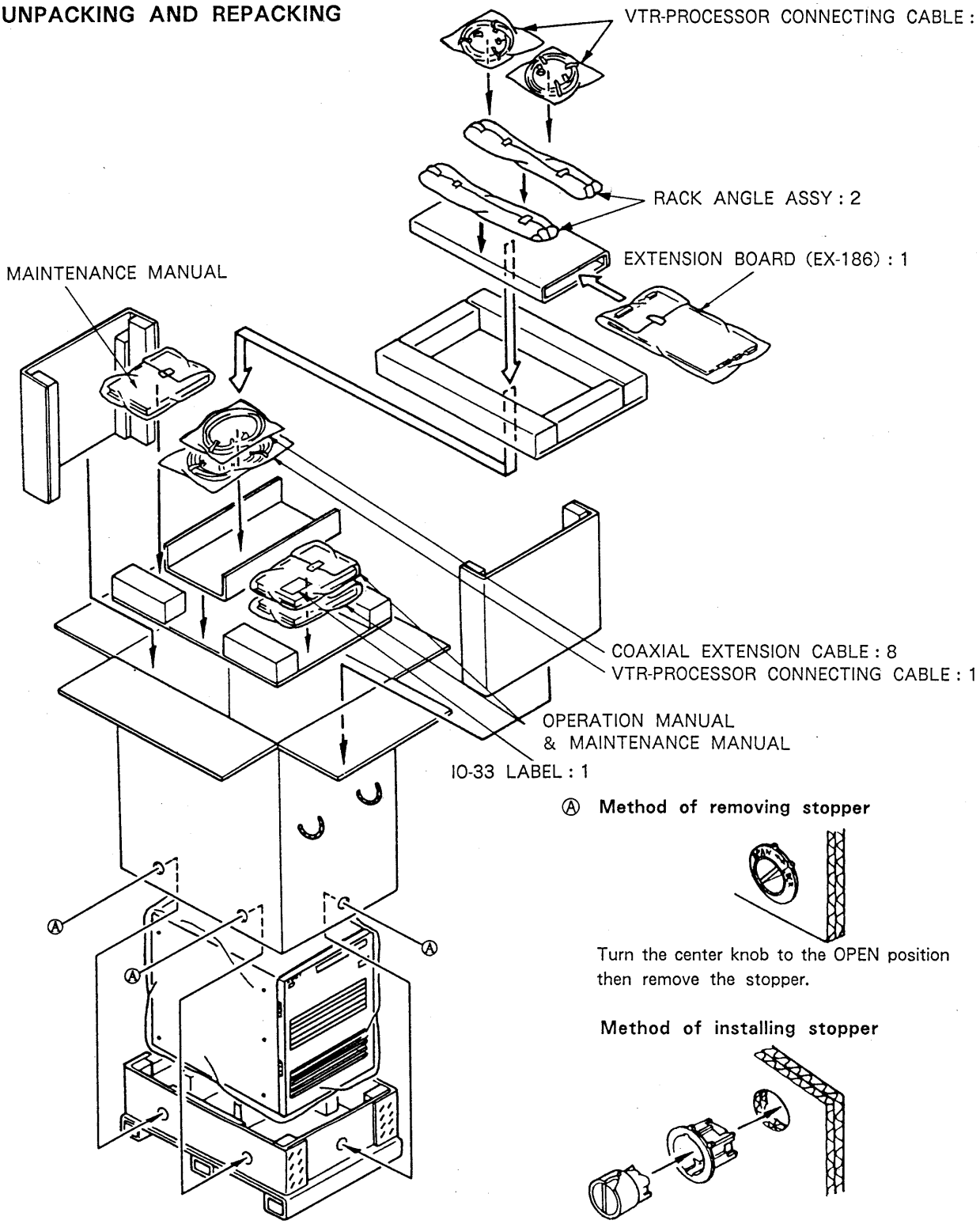
SECTION 1
INSTALLATION

1-1. UNPACKING AND REPACKING



Ⓐ **Method of removing stopper**

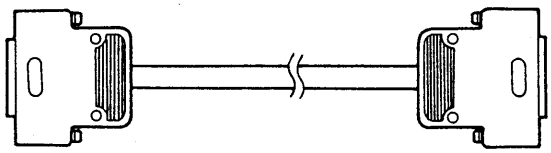
Turn the center knob to the OPEN position then remove the stopper.

Method of installing stopper

Hold the stopper with the OPEN protrusion facing directly upward, then insert it into the hole in the carton. Next, hold the center knob so that it is facing directly upward, then insert the stopper and turn it to the LOCK position.

1-2. ACCESSORIES

VTR-Processor Connecting Cable : 3
This cable is for connecting the HDDP-1000 to the HDD-1000.
D-Sub 50-pin, length 2m



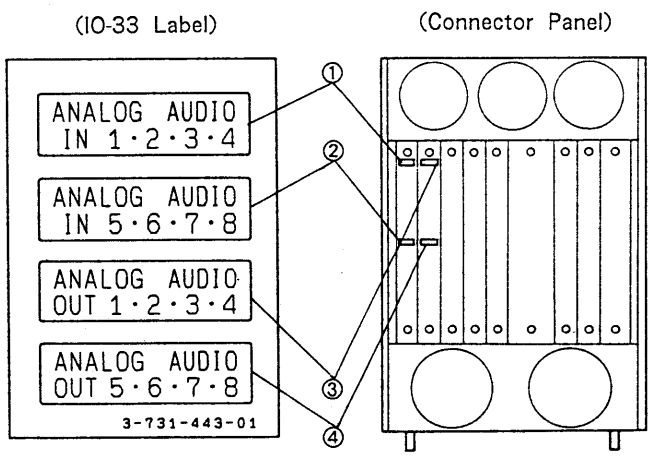
Rack Angle ASSY : 2
This is used for mounting the rack. See section 1-7 for rack mounting instructions.

Coaxial Extension Cable : 8
These are used for inspecting and servicing the printed circuit board (ADA-12 board).

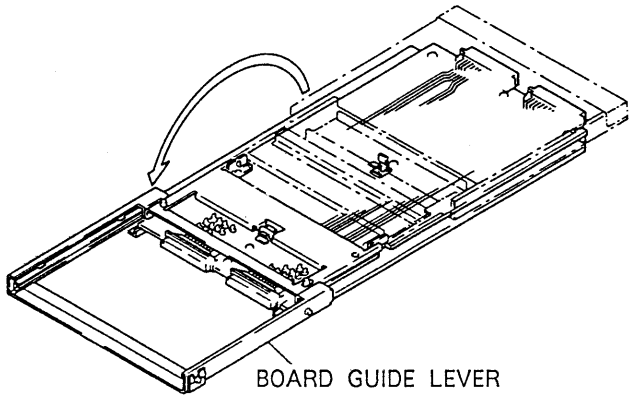
Operation Manual : 1
English version is provided with the USA/Canadian model.
English version, French version and German version are provided with the European model.

Maintenance Manual
Vol-1 and Vol-2 are provided with the unit.

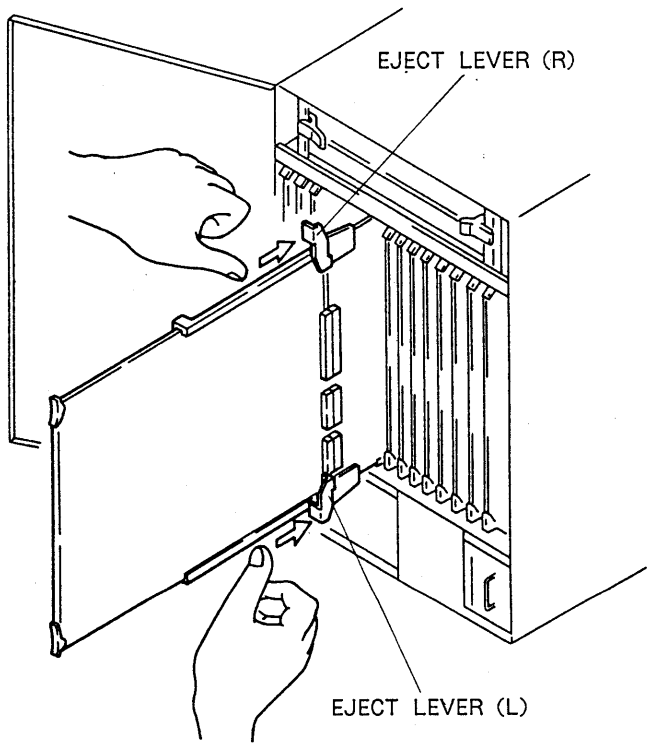
IO-33 Label : 1
Paste up the following labels of ① to ④ on the position of the ANALOG AUDIO IN/OUT connector panels shown below.



Extension Board (EX-186) : 1
This is used for inspecting and repairing plug-in circuit board in the card rack.
To use, tilt the board guide lower in the direction of the arrow.



Note : To remove a board mounted on an extension circuit board, press evenly on eject lever (R) and eject lever (L) and disengage the board.



1-3. POWER REQUIREMENTS

1-3-1. Capacity of AC Power Source

Power Line Voltage (switchable)
AC 100 to 120V±10% (for UC)
AC 220 to 240V±10% (for EK)
Power Line Frequency 50/60 Hz
Power Consumption 1100W max.

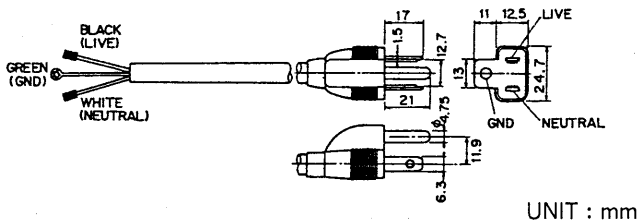
The supply voltage setting can be changed using the voltage selector switch on the front of the power supply unit. The above power is consumed during normal operation. When the unit is first switched on, however, a maximum surge current of between 14 and 16 A will flow. The AC supply must therefore be capable of supplying this surge current otherwise the power supply breaker on the AC supply side may trip, or the power supply inside the HDDP-1000 may not operate.

1-3-2. Power Cord

Length : Approx. 3m (For UC)
Length : Approx. 2.5m (For EK)

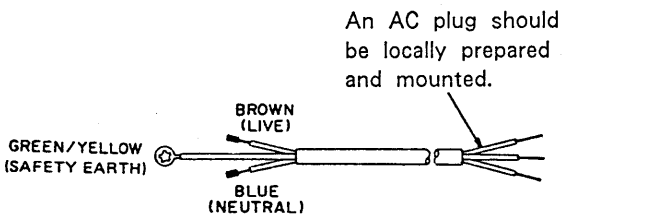
Plug configuration

For UC



UNIT : mm

For EK



UNIT : mm

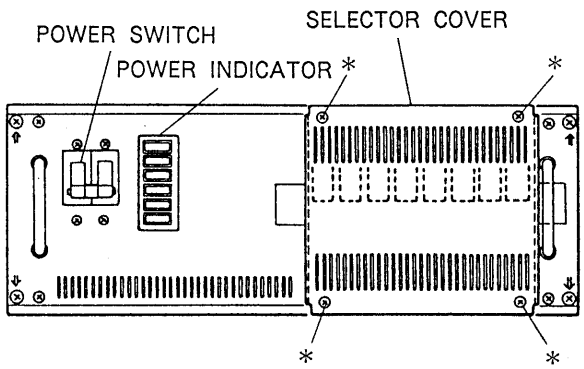
Note : Obtain an AC plug and install it on the end of the cable.

1-3-3. Voltage Selector Setting

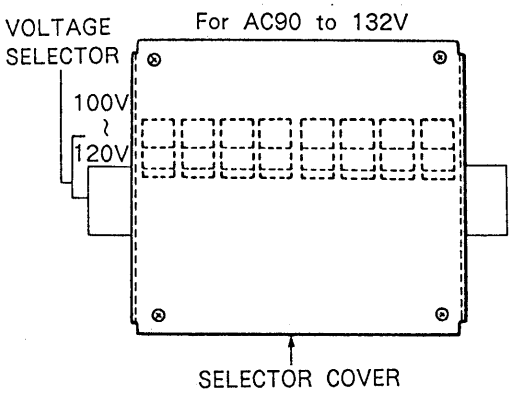
The voltage selector should be set the voltage of using area.
AC 90 to 132V ····· Set to "100−120V"
AC 198 to 264V ····· Set to "200−240V"
The setting of voltage can be changed according to necessity.

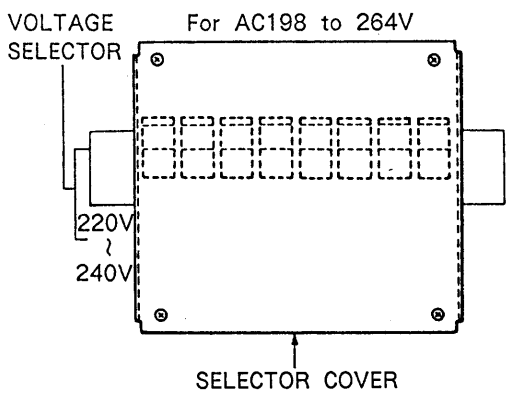
The select of voltage is as the following procedure.
① Remove the four screws (*) (B3×6) in the figure, and remove the selector cover.

<FRONT VIEW>



② Change the eight switches to requested voltage.
③ Install the selector cover so that the indication of its voltage may be seen.



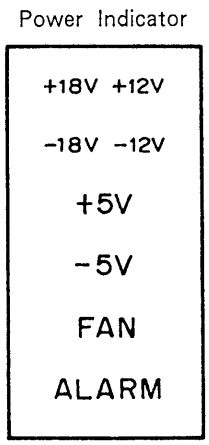


1-3-4. Ventilation and Heat Sink

The two fans which are located at the rear panel of the power unit, the fan which is located in the unit and the three fans which are located at the connector panel are used for air-cooling. Therefore, if either the intake or exhaust at the top, bottom, left or right side of the power unit should clog or the fans should stop, the power unit may be damaged. If the protective covers on the power unit are opened for maintenance or other activities, be sure not to operate the power unit for a long time without cooling.
If the temperature sensor in the power supply section of the unit operates, the buzzer in the power supply unit will sound and also the LED (ALARM) on the front panel of the power supply unit will flash. If the buzzer sounds, turn the power switch off immediately (within 10 seconds) and inspect the unit.

1-3-5. DC Output Indication

The DC output indication LEDs (Green) on the front panel of the power unit are lit when all DC voltage, i.e., +5V, −5V, +12V, −12V, +18V, −18V and Fan are output normally.



1-4. INSTALLATION CONDITIONS

Operating temperature : +10℃ to +35℃
Storage temperature : −20℃ to +60℃
Humidity : 10% to 85%
(no condensation)

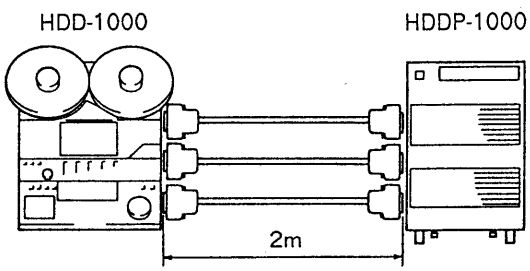
Notes for installation

1. The combined weight of the HDDP-1000 (approx. 100 kg) and HDD-1000 (approx. 70 kg) is approximately 170 kg.
2. The HDDP-1000 should be installed on a firm, level foundation and secured using the base panel adjuster screws.
3. Make sure that the exhaust fan does not become blocked in order to prevent internal overheating.
4. Do not install the unit in the following locations:
   - Exposed to direct sunlight or strong lights.
   - In a dusty location
   - Exposed to excessive vibrations
   - Exposed to strong electromagnetic fields
   - Exposed to high levels of electrical noise
   - Exposed to static electricity

1-5. HDDP-1000 AND HDD-1000 INSTALLATION

The HDDP-1000 and HDD-1000 should be placed no more than 2 meters apart and connected using VTR-processor connecting cables (three included with HDDP-1000).
Proper performance cannot be guaranteed if the HDDP-1000 and HDD-1000 are placed further apart than 2 meters. Use of the supplied VTR-processor connecting cables is therefore strongly recommended. When using the units by putting the HDD-1000 on the HDDP-1000, be careful not to be fallen in the earthquake or the movement of the unit.

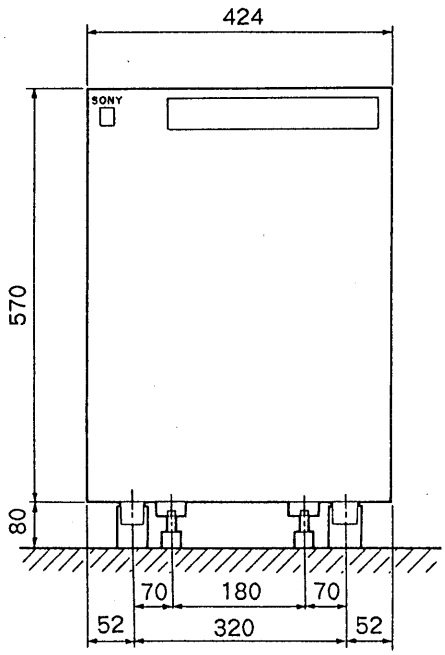
VTR-processor connecting cable : 2m



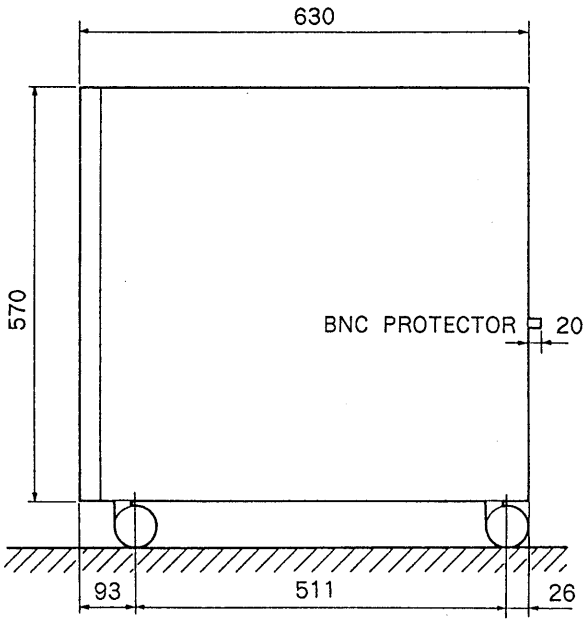
1-6. INSTALLATION SPACE

External Dimensions

<FRONT VIEW>



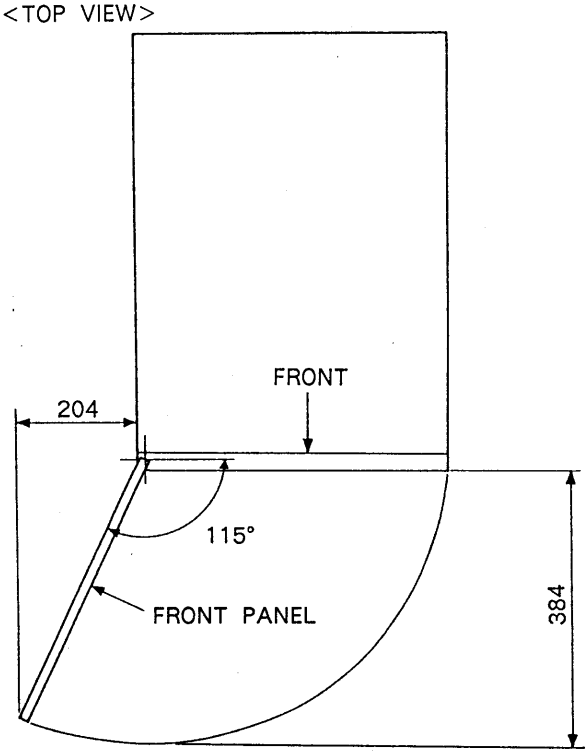
<SIDE VIEW>



UNIT : mm

Working Space : when opening Front panel

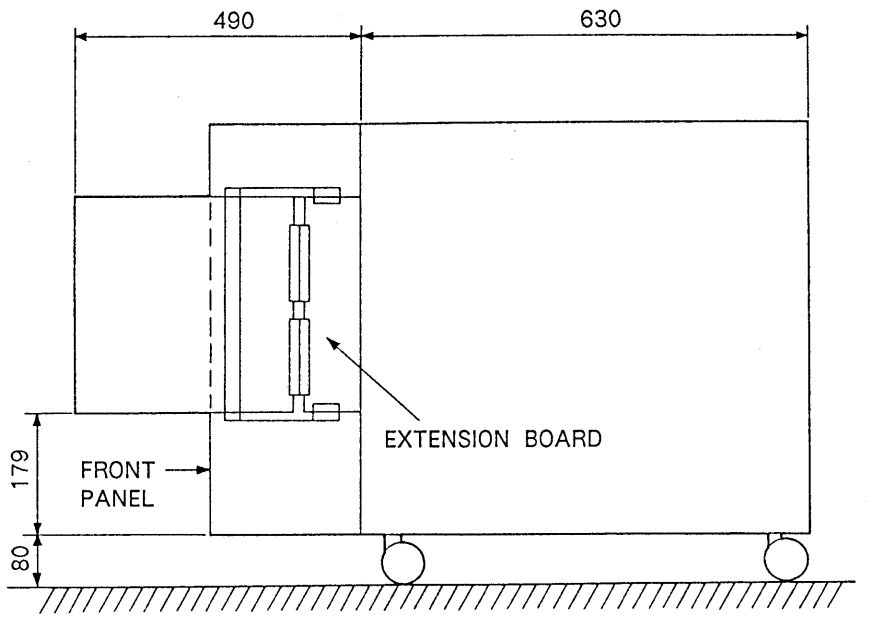
<TOP VIEW>



UNIT : mm

Working Space : when using Extension board

<SIDE VIEW>

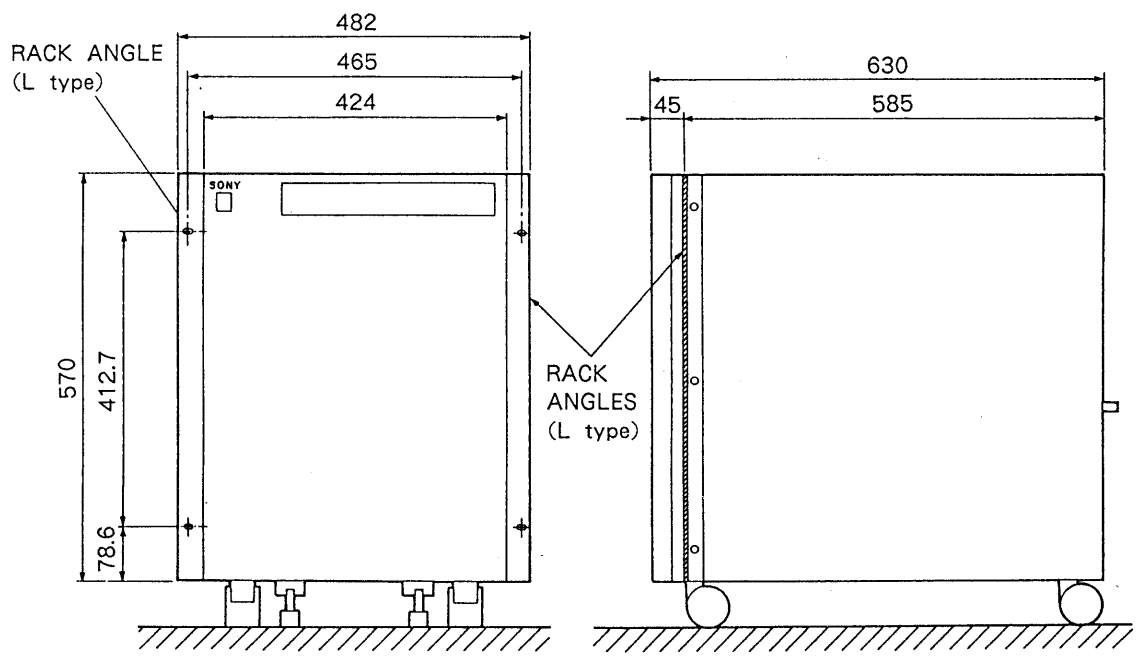


UNIT : mm

Working Space : when rack-mounting

<FRONT VIEW>

<SIDE VIEW>



UNIT : mm

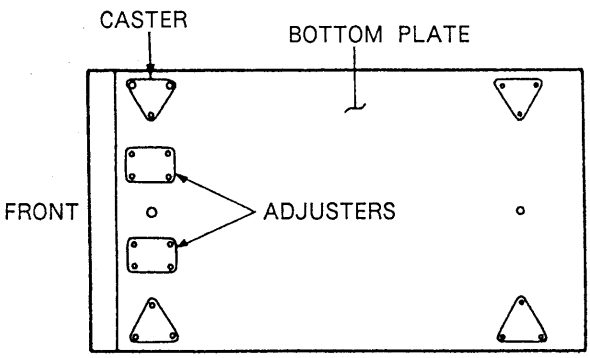
1-7. RACK MOUNTING

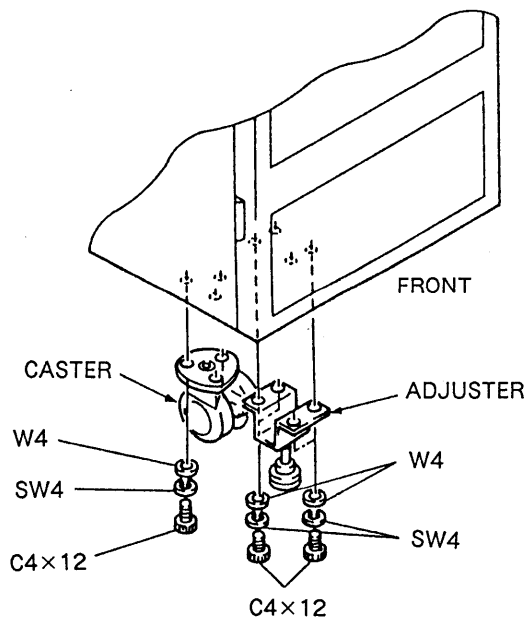
Prepare the following parts for rack-mounting.

Rack Angle : 1 pair
HDDP-1000 is equipped with 1 pair.
Support Angle : 1 pair
Be sure to use the parts recommended by the rack maker.
Screws and Nuts
To install the rack angle, remove the screws from the HDDP-1000 and reuse them.
To install the other mounting parts, use the screws and nuts recommended by the rack maker.

1. Remove the four casters and two adjusters, as shown in the figure. Fix the bottom plate using the screws which install the casters. (It is not necessary to tighten the adjuster screws.)
   Note : It is possible to rack-mount installing the casters and adjusters, however, remove them from necessity.

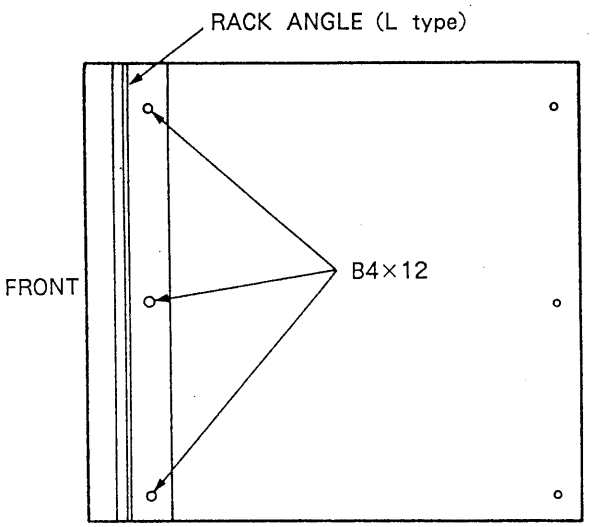
<BOTTOM VIEW>





2. Install the rack angles using the six screws (B4×12) which install the right and left side panels.

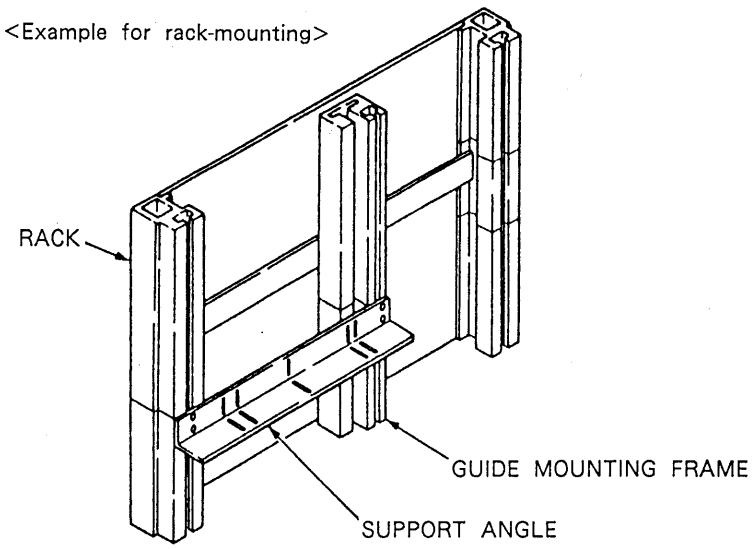
<SIDE VIEW>



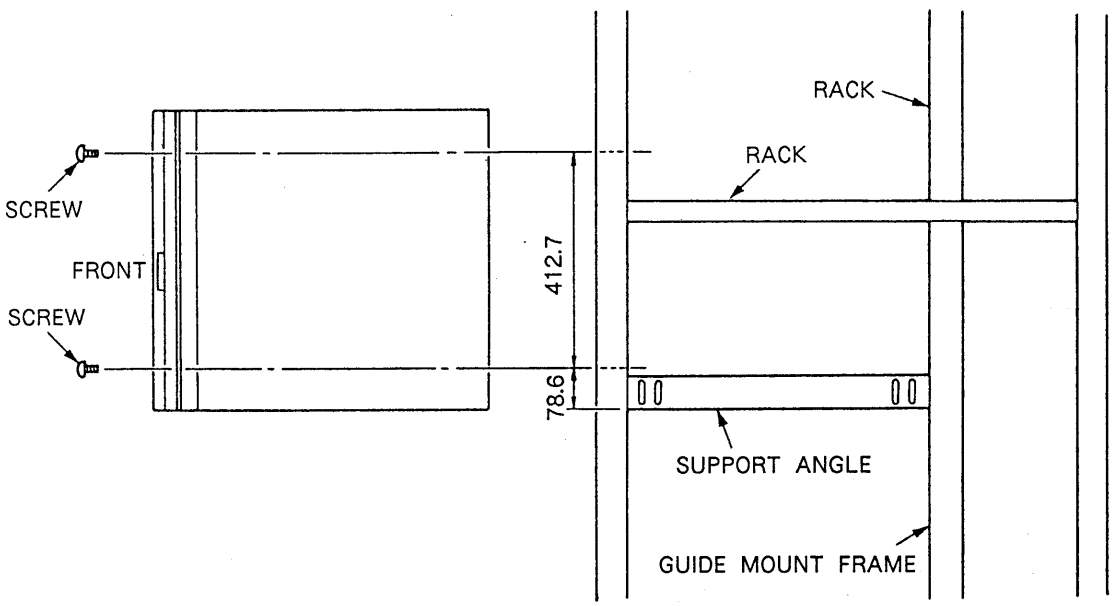
3. Install the support angle.

Note : Use the support angle, screws and nuts recommended by the rack maker. Depending on the rack used, a dedicated bracket and guide mounting frame may also be required. For details, consult with the rack maker. Also, the support angle used must be capable of adequately supporting the HDDP - 1000 (approx. 100 kg). The installation example shown in the figure below is for reference only. Depending upon the particular rack, the actual mounting may sometimes differ from the example.

<Example for rack-mounting>



4. Mount the HDDP-1000 on the rack



UNIT : mm

1-8. INPUT/OUTPUT INTERFACE

1-8-1. Matching Connectors and Cables

HDDP-1000 connectors		Matching Connectors/Cables	
Used for	Name	Name	Sony Part No.
VIDEO IN G/Y, B/P_B, R/P_R, SYNC	BNC	BNC	
VIDEO OUT-1 G/Y, B/P_B, R/P_R, SYNC	BNC	BNC	
VIDEO OUT-2 G/Y, B/P_B, R/P_R, SYNC	BNC	BNC	
WFM OUT G/Y, B/P_B, R/P_R, SYNC	BNC	BNC	
MONITOR OUT G/Y, B/P_B, R/P_R, SYNC	BNC	BNC	
DIGITAL VIDEO IN	D-Sub, 50P, Female	DIGITAL VIDEO CABLE	Optional Accessory (Note1)
DIGITAL VIDEO OUT	D-Sub, 50P, Female		
DIGITAL AUDIO PARALLEL IN	D-Sub, 15P, Female	DIGITAL AUDIO CABLE	Optional Accessory (Note2)
DIGITAL AUDIO PARALLEL OUT	D-Sub, 15P, Female		
DIGITAL AUDIO IN CH-1/2, CH-3/4, CH-5/6, CH-7/8	XLR, 3P, Female	XLR, 3P, Male	1-508-084-00 (Note3)
DIGITAL AUDIO OUT CH-1/2, CH-3/4, CH-5/6, CH-7/8	XLR, 3P, Male	XLR, 3P, Female	1-508-083-00 (Note4)
ANALOG AUDIO IN CH-1/5, CH-2/6, CH-3/7, CH-4/8	XLR, 3P, Female	XLR, 3P, Male	1-508-084-00 (Note3)
ANALOG AUDIO OUT CH-1/5, CH-2/6, CH-3/7, CH-4/8	XLR, 3P, Male	XLR, 3P, Female	1-508-083-00 (Note4)
RS-232C	D-Sub, 25P, Female	D-Sub, 25P, Male	
TO VTR CN-1	D-Sub, 50P, Female	VTR-Processor Connecting Cable	1-574-997-11 (Note5)
CN-2/3	D-Sub, 50P, Male		

(**Note 1**) DIGITAL VIDEO CABLE
This is used to input/output the digital video signal.

(**Note 2**) DIGITAL AUDIO CABLE
This is used to input/output the digital audio signal.
ECD-3C=3m
ECD-10C=10m
ECD-30C=30m

(**Note 3**) XLR 3-pin Female connector
Equivalent to CANNON XLR-3-11C.

(**Note 4**) XLR 3-pin Male connector
Equivalent to CANNON XLR-3-12C.

(**Note 5**) VTR-Processor Connecting Cable
Used for connecting the HDDP-1000 to the VTR HDD-1000. The length is 2m. Supplied three cables with the HDDP-1000.

1-8-2. Input/Output Signal of the Connectors

① VIDEO

VIDEO IN (Analog)

G/Y, B/P_B, R/P_R ; 1.0 Vp-p±2 dB

SYNC ; ±0.3V±3 dB

75 Ω, G/B/R or Y/P_B/P_R selectable

VIDEO OUT-1/2

G/Y, B/P_B, R/P_R ;

0.7 Vp-p (video), ±0.3V (sync)

SYNC ; ±0.3V

75 Ω, G/B/R or Y/P_B/P_R selectable

WFM OUT

G/Y, B/P_B, R/P_R ;

0.7 Vp-p (video), ±0.3V (sync), 75 Ω

SYNC ; ±0.3V (input/output video), 75 Ω

0.6 Vp-p (CTL), 75 Ω

0.4 Vp-p (RF envelope), 75 Ω

Either one of the values is selected in the HDD-1000 and HDDP-1000, and output.

Either CTL or RF envelope is selected in the HDD-1000, and input into the HDDP-1000.

MONITOR OUT

G/Y, B/P_B, R/P_R ;

0.7 Vp-p (video), ±0.3V (sync)

SYNC ; ±0.3V

② AUDIO

DIGITAL AUDIO IN (CH-1/2, CH-3/4, CH-5/6, CH-7/8) ;

ANALOG AUDIO IN (CH-1/2, CH-3/4, CH-5/6, CH-7/8) ;

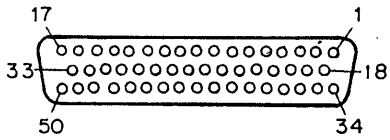
−16 dBm to +10 dBm, reference level +4 dBm 600 Ω/high impedance (more than 10k Ω) selectable, balanced

DIGITAL AUDIO OUT (CH-1/2, CH-3/4, CH-5/6, CH-7/8) ;

ANALOG AUDIO OUT (CH-1/2, CH-3/4, CH-5/6, CH-7/8) ;

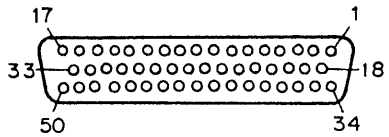
+4 dBm nominal, 600 Ω, balanced

③ DIGITAL VIDEO IN Connector



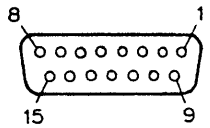
Pin No.	Signal	Remarks
1	IDCK+	74.25 MHz clock ; Differential in ECL level
34	IDCK−	
2	IYD7+	Digital Y signal data ; Differential in ECL level
35	IYD7−	
3	IYD6+	
36	IYD6−	
4	IYD5+	
37	IYD5−	
5	IYD4+	
38	IYD4−	
6	IYD3+	
39	IYD3−	
7	IYD2+	
40	IYD2−	
8	IYD1+	
41	IYD1−	
9	IYD0+	
42	IYD0−	
10	ICD7+	Digital chroma signal data ; Differential in ECL level
43	ICD7−	
11	ICD6+	
44	ICD6−	
12	ICD5+	
45	ICD5−	
13	ICD4+	
46	ICD4−	
14	ICD3+	
47	ICD3−	
15	ICD2+	
48	ICD2−	
16	ICD1+	
49	ICD1−	
17	ICD0+	
50	ICD0−	
18	GND	
19	GND	
20	GND	
21	GND	
22	GND	
23	GND	
24	GND	
25	GND	
26	GND	
27	GND	
28	GND	
29	GND	
30	GND	
31	GND	
32	GND	
33	GND	

④ DIGITAL VIDEO OUT Connector



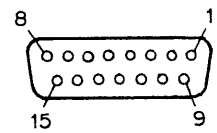
Pin No.	Signal	Remarks
1	ODCK+	74.25 MHz clock ; Differential out ECL level
34	ODCK−	
2	OYD7+	Digital Y signal data ; Differential out ECL level
35	OYD7−	
3	OYD6+	
36	OYD6−	
4	OYD5+	
37	OYD5−	
5	OYD4+	
38	OYD4−	
6	OYD3+	
39	OYD3−	
7	OYD2+	
40	OYD2−	
8	OYD1+	
41	OYD1−	
9	OYD0+	
42	OYD0−	
10	OCD7+	Digital chroma signal data ; Differential out, ECL level
43	OCD7−	
11	OCD6+	
44	OCD6−	
12	OCD5+	
45	OCD5−	
13	OCD4+	
46	OCD4−	
14	OCD3+	
47	OCD3−	
15	OCD2+	
48	OCD2−	
16	OCD1+	
49	OCD1−	
17	OCD0+	
50	OCD0−	
18	GND	
19	GND	
20	GND	
21	GND	
22	GND	
23	GND	
24	GND	
25	GND	
26	GND	
27	GND	
28	GND	
29	GND	
30	GND	
31	GND	
32	GND	
33	GND	

⑤ DIGITAL AUDIO PARALLEL IN Connector
Conforms to the AES/EBU format



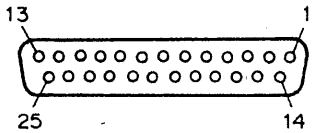
Pin No.	Signal	Remarks
1	FRAME GND	
2	I/O IN 1 (X)	Digital audio CH-1/2 data in RS422A level
3	I/O IN 1 (Y)	
4	I/O IN 1 (G)	
5	NC	
6	I/O IN 2 (X)	Digital audio CH-3/4 data in RS422A level
7	I/O IN 2 (Y)	
8	I/O IN 2 (G)	
9	I/O IN 3 (X)	Digital audio CH-5/6 data in RS422A level
10	I/O IN 3 (Y)	
11	I/O IN 3 (G)	
12	NC	
13	I/O IN 4 (X)	Digital audio CH-7/8 data in RS422A level
14	I/O IN 4 (Y)	
15	I/O IN 4 (G)	

⑥ DIGITAL AUDIO PARALLEL OUT Connector
Conforms to the AES/EBU format



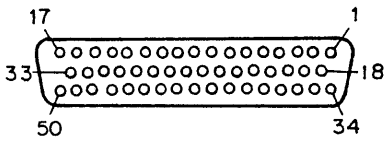
Pin No.	Signal	Remarks
1	FRAME GND	
2	I/O OUT 1 (X)	Digital audio CH-1/2 data out RS422A level
3	I/O OUT 1 (Y)	
4	I/O OUT 1 (G)	
5	NC	
6	I/O OUT 2 (X)	Digital audio CH-3/4 data out RS422A level
7	I/O OUT 2 (Y)	
8	I/O OUT 2 (G)	
9	I/O OUT 3 (X)	Digital audio CH-5/6 data out RS422A level
10	I/O OUT 3 (Y)	
11	I/O OUT 3 (G)	
12	NC	
13	I/O OUT 4 (X)	Digital audio CH-7/8 data out RS422A level
14	I/O OUT 4 (Y)	
15	I/O OUT 4 (G)	

⑦ RS-232C Connector



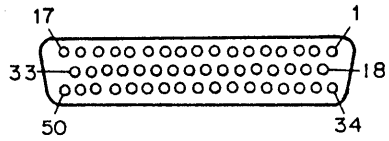
Pin No.	Signal	Remarks
1	GND	
2	RXB 232C	Data in, RS232 level
3	TXB 232C	Data out, RS232 level
4	CTSB	Control in, RS232 level
5	RTSB	Control out, RS232 level
6	NC	
7	GND	
8	NC	
9	NC	
10	NC	
11	NC	
12	NC	
13	NC	
14	NC	
15	NC	
16	NC	
17	NC	
18	NC	
19	NC	
20	NC	
21	NC	
22	NC	
23	NC	
24	NC	
25	NC	

⑧ TO VTR Connector (CN-1 : AUDIO IN/OUT)



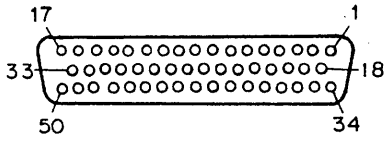
Pin No.	Signal	Remarks
1	NC	
34	NC	
2	MONI R1 (X)	Analog audio monitor data (R) out −2 dBs
18	MONI R1 (G)	
35	MONI R1 (Y)	
3	MONI L1 (X)	Analog audio monitor data (L) out −2 dBs
19	MONI L1 (G)	
36	MONI L1 (Y)	
4	TR8 DATA (+)	Audio CH-8 PB data in RS422A level
37	TR8 DATA (−)	
5	TR7 DATA (+)	Audio CH-7 PB data in RS422A level
38	TR7 DATA (−)	
6	TR6 DATA (+)	Audio CH-6 PB data in RS422A level
39	TR6 DATA (−)	
7	TR5 DATA (+)	Audio CH-5 PB data in RS422A level
40	TR5 DATA (−)	
8	TR4 DATA (+)	Audio CH-4 PB data in RS422A level
41	TR4 DATA (−)	
9	TR3 DATA (+)	Audio CH-3 PB data in RS422A level
42	TR3 DATA (−)	
10	TR2 DATA (+)	Audio CH-2 PB data in RS422A level
43	TR2 DATA (−)	
11	TR1 DATA (+)	Audio CH-1 PB data in RS422A level
44	TR1 DATA (−)	
12	REC EN LCK (+)	Clock for REC amplifier out RS422A level
45	REC EN LCK (−)	
13	REC EN (+)	CH-1 to CH-8 audio REC EN signal out, RS422A level
46	REC EN (−)	
14	LCK (+)	Clock to latch audio REC data out RS422A level
47	LCK (−)	
15	BCK (+)	Clock to shift audio REC data out RS422A level
48	BCK (−)	
16	DATA 2 (+)	Audio CH-5 to CH-8 REC data out RS422A level
49	DATA 2 (−)	
17	DATA 1 (+)	Audio CH-1 to CH-4 REC data out RS422A level
50	DATA 1 (−)	
20	F GND	
21	F GND	
22	F GND	
23	F GND	
24	F GND	
25	F GND	
26	F GND	
27	F GND	
28	F GND	
29	F GND	
30	F GND	
31	F GND	
32	F GND	
33	F GND	

⑨ TO VTR Connector (CN-2 : VIDEO IN/OUT)



Pin No.	Signal	Remarks
1	CPU V (−)	Communication timing reference in RS422A level
34	CPU V (+)	
2	MIX OUT (X)	Digital audio mix signal for CUE channel REC −2 dBs
18	MIX OUT (G)	
35	MIX OUT (Y)	
3	WFM IN (X)	CTL/RF envelope signal (Refer to Menu S03) 0.3 Vp-p to 0.8 Vp-p
19	WFM IN (G)	
36	WFM IN (Y)	
12	R CK (+)	Clock for REC video data out ECL level
45	R CK (−)	
4	R DATA-1 (+)	Video CH-1 REC data out ECL level
37	R DATA-1 (−)	
5	R DATA-2 (+)	Video CH-2 REC data out ECL level
38	R DATA-2 (−)	
6	R DATA-3 (+)	Video CH-3 REC data out ECL level
39	R DATA-3 (−)	
7	R DATA-4 (+)	Video CH-4 REC data out ECL level
40	R DATA-4 (−)	
8	R DATA-5 (+)	Video CH-5 REC data out ECL level
41	R DATA-5 (−)	
9	R DATA-6 (+)	Video CH-6 REC data out ECL level
42	R DATA-6 (−)	
10	R DATA-7 (+)	Video CH-7 REC data out ECL level
43	R DATA-7 (−)	
11	R DATA-8 (+)	Video CH-8 REC data out ECL level
44	R DATA-8 (−)	
13	CHARA GATE (+)	Blanking signal for character insertion RS422A level
46	CHARA GATE (−)	
14	CHARA SIG (+)	Character data in RS422A level
47	CHARA SIG (−)	
15	REF SYNC OUT (+)	Servo reference signal out RS422A level
48	REF SYNC OUT (−)	
16	RS-422 OUT (+)	Proc.-to-VTR communication data RS422A level
49	RS-422 OUT (−)	
17	RS-422 IN (+)	VTR-to-Proc. communicaion data RS422A level
50	RS-422 IN (−)	
20	GND	
21	GND	
22	GND	
23	GND	
24	GND	
25	GND	
26	GND	
27	GND	
28	GND	
29	GND	
30	GND	
31	GND	
32	GND	
33	GND	

⑩ TO VTR Connector (CN-3 : VIDEO IN)



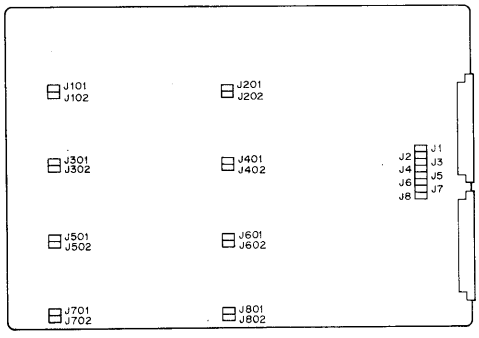
Pin No.	Signal	Remarks
1	NC	
34	NC	
2	RTN DATA-1 (+)	Video CH-1 PB data in ECL level
35	RTN DATA-1 (−)	
4	RTN DATA-2 (+)	Video CH-2 PB data in ECL level
37	RTN DATA-2 (−)	
6	RTN DATA-3 (+)	Video CH-3 PB data in ECL level
39	RTN DATA-3 (−)	
8	RTN DATA-4 (+)	Video CH-4 PB data in ECL level
41	RTN DATA-4 (−)	
10	RTN DATA-5 (+)	Video CH-5 PB data in ECL level
43	RTN DATA-5 (−)	
12	RTN DATA-6 (+)	Video CH-6 PB data in ECL level
45	RTN DATA-6 (−)	
14	RTN DATA-7 (+)	Video CH-7 PB data in ECL level
47	RTN DATA-7 (−)	
16	RTN DATA-8 (+)	Video CH-8 PB data in ECL level
49	RTN DATA-8 (−)	
3	RTN CK-1 (+)	Clock CH-1 PB data in ECL level
36	RTN CK-1 (−)	
5	RTN CK-2 (+)	Clock CH-2 PB data in ECL level
38	RTN CK-2 (−)	
7	RTN CK-3 (+)	Clock CH-3 PB data in ECL level
40	RTN CK-3 (−)	
9	RTN CK-4 (+)	Clock CH-4 PB data in ECL level
42	RTN CK-4 (−)	
11	RTN CK-5 (+)	Clock CH-5 PB data in ECL level
44	RTN CK-5 (−)	
13	RTN CK-6 (+)	Clock CH-6 PB data in ECL level
46	RTN CK-6 (−)	
15	RTN CK-7 (+)	Clock CH-7 PB data in ECL level
48	RTN CK-7 (−)	
17	RTN CK-8 (+)	Clock CH-8 PB data in ECL level
50	RTN CK-8 (−)	
18	GND	
19	GND	
20	GND	
21	GND	
22	GND	
23	GND	
24	GND	
25	GND	
26	GND	
27	GND	
28	GND	
29	GND	
30	GND	
31	GND	
32	GND	
33	GND	

1-9. SWITCH/JUMPER SETTINGS

1-9-1. Changing the Input Impedance of Analog Audio

AD-38 Board

Component Side



J101/102 : CH-1 analog audio input impedance select jumper
J201/202 : CH-2 analog audio input impedance select jumper
J301/302 : CH-3 analog audio input impedance select jumper
J401/402 : CH-4 analog audio input impedance select jumper
J501/502 : CH-5 analog audio input impedance select jumper
J601/602 : CH-6 analog audio input impedance select jumper
J701/702 : CH-7 analog audio input impedance select jumper
J801/802 : CH-8 analog audio input impedance select jumper

The input impedance is set to 600 Ω, when shipped. However, the AD-38 board changed as shown on the table right makes high impedance (more than 10 kΩ) possible.
The sockets for inserting onto J101 to J802 are able to insert onto the spaces of J1 to J8 in order not to be lost.

Channel	Jumper	600 Ω (When shipped)	High impedance
CH-1	J101	SHORT	OPEN
	J102	OPEN	OPEN
CH-2	J201	SHORT	OPEN
	J202	OPEN	OPEN
CH-3	J301	SHORT	OPEN
	J302	OPEN	OPEN
CH-4	J401	SHORT	OPEN
	J402	OPEN	OPEN
CH-5	J501	SHORT	OPEN
	J502	OPEN	OPEN
CH-6	J601	SHORT	OPEN
	J602	OPEN	OPEN
CH-7	J701	SHORT	OPEN
	J702	OPEN	OPEN
CH-8	J801	SHORT	OPEN
	J802	OPEN	OPEN

1-9-2. Switches, Jumpers and Indicators on Boards

The boards which have the switch, jumper and indicator are listed below.

System	Slot. No.	Board	Circuit function
VIDEO	1	PS-183	PARALLEL/SERIAL CONVERTER
	2	CF-39	CONCEAL FILTER
	3 to 6	VD-04	VIDEO DECODER
	7	CI-05	CHANNEL INTERCHANGER
	8	TB-07	TIME BASE CORRECTOR
	9, 10	VE-18	VIDEO ENCODER
	11	SP-06	SERIAL/PARALLEL CONVERTER
	12	SG-151 (&SW-334)	SYNC GENERATOR
		ADA-12	VIDEO A/D, D/A CONVERTER
AUDIO	13	DEC-41	AUDIO DECODER/ENCODER
	14	PR-115	AUDIO PROCESSOR & SYSTEM CONTROLLER
	15	DA-28	AUDIO D/A CONVERTER
	16	AD-38	AUDIO A/D CONVERTER

Note 1 : Set the video system boards mode select switch (S7-7/PR-115 ; normally set to OFF) to ON, when using the switches on the PS-183, CF-39, VD-04, VE-18 and SP-06 boards.

Note 2 : Set the video system boards mode select switch (S7-7/PR-115 : normally set to OFF) and the CI-05 board mode select switch (S7-8/PR-115 : normally set to OFF) to ON, or the TEST ON/OFF switch (S2-8/CI-05 : normally set to OFF) to ON, when using the switches on the CI-05 board.

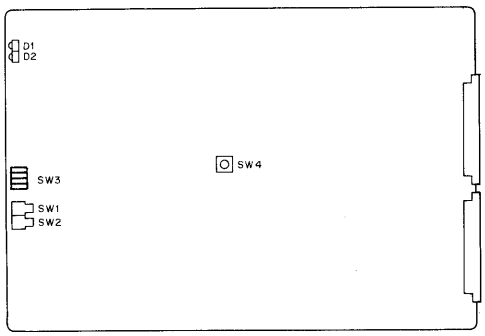
Note 3 : Set the TEST ON/OFF switch (S3-8/SG-151 : normally set to OFF) to ON, when using the switches on the SG-151 board.

Note 4 : Set the LOCAL/REMOTE select switch (S1-8/ADA-12 : normally set to OFF) to ON, when using the switches on the ADA-12 board.

PS-183 Board

(Slot No.1 : PARALLEL/SERIAL CONVERTER)

Component Side



D1 : ALARM indicator (red)
Lights if an error occurs on the PS-183 board.

D2 : LOCAL indicator (green)
When this indicator lights, the switches on the PS-183 board are enabled. It lights under the following conditions.

1. When the video system boards mode select switch (S7-7/PR-115) is set to ON
2. When only the power of the processor is turned ON, while the powers both the VTR and the processor are OFF
3. When the PR-115 board is not inserted

SW1, SW2 : VIDEO PHASE adjusting switch
Used for adjusting the phase of the analog video output. The adjustable range is from −32 samples to +31 samples (−431 nsec to +417.5 nsec, approximately 13.5 nsec per 1 sample.)
When the video system boards mode setting switch (S7-7/PR-115 : normally set to OFF) is set to ON, these switches are enabled.
The switch position and the phase are shown on the next page.
The + sample means that the phase of the analog video output delays, the − sample means that the phase advances.
When shipped, both SW1 and SW2 are set to 0.

Switch				Phase
SW1	SW2	or	SW1 SW2	
C	0		4 0	−32 Samples (−431 nsec)
C	1		4 1	
–	–		– –	
D	E		5 E	
D	F		5 F	
E	0		6 0	
E	1		6 1	−31 Samples (−417.5 nsec)
E	2		6 2	−30 Samples (−404 nsec)
–	–		– –	
F	E		7 E	−2 Samples (−27 nsec)
F	F		7 F	−1 Sample (−13.5 nsec)
0	0		8 0	0 Sample (0 nsec)
0	1		8 1	+1 Sample (+13.5 nsec)
0	2		8 2	+2 Samples (+27 nsec)
–	–		– –	
1	D		9 D	+29 Samples (+390.5 nsec)
1	E		9 E	+30 Samples (+404 nsec)
1	F		9 F	+31 Samples (+417.5 nsec)
2	0		A 0	
2	1		A 1	
–	–		– –	
3	E		B E	
3	F		B F	

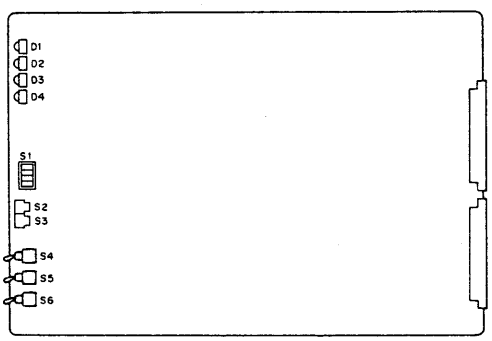
SW3-1 : User data digital out ON/OFF switch
Enables to output the user data (digital data) in the V blanking via the DIGITAL VIDEO OUT connector. When the video system boards mode select switch (S7-7/PR-115 : normally set to OFF) is set to ON, this switch is enabled.
ON : The digital signal is output.
OFF : The digital signal is not output.
Set to OFF when shipped.

SW3-2 to SW3-4 : Not used.

SW4 : PB Y/C DELAY adjusting switch
This switch compensates the delay which is caused by the filter of the ADA-12 board.
When turning this switch clockwise by one step, the Y signal delays by 13.5 nsec. When turning counterclockwise, the chroma signal (P_B, P_R) delays. Never turn this switch because it has been adjusted for the filter on the ADA-12 board at factory.

CF-39 Board (Slot No.2 : CONCEAL FILTER)

Component Side



D1 : ALARM indicator (red)
Lights if an error occurs on the CF-39 board.

D2 : LOCAL indicator (green)
When this indicator lights, the switches on the CF-39 board are enabled. It lights under the following conditions.
1. When the video system boards mode select switch (S7-7/PR-115) is set to ON
2. When only the power of the processor is turned ON, while the powers both the VTR and the processor are OFF
3. When the PR-115 board is not inserted

D3 : CONCEAL (concealment) indicator (green)
Lights when the conceal circuit operates. Refer to the description of the CONCEAL switch (S5) on the CF-39 board.

D4 : FLAG (error flag) indicator (yellow)
Lights when the video signal which is converted to the error flags is output from the DIGITAL/ANALOG VIDEO OUT connectors and the MONITOR OUT connector. Refer to the description of the FLAG switch (S6) on the CF-39 board.

S1-1 : CHANNEL DE-INTERLEAVE OFF switch
Be sure to set this switch to the same position as that of the CHANNEL INTERLEAVE OFF switch (S4-1/SP-06 : normally set to OFF).
If not, the signals are not processed correctly.
When both of those switches are set to ON, the Y signal and the chroma (P_B, P_R) signal are mixed at the channel interleave circuit on the SP-06 board and then the Y signal and the chroma (P_B, P_R) signal are separated at the channel de-interleave circuit on the CF-39 board.
When both of them are set to OFF, the Y signal and the chroma (P_B, P_R) signal are not mixed and the separated signals are processed.
When the video system boards mode select switch (S7-7/PR-115 : normally set to OFF) is set to ON, this switch is enabled.
Set to OFF when shipped.

S1-2 to S1-4 : Not used.

S2 : CHANNEL SHIFT switch
This switch makes the channel of the 8-channel playback video data shift.
Used to find and/or check the channel in which an error occurs.
When the video system boards mode select switch (S7-7/PR-115 : normally set to OFF) and the CHANNEL DE-INTERLEAVE OFF switch (S1-1 : normally set to OFF) are set to ON, this switch is enabled.

S2	Channel shift
0 or 8	0
1 or 9	1
2 or A	2
3 or B	3
4 or C	4
5 or D	5
6 or E	6
7 or F	7

EX. When S2 is set to 4 or C, all channels are shifted by 4 channels.
Set to 0 when shipped.

S3 : FLAG M-SEL (error flag monitor select) switch
Selects the error flag on which channel (video head) is mixed to the video signal, when the video signal is output with the error flag from the MONITOR OUT connector.
When the HDD-1000 Menu T11. ERR FLAG DISP (MONI) is set to ON, or both the LOCAL/REMOTE select switch (S1-8/ADA-12 : normally set to OFF) and the DISPLAY control switch (S1-3/ADA-12 : normally set to OFF) are set to ON, this switch is enabled.

The setting of S3 and the selected channel (video head) are as follows.

S3	Video head
0	CH-1 to CH-8
1	CH-1
2	CH-2
3	CH-3
4	CH-4
5	CH-5
6	CH-6
7	CH-7
8	CH-8
9, A to F	CH-1 to CH-8

Set to 0 when shipped.

S4 : ERROR CORRECT (error correction circuits) switch
Used to operate the inner correction and outer correction circuits. When the video system boards mode select switch (S7-7/PR-115 : normally set to OFF) is set to ON, this switch is enabled.
ECC2 : The inner correction circuit and outer correction circuit operate. Normally, select this setting.
ECC1 : The inner correction circuit operates. The outer correction circuit does not operate, and detects an error.
OFF : None of the inner correction and outer correction circuits operates. An error can be detected.
Set to ECC2 when shipped.

The inner/outer correction circuits operate when the menu and switches are set as follows.

1. Inner correction :
   When the VTR's menu T08. INNER CORRECTION is set to ON or the switches of the processor are set as shown on the table below :

S7-7/PR-115	S4/CF-39	S1-4/VD-04	S1-5/VD-04
ON	ECC2 or ECC1	OFF	ON

When the inner correction circuit operates, the INNER indicator (D3/VD-04) is lit on.

2. Outer correction :
   When the VTR's menu T09. OUTER CORRECTION is set to ON or the switches of the processor are set as shown on the table below :

S7-7/PR-115	S4/CF-39	S1-6/VD-04	S1-7/VD-04	S1-8/VD-04
ON	ECC2	OFF	ON	ON

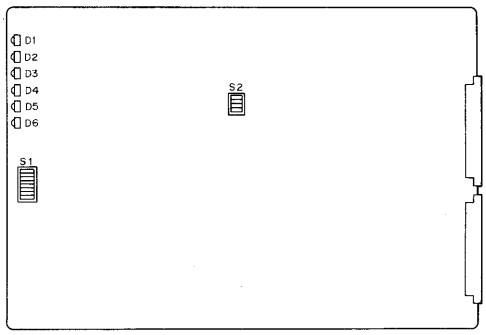
When the outer correction circuit operates, the OUTER indicator (D4/VD-04) is lit on.

S5 : CONCEAL (concealment) switch
Selects whether the error which has not been corrected by the inner correction and the outer correction circuits is compensated.
When the video system boards mode select switch (S7-7/PR-115 : normally set to OFF) is set to ON, this switch is enabled.
When this switch is set to OFF, selecting by the VTR's menu T07. CONCEAL is possible. When setting the menu T07. to ON, the error is compensated.
ON : The error which has not been corrected is compensated. The CONCEAL indicator (D3) is lit on.
OFF : The error is not compensated.
Set to ON when shipped.

S6 : FLAG (error flag) switch
When inspecting the number of the errors in the video signal, this switch selects whether the DIGITAL /ANALOG VIDEO OUT and MONITOR OUT connectors output the normal video signal or the error flag that is converted to the video signal.
When the video system boards mode select switch (S7-7/PR-115 : normally set to OFF) is set to ON, this switch is enabled.
When S6 is set to OFF, selecting by the VTR's menu T10. ERR FLAG DISP (LINE) is possible. When setting to menu T10. to the item except OFF, the error flags output.
ON : The video signal to which the error flag has converted is output. The FLAG indicator (D4) is lit on.
OFF : The normal video signal is output.
Set to OFF when shipped.

VD-04 Board (Slot No.3 to No.6 : VIDEO DECODER)

Component Side



D1 : ALARM indicator (red)
Lights if an error occurs on the VD-04 board.

D2 : LOCAL indicator (green)
When this indicator lights, the switches on the VD-04 are enabled. It lights under the following conditions.

1. When the video system boards mode select switch (S7-7/PR-115) is set to ON
2. When only the power of the processor is turned ON, while the powers both the VTR and the processor are OFF
3. When the PR-115 board is not inserted

D3 : INNER (inner correction) indicator (green)
Lights when the inner correction circuit operates. Not light when the error is detected but not corrected. Refer to the description of the ERROR CORRECT switch (S4) on the CF-39 board.

D4 : OUTER (outer correction) indicator (green)
Lights when the outer correction circuit operates. Not light when the error is detected but not corrected. Refer to the description of the ERROR CORRECT switch (S4) on the CF-39 board.

D5 : ERROR (A) indicator (yellow)
D6 : ERROR (B) indicator (yellow)
Lights when the error on the following video heads is concealed without correcting at the error correction circuit.

Slot No.	3		4		5		6	
Indicator	D5	D6	D5	D6	D5	D6	D5	D6
Video head	CH-7	CH-8	CH-5	CH-6	CH-3	CH-4	CH-1	CH-2

S1-1 to S1-3 : Not used.

S1-4, S1-5 : INNER CORRECTION mode select switch
Enables the inner correction circuit to operate. Refer to the description of the ERROR CORRECT switch (S4) on the CF-39 board.
When the video system boards mode select switch (S7-7/PR-115 : normally set to OFF) is set to ON and the ERROR CORRECT switch (S4/CF-39 : normally set to ECC2) is set to ECC2 or ECC1, these switches are enabled.
When shipped, S1-4 is set to OFF and S1-5 to ON. Never change the setting of these switches. If changing, the inner correction circuit does not operate.

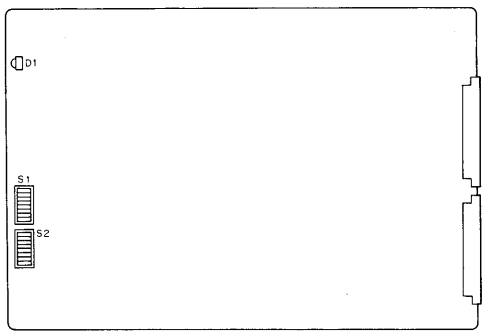
S1-6 to S1-8 : OUTER CORRECTION mode select switch
Enables the outer correction circuit to operate. Refer to the description of the ERROR CORRECT switch (S4) on the CF-39 board.
When the video system boards mode select switch (S7-7/PR-115 : normally set to OFF) is set to ON and the ERROR CORRECT switch (S4/CF-39 : normally set to ECC2) is set to ECC2, these switches are enabled.
When shipped, S1-6 is set to OFF and S1-7 and S1-8 are set to ON.
Never change the setting of these switches. If changing, the outer correction circuit does not operate.

S2-1, S2-2 : INNER DECODER OUTPUT mode select switch
Used to check the inner decoder.
When shipped, these are set to ON. Never change the setting of these switches.

S2-3, S2-4 : OUTER DECODER OUTPUT mode select switch
Used to check the outer decoder.
When shipped, these are set to ON. Never change the setting of these switches.

CI-05 Board (Slot No.7 : CHANNEL INTERCHANGER)

Component Side



Note : When both the video system boards mode select switch (S7-7/PR-115) and the CI-05 board mode select switch (S7-8/PR-115) are set to ON or the TEST ON/OFF switch (S2-8/CI-05) is set to ON, the switches marked by * are enabled. These switches are normally set to OFF.

D1 : ALARM indicator
Lights if an error occurs on the CI-05 board and/or the TEST ON/OFF switch (S2-8/CI-05) is set to ON.

S1-1 to S1-3 : Normally set to OFF.

***S1-4** : NOR/STUNT select switch
Enables the processor to be set to the slow stunt playback mode regardless of the mode of the VTR.
ON : Slow stunt playback mode regardless of the mode of the VTR.
OFF : Normal playback mode
Set to OFF (NOR) when shipped.

***S1-5** : NOR/FAST select switch
Enables the processor to be set to the fast playback mode regardless of the mode of the VTR.
ON : Fast playback mode regardless of the mode of the VTR.
OFF : Normal playback mode
Set to OFF (NOR) when shipped.

*S1-6 : FOW/REV select switch
Enables the processor to be set to the forward or reverse mode regardless of the mode of the VTR. When the NOR/STUNT switch (S1-4 : normally set to OFF) is set to ON (STUNT), this switch is enabled.
ON : REVERSE mode
OFF : FORWARD mode
Set to OFF (FOW) when shipped.

*S1-7 : REC/PB select switch
Enables the processor to be set to the REC or PB mode regardless of the mode of the VTR.
ON : Playback mode regardless of the mode of the VTR.
OFF : REC mode regardless of the mode of the VTR.
Set to OFF (REC) when shipped.

*S1-8 : NOR/MOV select switch
Enables the processor to be set to the bidirex playback mode regardless of the mode of the VTR.
ON : Bidirex playback mode
OFF : Normal playback mode
Set to OFF (NOR) when shipped.

*S2-1 : FREEZE switch A
*S2-2 : FREEZE switch B
Enables the processor to output the freeze picture.

S2-1	S2-2	Types of freeze picture
ON	ON	FIELD 1 FREEZE
ON	OFF	FIELD 2 FREEZE
OFF	ON	FRAME (FIELD 1 & 2) FREEZE
OFF	OFF	NORMAL PICTURE

When shipped, both switches are set to OFF.

*S2-3 : EE/TAPE select switch
Enables the processor to be set to the EE mode regardless of the mode of the VTR.
ON : Normal playback mode
OFF : EE mode regardless of the mode of the VTR
Set to OFF (EE) when shipped.

*S2-4 : BYPASS-A switch
Sets the video system to the bypass mode between the SIF-4 and the PIF-3 boards.
ON : Normal mode
OFF : Bypass mode
Set to OFF when shipped.

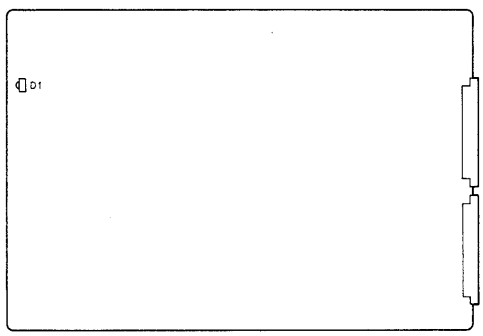
*S2-5 : BYPASS-B switch
Always set to OFF. Never change the setting.

S2-6, S2-7 : Not used.

S2-8 : TEST ON/OFF switch
When both the video system boards mode select switch (S7-7/PR-115) and the CI-05 board mode select switch (S7-8/PR-115) are set to ON, the switches on all of the video system boards are enabled.
However, when S2-8/CI-05 is set to ON, all switches on the CI-05 board will be enabled regardless of the setting of S7-7 and S7-8 on the PR-115 board.
When S2-8/CI-05 is set to ON, the ALARM indicator (D1/CI-05) and the red TEST MODE indicator on the front panel light on.

TB-07 Board (Slot No.8 : TIME BASE CORRECTOR)

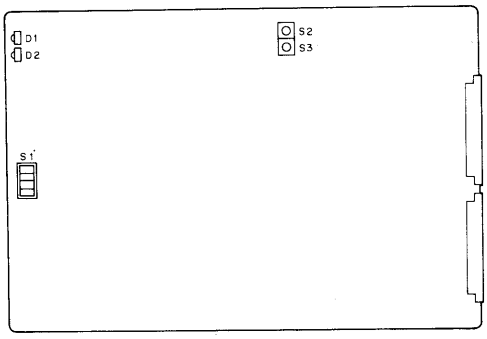
Component Side



D1 : ALARM indicator (red)
Lights if an error occurs on the TB-07 board.

VE-18 Board (Slot No.9 & 10 : VIDEO ENCODER)

Component Side



D1 : ALARM indicator (red)
Lights if an error occurs on the VE-18 board.

D2 : LOCAL indicator (green)
When this indicator lights, the switches on the VE-18 board are enabled. It lights under the following conditions.

1. When the video system boards mode select switch (S7-7/PR-115) is set to ON
2. When only the power of the processor is turned ON, while the powers both the VTR and the processor are OFF
3. When the PR-115 board is not inserted

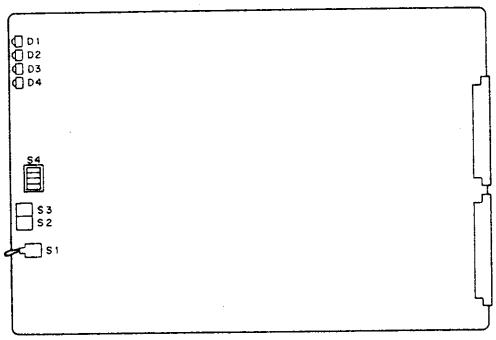
S1-1 : 8-8 conversion switch
When the video system boards mode select switch (S7-7/PR-115 : normally set to OFF) is set to ON, this switch is enabled.
Normally, set to OFF. If setting to ON, 8-8 conversion is not performed.

S1-2 to S1-4 : Not used.

S2, S3 : Delay among channels setting switch
Never change the setting. If changing, the recording may not be normally.
When shipped, S2 is set to D, S3 to 6.

SP-06 Board
(Slot No.11 : SERIAL/PARALLEL CONVERTER)

Component Side



D1 : ALARM indicator (red)
Lights if an error occurs on the SP-06 board.

D2 : LOCAL indicator (green)
When this indicator lights, the switches on the SP-06 board are enabled. It lights under the following conditions.

1. When the video system boards mode select switch (S7-7/PR-115) is set to ON
2. When only the power of the processor is turned ON, while the powers both the VTR and the processor are OFF
3. When the PR-115 board is not inserted

D3 : DIN (Digital input) indicator (green)
Lights when the digital input is selected for video input signal.
Refer to the description of the analog/digital input select switch (S6-8/PR-115).

D4 : SG (internal test signal) indicator (yellow)
Lights when the test signal which is generated in the processor is used. Refer to the description of the SG switch (S1/SP-06).

S1 : SG (test signal) switch
Selects the external video input signal or the test signal generated in the processor. When the video system boards mode select switch (S7-7/PR-115 : normally set to OFF) is set to ON, this switch is enabled.
ON : The test signal which is generated in the processor is used.
The type of the test signals by the SG SELECT switch (S2) is selected. The SG indicator (D4) lights on.
OFF : The external video input signal is used.
Set to OFF when shipped.
However, when S7-7 on the PR-115 board is set to OFF and setting the VTR's Menu T20. VIDEO TEST SG to the item except OFF, the test signal is used regardless of the setting of S1 on the SP-06 board, and D4 on the SP-06 board lights on.

S2 : SG SELECT (signal generator) switch
Selects the type of the test signals generated in the processor, when both the video system boards mode select switch (S7-7/PR-115 : normally set to OFF) and the SG switch (S1/SP-06 : normally set to OFF) are set to ON.

S2	Test signal
0 or 8	Composite signal (Note)
1 or 9	Color bar
2 or A	Multi burst
3 or B	10-step linearity
4 or C	Pulse & bar
5, 6, 7, D, E, or F	Black burst

Note : The composite signal consists of color bar, multi burst, pulse & bar and 10-step linearity signals.

Set to 0 when shipped.

S3 : CHANNEL SHIFT switch
This switch makes the channels of the recording video signals which are paralleled to 8 channels shift. Used to find and check the channel on which an error occurs.
When both the video system boards mode select switch (S7-7/PR-115 : normally set to OFF) and the CHANNEL INTERLEAVE OFF switch (S4-1 : normally set to OFF) are set to ON, this switch is enabled.

S3	Channel shift
0 or 8	0
1 or 9	1
2 or A	2
3 or B	3
4 or C	4
5 or D	5
6 or E	6
7 or F	7

EX. When S3 is set to 4 or C, all channels are shifted by 4 channels.
Set to 0 when shipped.

S4-1 : CHANNEL INTERLEAVE OFF switch
Selects whether Y and chroma (P_B, P_R) signals are mixed or not.
When the video system boards mode select switch (S7-7/PR-115 : normally set to OFF) is set to ON, this switch is enabled. S4-1 must be set to the same position as that of the CHANNEL DE-INTERLEAVE OFF switch (S1-1/CF-39 : normally set to OFF).
ON : The Y and chroma (P_B, P_R) signals are separately processed.
OFF : The mixed Y and chroma signals are processed.
Set to OFF when shipped.

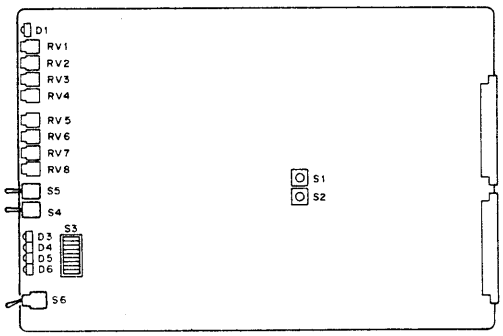
S4-2 : User data REC INT/EXT select switch
Selects the signal source of the user data (VITC etc.).
When the video system boards mode select switch (S7-7/PR-115 : normally set to OFF) is set to ON, this switch is enabled.
ON : The user data which are input to the DIGITAL IN connector are recorded.
OFF : The user data which are generated in the HDDP-1000 are recorded.
Set to OFF when shipped.

S4-3, S4-4 : Not used.

SG-151 (and SW-334) Board

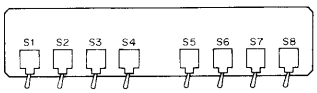
(Slot No.12 : SYNC GENERATOR)

Component Side



SW-334 Board

Component side



Note : When the TEST ON/OFF switch (S3-8/SG-151 : normally set to OFF) is set to ON, the switches marked by * are enabled.

D1 : ALARM indicator (red)
Lights if an error occurs on the SG-151 board or when the TEST ON/OFF switch (S3-8/SG-151) is set to ON.

D3 : IS mode indicator (yellow)
Lights when the analog video G/Y input signal carries the sync signal.

D4 : ES mode indicator (yellow)
Lights when the SYNC signal (analog video input) is input.

D5 : DS mode indicator (yellow)
Lights when the sync is detected from the digital video sync signal input.

D6 : LOCK mode indicator (green)
Lights when the input reference signal generator is locked to the analog input (G/Y or SYNC) signal.

RV1 : G/Y signal input level control
RV2 : B/P_B signal input level control
RV3 : R/P_R signal input level control
Adjust the analog video input level. Only the following settings make these controls to be enabled.
When S1/SW-334 is set to MAN, RV1/SG-151 is enabled.
When S2/SW-334 is set to MAN, RV2/SG-151 is enabled.
When S3/SW-334 is set to MAN, RV3/SG-151 is enabled.

RV4 : MASTER input level control
Adjusts the analog video input level of the GBR or YP_BP_R signals simultaneously. When the MASTER input level adjustment MAN/FIX switch (S4/SW-334) is set to MAN, this control is enabled. (Even though others of the input level adjustment MAN/FIX switches are set to FIX, this control is enabled.)

RV5 : Y signal output level control
RV6 : P_B signal output level control
RV7 : P_R signal output level control
Adjust the analog video output level. Only the following settings make these controls to be enabled.
When S5/SW-334 is set to MAN, RV5/SG-151 is enabled.
When S6/SW-334 is set to MAN, RV6/SG-151 is enabled.
When S7/SW-334 is set to MAN, RV7/SG-151 is enabled.

RV8 : MASTER output level control
Adjusts the analog video output level of the YP_BP_R signal. When the MASTER output level adjustment MAN/FIX switch (S8/SW-334) is set to MAN, this control is enabled. (Even though others of the output level adjustment MAN/FIX switches are set to FIX, this control is enabled.)

S1 : SYNC PHASE OFFSET switch
Selects the adjustable range of the SYNC PHASE adjusting switches (S4, S5). When S1 is set to 5 (factory setting), the adjustable range of S4 and S5 is $+1.5\,\mu$sec to $-0.5\,\mu$sec. When S1 is set to 6, the adjustable range is offset by $0.85\,\mu$sec delay : as a result, the range becomes $+0.65\,\mu$sec to $-1.35\,\mu$sec. When S1 is set to 4, the range is offset by $0.85\,\mu$sec advance : as a result, the range becomes $+2.35\,\mu$sec to $+0.35\,\mu$sec.
If the factory setting (position 5) is not, use this switch.
Never set this switch to the position except 4, 5 or 6. If not, the processor may not normally operate.

S2 : REC Y/C DELAY adjusting switch
This switch compensates the delay which is caused by the filter of the ADA-12 board.
When turning this switch clockwise by one step, the Y signal delays by 13.5 nsec. When turning counterclockwise, the chroma signal (P_B, P_R) delays.
Never turn this switch because it has been adjusted for the filter on the ADA-12 board at factory.
Set to 3 when shipped. (The setting is different by the units.)
When setting to 0 to 5, this switch is enabled.

***S3-1** : Processor reference select switch
Selects the source of the PROC. REF signal (reference signal of the video PB processor), the digital video input signal or the analog video input signal. Selection of the source of the COM REF signal (reference signal of the video REC processor and the VTR) depends on the setting of S3-2. When the TEST ON/OFF switch (S3-8/SG-151 : normally set to OFF) is set to ON, these switches are enabled.

ON : The PROC. REF signal is generated from the sync signal which is detected from the digital video input signal. The REF SYNC indicator on the front panel indicates both INPUT and EXT REF.

OFF : The PROC. REF signal is generated from the signal which is selected by the analog reference select switch (S3-4/SG-151 : normally set to OFF). When the selected signal is not input to the HDDP-1000 and/or the GEN/INT switch (S3-3/SG-151 : normally set to GEN) is set to INT, the PROC. REF signal is made from the oscillator inside the HDDP-1000. The REF SYNC indicator on the front panel depends on the setting of S3-4.

Set to OFF when shipped.

When the selected signal is not input, the REF SYNC indicator on the front panel blinks.
The reference signal is selected by not only the switches on the SG-151 board but also S6-7 on the PR-115 board and the VTR's menu S12. REF SELECT, I80. INPUT ANALOG/DIGITAL and I82. PROC PB REF SELECT. Which of them is enabled depends on the settings of S3-8 on the SG-151 board and S7-7 on the PR-115 board as shown below.

S3-8 SG-151	S7-7 PR-115	Ref. signal selection
0	0	depends on Menu S12, I80, I82
0	1	depends on S6-7/PR-115
1	×	depends on switches/SG-151

0 : OFF, 1 : ON, × : OFF or ON

When S3-8 on the SG-151 board is set to ON, the reference signal is selected as shown on the table below. In case of other setting, the recording and/or playback is not performed correctly.

PROC REF : 0=OFF=ANA, 1=ON=DIG
COM REF : 0=OFF=ANA, 1=ON=DIG
REF SYNC : 0=60Hz 1=59.94Hz, X=60 or 59.94Hz
GEN/INT : 0=OFF=EXT, 1=ON=INT, X=OFF or ON
ANALOG REF : 0=OFF=G/Y, 1=ON=SYNC, X=OFF or ON

S3-1	⑤ S3-2	S6	S3-3	S3-4	Source of COM REF signal	Source of PROC. REF signal	Note
0	0	0	0	0	ANALOG VIDEO G/Y IN signal	ANALOG VIDEO G/Y IN signal	①
0	0	0	0	1	ANALOG VIDEO SYNC IN signal	ANALOG VIDEO SYNC IN signal	①
0	0	0	1	×	Oscillator in HDDP-1000	Oscillator in HDDP-1000	②
0	0	1	0	0	ANALOG VIDEO G/Y IN signal	ANALOG VIDEO G/Y IN signal	③
0	0	1	0	1	ANALOG VIDEO SYNC IN signal	ANALOG VIDEO SYNC IN signal	③
0	1	0	0	0	DIGITAL VIDEO IN signal	ANALOG VIDEO G/Y IN signal	④
0	1	0	0	1	DIGITAL VIDEO IN signal	ANALOG VIDEO SYNC IN signal	④
1	0	0	0	0	ANALOG VIDEO G/Y IN signal	DIGITAL VIDEO IN signal	④
1	0	0	0	1	ANALOG VIDEO SYNC IN signal	DIGITAL VIDEO IN signal	④
1	1	×	×	×	DIGITAL VIDEO IN signal	DIGITAL VIDEO IN signal	

0 : OFF, 1 : ON, × : OFF or ON

Note ① : The field frequency of the analog video (G/Y or SYNC) input signal must be 60 Hz.

Note ② : Only playback is correctly performed. The field frequency is 60 Hz.

Note ③ : Only playback is correctly performed. The field frequency of the analog video (G/Y or SYNC) input signal must be 59.94 Hz.

Note ④ : The field frequency of both the digital video input signal and the analog video (G/Y or SYNC) input must be 60 Hz and they must be synchronized within the 50 μ sec phase difference.

Note ⑤ : The COM REF select switch (S3-2) must be set to the same position as that of the ANALOG/DIGITAL IN select switch (S3-7).

＊S3-2 : COM. reference select switch
Selects the source of the COM. REF signal (reference signal of the video REC processor and the VTR). When the TEST ON/OFF switch (S3-8 : normally set to OFF) is set to ON, this switch is enabled.
The reference signal is selected by not only S3-2 but also some switches. Refer to the description of the processor reference select switch (S3-1).
ON : The reference signal is generated from the sync which is detected from the digital video input signal.
OFF : The reference signal is generated from the analog signal which is selected by the analog reference select switch (S3-4). Be sure to the same setting as that of the analog/digital input select switch (S3-7/SG-151 : normally set to OFF).
Set to OFF when shipped.

＊S3-3 : GEN/INT select switch
Selects whether the reference signal oscillator in the HDDP-1000 is made to lock to the analog input signal (G/Y or SYNC) or not.
When adjusting the oscillating frequency of the reference signal oscillator by RV9 on the SG-151 board, set this switch to ON (INT).
Refer to the description of the processor reference select switch (S3-1).
ON : The HDDP-1000 is put into the internal mode. The reference signal oscillator free-runs.
OFF : The HDDP-1000 is put into the genlock mode. The reference signal oscillator is locked to the analog input signal which is selected by S3-4.
Set to OFF when shipped.

＊S3-4 : Analog reference select switch
Selects the source of the analog reference signal. When the TEST ON/OFF switch (S3-8 : normally set to OFF) is set to ON, this switch is enabled.
The reference signal is selected by not only S3-4 but also some switches. Refer to the description of the processor reference select switch (S3-1).
ON : The analog video SYNC input is selected for the source of the analog reference signal. The REF SYNC indicator on the front panel indicates EXT.
OFF : The analog video G/Y input is selected for the source of the analog reference signal. The REF SYNC indicator on the front panel indicates INPUT.
When the selected signal is not input, the REF SYNC indicator on the front panel blinks.
Set to OFF when shipped.

＊S3-5 : MONITOR SEL0 INP/OUT select switch
＊S3-6 : MONITOR SEL1 VID/CTL/RF select switch
Select the video signal which is output from the MONITOR OUT and WFM OUT connector (G/Y, B/P_B, R/P_R, SYNC) as shown on the table below. When the TEST ON/OFF switch (S3-8 : normally set to OFF) is set to ON, these switches are enabled.

S3-5	S3-6	MONITOR OUT signal	WFM OUT signal
0	0	ANALOG VIDEO IN signal	PB CTL or RF envelope (depends on Menu S03)
0	1	ANALOG VIDEO IN signal	ANALOG VIDEO IN signal
1	0	ANALOG VIDEO OUT signal	PB CTL or RF envelope (depends on Menu S03)
1	1	ANALOG VIDEO OUT signal	ANALOG VIDEO IN signal

0 : OFF, 1 : ON

Set to OFF when shipped.

＊S3-7 : Analog/digital input select switch
Selects the video input signal (recording signal). Be sure to set S3-7 to the same setting as that of the COM. reference select switch (S3-2 : normally set to OFF). When the TEST ON/OFF switch (S3-8 : normally set to OFF) is set to ON, this switch is enabled.
ON : The digital video input signal is selected for the recording signal. The INPUT VIDEO indicator on the front panel indicates DIGITAL, and the SOURCE VIDEO indicator lights off.
OFF : The analog video input signal is selected for the recording signal. The INPUT VIDEO indicator on the front panel indicates ANALOG.
Set to OFF when shipped.

＊S3-8 : TEST ON/OFF switch
ON : The switches (marked by ＊) on the SG-151 board are enabled.
The ALARM indicator (D1/SG-151) lights on, and the PROC. SW ENABLE indicator on the front panel indicates ON.
OFF : The switches (marked by ＊) on the SG-151 board are disabled.
In this case, the setting is performed by the menu of the VTR.
Set to OFF when shipped.

S4 : SYNC PHASE FINE adjustment switch
S5 : SYNC PHASE COARSE adjustment switch
Used to adjust the phase of the video output (analog and digital) to the reference signal. The adjustable range is +1.5 μ sec to −0.5 μ sec to the reference signal, and 1 step of S4 is approximately 13 nsec, that of S5 is approximately 160 nsec.
When turning the switches clockwise, the phase delays.
During adjusting, the picture may be disturbed, but it is not trouble.
The thick line on the panel of S5 shows the preset position. When turning S4 while S5 is preset, the video output phase to the reference signal is able to be adjusted within 0±7 nsec.
The adjustable range of these switches is able to be offset by the SYNC PHASE OFFSET switch (S1 : normally set to OFF). Refer to the description of S1.
When shipped, S5 is set to PRESET but S4 is free.

S6 : REF SYNC select switch
Selects whether the reference signal oscillator for the vertical frequency 59.94 Hz in the HDDP-1000 operates or that for 60.00 Hz.
Refer to the description of the processor reference select switch (S3-1 : normally set to OFF).
59.94 Hz : This position is permitted in the playback mode but not in the recording mode.
60.00 Hz : This position is permitted in both the playback and recording modes.
Set to 60 Hz when shipped.

S1/SW-334 : G/Y signal input level adjustment MAN/FIX switch
S2/SW-334 : B/P_B signal input level adjustment MAN/FIX switch
S3/SW-334 : R/P_R signal input level adjustment MAN/FIX switch
MAN : Enable each analog video input level to be adjusted by RV1 (G/Y), RV2 (B/P_B) and RV3 (R/P_R) on the SG-151 board.
FIX : The input level is preset.
When shipped, all of those switches are set to FIX.

S4/SW-334 : MASTER input level adjustment MAN/FIX switch
MAN : Enables the level of the analog video GBR (or YP_BP_R) input signals to be adjusted simultaneously by RV4 on the SG-151 board.
FIX : The input level is preset.
Set to FIX when shipped.

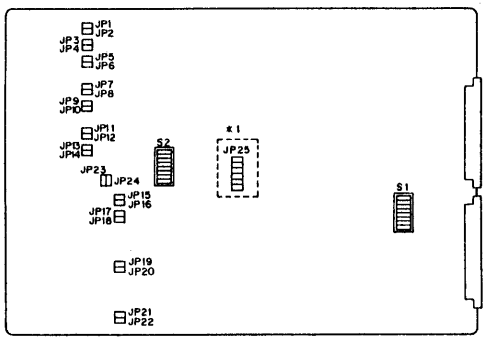
Note : Set the analog video input signal select switch (S7-5/PR-115) or menu I81. INPUT G.B.R/Y.P_B.P_R according to the type of the analog video input signals.

S5/SW-334 : Y signal output level adjustment MAN/FIX switch
S6/SW-334 : P_B signal output level adjustment MAN/FIX switch
S7/SW-334 : P_R signal output level adjustment MAN/FIX switch
MAN : Enables each analog video output level to be adjusted by RV5 (Y), RV6 (P_B) and RV7 (P_R) on the SG-151 board.
FIX : The output level is preset.
When shipped, all of those switches are set to FIX.

S8/SW-334 : MASTER output level adjustment MAN/FIX switch
MAN : Enables the analog video YP_BP_R output signal to be adjusted simultaneously by RV8 on the SG-151 board.
FIX : The output level is preset.
Set to FIX when shipped.

ADA-12 Board (VIDEO A/D, D/A CONVERTER)

Component Side



***1 : The ADA-12 board with suffix-12 or later has the jumper JP25.**

S1-1 : Not used.

S1-2 : Analog video input select switch
Set this switch according to the type of the analog video input signals (GBR or YP_BP_R). When the LOCAL/REMOTE select switch (S1-8 : normally set to OFF) is set to ON (LOCAL), this switch is enabled.
ON : GBR signals are the input signals. The SOURCE VIDEO indicator on the front panel indicates GBR.
OFF : YP_BP_R signals are the input signals. The SOURCE VIDEO indicator on the front panel indicates Y/P_B/P_R.
Set to OFF when shipped.

Selection of the type of the analog video input signals is performed by not only S1-2 but also S7-5 on the PR-115 board and the VTR's menu I81. INPUT G.B.R/Y.P_B.P_R. Which of them is enabled depends on the setting of S1-8 on the ADA-12 board and S7-7 on the PR-115 board as shown on the table.

S1-8 ADA-12	S7-7 PR-115	Selection of the analog video input signal (GBR/$YP_B P_R$)
0	0	Menu I81.
0	1	S7-5/PR-115
1	×	S1-2/ADA-12

0 : OFF, 1 : ON, × : OFF or ON

S1-3 : Monitor video output level select switch
Decreases the level of the video signals which are output to the MONITOR OUT connector.
When the LOCAL/REMOTE select switch (S1-8 : normally set to OFF) is set to ON (LOCAL), this switch is enabled.
ON : The normal level is output.
OFF : The monitor video output level decreases to 490 to 560 mV.
Set to OFF when shipped.

S1-4 : Analog video output select switch
Selects the analog video output signal (GBR or YP_BP_R).
When the LOCAL/REMOTE select switch (S1-8 : normally set to OFF) is set to ON (LOCAL), this switch is enabled.
ON : GBR signals are output. The ANALOG OUT indicator on the front panel indicates GBR.
OFF : YP_BP_R signals are output. The ANALOG OUT indicator on the front panel indicates Y/P_B/P_R.
Set to OFF when shipped.

Selection of the type of the analog video output signals is performed by not only S1-4 but also S7-6 on the PR-115 board and the VTR's menu I83. OUTPUT G.B.R/Y.P_B.P_R. Which of them is enabled depends on the settings of S1-8 on the ADA-12 board and S7-7 on the PR-115 board as shown on the table below.

S1-8 ADA-12	S7-7 PR-115	Selection of the analog video output signal (GBR/$YP_B P_R$)
0	0	Menu I83.
0	1	S7-6/PR-115
1	×	S1-4/ADA-12

0 : OFF, 1 : ON, × : OFF or ON

S1-5 : Monitor video black select switch
S1-6 : Monitor video gray select switch
Sets the analog video signals which are output from the MONITOR OUT connector to the black signal or the gray signal as shown on the table below.
When the LOCAL/REMOTE select switch (S1-8 : normally set to OFF) is set to ON (LOCAL), these switches are enabled.

S1-5	S1-6	MONITOR OUT signal
1	1	Normal analog video signal
0	0	Gray signal
0	1	Black signal

0 : OFF, 1 : ON

When shipped, all of those switches are set to OFF.

S1-7 : Character addition mode select switch
Selects whether the character can be added to the MONITOR OUT and WFM OUT signals or to the analog video input signals.
When the LOCAL/REMOTE select switch (S1-8 : normally set to OFF) is set to ON (LOCAL), this switch is enabled.
ON : The character can be added to the MONITOR OUT and the WFM OUT signals. When setting the VTR's menu S59. MIXED CHARA OUTPUT to MONITOR, the character is added.
OFF : The character can be added to the analog input video signal. When setting the VTR's menu S59. MIXED CHARA OUTPUT to MONITOR and I60. CHARACTER RECORD to ENABLE and the VTR is in the REC mode, the character is added.
Set to OFF when shipped.

S1-8 : LOCAL/REMOTE select switch
When setting to ON, S1-1 to S1-7 of S1 are enabled, and the red TEST MODE indicator on the front panel lights on.
When setting to OFF, S1-1 to S1-7 of S1 are disabled. Therefore, the function of S1 is controlled by the switches on the PR-115 board (enables the analog video in/out to select) or the VTR.

S2-1 : P_R output gain control ON/OFF switch
S2-2 : P_B output gain control ON/OFF switch
S2-3 : Y output gain control ON/OFF switch
Selects whether the gain of the analog video output signals (YP_BP_R) is controlled by the potentiometers on the SG-151 or preset.
Used to inspect the operation of only the ADA-12 board.
ON : The output gain can be controlled by RV5 (Y), RV6 (P_B) and RV7 (P_R) on the SG-151 board.
OFF : The output gain is preset.
When shipped, all of those switches are set to ON.

S2-4 : R/P_R input gain control ON/OFF switch
S2-5 : B/P_B input gain control ON/OFF switch
S2-6 : G/Y input gain control ON/OFF switch
Selects whether the gain of the analog video input signals (YP_BP_R or GBR) is controlled by the potentiometers on the SG-151 or preset.
Used to inspect the operation of only the ADA-12 board.
ON : The input gain can be controlled by RV1 (G/Y), RV2 (B/P_B) and RV3 (R/P_R) on the SG-151 board.
OFF : The input gain is preset.
When shipped, all of those switches are set to ON.

S2-7, **S2-8** : Not used.

JP1 to JP22 :
These are the jumper pins for corresponding to change the matrix. Normal settings are shown below. The ADA-12 board with the suffix -11 does not have A/B indications. If it is the case, replace A with short and B with open.

JP1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21 : A
JP2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22 : B

JP23, **JP24** : SYNC COMP/NON COMP select jumper
Select whether the sync pulse is added to the analog video output (and MONITOR OUT and WFM OUT) signals or not.
Never set them to the other combination than the table below.

JP23	JP24	Analog video output signal
SHORT	OPEN	with sync (When shipped)
OPEN	SHORT	without sync

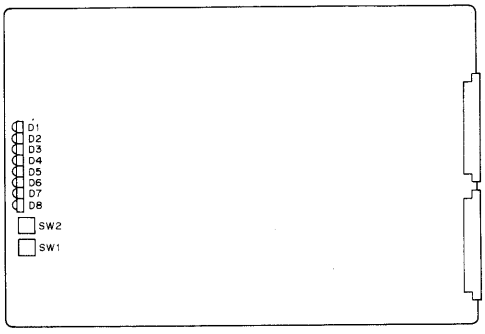
***1 : The jumper JP25 is used for the ADA-12 board with suffix-12.**

JP25 : SYNC out DELAY adjusting jumper
This jumper pin compensates the delay which is caused by the filters (FL401, FL501, FL601 and FL701) on the ADA-12 board.
Never set it to the other position.

DEC-41 Board

(Slot No.13 : AUDIO DECODER/ENCODER)

Component Side



D1 : CH-1 CRCC ERR (CRCC error) indicator (red)
D2 : CH-2 CRCC ERR (CRCC error) indicator (red)
D3 : CH-3 CRCC ERR (CRCC error) indicator (red)
D4 : CH-4 CRCC ERR (CRCC error) indicator (red)
D5 : CH-5 CRCC ERR (CRCC error) indicator (red)
D6 : CH-6 CRCC ERR (CRCC error) indicator (red)
D7 : CH-7 CRCC ERR (CRCC error) indicator (red)
D8 : CH-8 CRCC ERR (CRCC error) indicator (red)
Light when the CRCC error is detected from the digital audio track.

SW1 : MUTE SENS (mute sense) switch
Sets the number of samples, which could not be corrected, in one block of the de-interleaved digital audio playback data at which the audio will be muted. One block has six odd samples and six even samples. The audio output will be muted when the number of not corrected samples exceeds the designated number in both odd and even samples simultaneously.

SW1	Samples
0, 1, 2, 8, 9 ro A	2
3 or B	3
4 or C	4
5 or D	5
6, 7, E or F	6

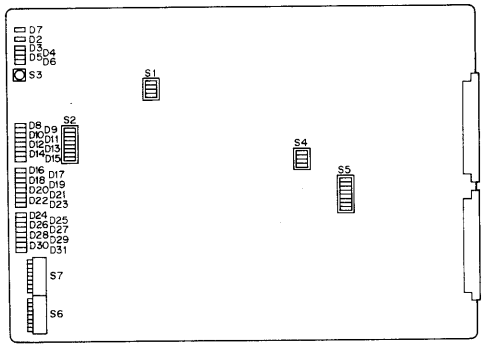
Normally, set to 3 or B.

SW2 : Normally, set to 0.

PR-115 Board

(Slot No.14 : AUDIO PROCESSOR & SYSTEM CONTROLLER)

Component Side



D2 : REC indicator (red)
Lights during audio recording.

D3 : CH-1/2 DIN (digital audio input) indicator (green)
D4 : CH-3/4 DIN (digital audio input) indicator (green)
D5 : CH-5/6 DIN (digital audio input) indicator (green)
D6 : CH-7/8 DIN (digital audio input) indicator (green)
Light when an AES/EBU format digital audio signal is input.

D7 : LOCK indicator (green)
Lights when the audio system clock is locked to the video sync signal.

D8 : CH-1 MUTE indicator (red)
D9 : CH-2 MUTE indicator (red)
D10 : CH-3 MUTE indicator (red)
D11 : CH-4 MUTE indicator (red)
D12 : CH-5 MUTE indicator (red)
D13 : CH-6 MUTE indicator (red)
D14 : CH-7 MUTE indicator (red)
D15 : CH-8 MUTE indicator (red)
Light when the audio is muted due to incomplete concealment or when the system requires audio muting.

D16 : CH-1 HOLD indicator (yellow)
D17 : CH-2 HOLD indicator (yellow)
D18 : CH-3 HOLD indicator (yellow)
D19 : CH-4 HOLD indicator (yellow)
D20 : CH-5 HOLD indicator (yellow)
D21 : CH-6 HOLD indicator (yellow)
D22 : CH-7 HOLD indicator (yellow)
D23 : CH-8 HOLD indicator (yellow)
Light when the error data, which could not be corrected are replaced with the preceding data.

D24 : CH-1 AVER indicator (green)
D25 : CH-2 AVER indicator (green)
D26 : CH-3 AVER indicator (green)
D27 : CH-4 AVER indicator (green)
D28 : CH-5 AVER indicator (green)
D29 : CH-6 AVER indicator (green)
D30 : CH-7 AVER indicator (green)
D31 : CH-8 AVER indicator (green)
Light when the error data, which could not be corrected are interpolated by the average value of the preceding and succeeding data.

S1 : Not used (not installed).

S2-1 to S2-4 : Normally set to OFF.

S2-5 : CPU SQUEEZE switch
ON : The main CPU of HDDP-1000 can be interrupted.
OFF : The main CPU of HDDP-1000 cannot be interrupted.
Set to ON when shipped.

S2-6 to S2-8 : Normally set to ON.

S3 : SYSTEM RESET switch
Return the CPU of HDDP-1000 to the initial setting. Use it when HDDP-1000 cannot normally operate.

S4, S5 : Normally set to OFF.

Note : The PR-115 board with suffix-12 or later does not have the switch S4.

S6-1 : Audio system VTR control inhibit switch
ON : The audio system control from the VTR is inhibited, and the setting is kept when the switch is turned to ON. The PROC. SW ENABLE indicator on the front panel indicates ON, and the error message, PR115 SW, is indicated on the control panel of the VTR.
OFF : Enables the audio system controls from the VTR. The PROC. SW ENABLE indicator on the front panel indicates OFF.
Set to OFF when shipped.

S6-2 : REC INHIBITION switch
Selects whether the audio recording is inhibited or permitted.
ON : Audio recording is inhibited.
OFF : Audio recording is permitted.
Set to OFF when shipped.

S6-3 to S6-6 : Normally set to OFF.

S6-7 : Analog reference select switch
Selects the source of the analog reference signal. When the video system boards mode select switch (S7-7/PR-115 : normally set to OFF) is set to ON and the TEST ON/OFF switch (S3-8/SG-151 : normally set to OFF) is set to OFF, this switch is enabled.
ON : The analog video SYNC input is selected for the source of the analog reference signal. The REF SYNC indicator on the front panel indicates EXT.
OFF : The analog video G/Y input is selected for the source of the analog reference signal. The REF SYNC indicator on the front panel indicates INPUT.
Set to OFF when shipped.

The analog reference signal is selected by not only S6-7 but also S3-4 on the SG-151 board and the VTR's menu S12. REF SELECT.
Which of them is enabled depends on the settings of S3-8 on the SG-151 board and S7-7 on the PR-115 board.

S3-8 SG-151	S7-7 PR-115	Selection of the analog reference signal
0	0	Menu S12.
0	1	S6-7/PR-115
1	×	S3-4/SG-151

0 : OFF, 1 : ON, × : OFF or ON

S6-8 : Analog/digital input select switch
Selects the video input signal (recording signal). When the video system boards mode select switch (S7-7/PR-115 : normally set to OFF) is set to ON and the TEST ON/OFF switch (S3-8/SG-151 : normally set to OFF) is set to OFF, this switch is enabled.
ON : The digital video input signal is selected for the recording signal. The INPUT VIDEO indicator on the front panel indicates DIGITAL.
OFF : The analog signal is selected for the recording signal. The INPUT VIDEO indicator on the front panel indicates ANALOG.
Set to OFF when shipped.

The video input signal is selected by not only S6-8 but also S3-7/SG-151 and the VTR's menu I80. INPUT ANALOG/DIGITAL. Which of them is enabled depends on the settings of S3-8 on the SG-151 board and S7-7 on the PR-115 board.

S3-8 SG-151	S7-7 PR-115	Selection of the video input signal (analog/digital)
0	0	Menu I80.
0	1	S6-8/PR-115
1	×	S3-7/SG-151

0 : OFF, 1 : ON, × : OFF or ON

S7-1 to S7-3 : Normally set to OFF.

S7-4 :
Determines the mode of the video system of HDDP-1000 when the communication between the HDD-1000 and the HDDP-1000 is interrupted.
ON : EE mode
OFF : The mode is kept at that time.
Set to OFF when shipped.

S7-5 : Analog video input select switch
Set this switch according to the type of the analog video input signal (GBR or YPBPR). When the video system boards mode select switch (S7-7/PR-115) is set to ON and the LOCAL/REMOTE select switch (S1-8/ADA-12) is set to OFF, this switch is enabled.
ON : YPBPR signals are the input signals. The SOURCE VIDEO indicator on the front panel indicates YPBPR.
OFF : GBR signals are the input signals. The SOURCE VIDEO indicator on the front panel indicates GBR.
Set to OFF when shipped.

Selection of the the type of the analog video input signals is performed by not only S7-5 but also S1-2 on the ADA-12 board and the VTR's menu I81. INPUT G.B.R/Y.PB.PR. Which of them is enabled depends on the settings of S1-8 on the ADA-12 board and S7-7 on the PR-115 board.

S1-8 ADA-12	S7-7 PR-115	Selection of the analog video input signal (GBR/YPB PR)
0	0	Menu I81.
0	1	S7-5/PR-115
1	×	S1-2/ADA-12

0 : OFF, 1 : ON, × : OFF or ON

S7-6 : Analog video output select switch
Selects the analog video output signal (GBR or YPBPR). When the video system boards mode select switch (S7-7/PR-115) and the LOCAL/REMOTE select switch (S1-8/ADA-12) is set to OFF, this switch is enabled.
ON : YPBPR signals are output. The ANALOG OUT indicator on the front panel indicates YPBPR.
OFF : GBR signals are output. The ANALOG OUT indicator on the front panel indicates GBR.
Set to OFF when shipped.

Selection of the type of the analog video output signals is performed by not only S7-6 but also S1-4 on the ADA-12 board and the VTR's menu I83. OUTPUT G.B.R/Y.PB.PR. Which of them is enabled depends on the settings of S1-8 on the ADA-12 board and S7-7 on the PR-115 board.

S1-8 ADA-12	S7-7 PR-115	Selection of the analog video output signal (GBR/YPB PR)
0	0	Menu I83.
0	1	S7-6/PR-115
1	×	S1-4/ADA-12

0 : OFF, 1 : ON, × : OFF or ON

S7-7 : Video system boards mode select switch

ON : The settings of switches on the PS-183, CF-39, VD-04, VE-18 and SP-06 boards of the video system boards are enabled, and the settings of switches have priority over the setting of the VTR's menus. Each of the LOCAL indicators (D2/PS-183, CF-39, VD-04, VE-18 and SP-06 boards) lights on. The PROC. SW ENABLE indicator on the front panel indicates ON. Error message, PR115 SW, is displayed on the control panel of the VTR.
When S7-8 on the PR-115 board is set to ON, the switches on the CI-05 board are enabled.
When S3-8 on the SG-151 board is set to OFF, S6-7 and S6-8 on the PR-115 board are enabled.
When S1-8 on the ADA-12 board is set to OFF, S7-5 and S7-6 on the PR-115 board are enabled.

OFF : The settings of switches on the PS-183, CF-39, VD-04, VE-18 and SP-06 boards are disabled, and the settings of the VTR's menus are enabled. Each of the LOCAL indicators on the boards lights off. The PROC. SW ENABLE indicator on the front panel indicates OFF.
The settings of S6-7, S6-8, S7-5 and S7-6 on the PR-115 board are disabled.

Set to OFF when shipped.

When either of S3-8 on the SG-151 board or S1-8 on the ADA-12 board is set to ON, the switches on the SG-151 board or the ADA-12 board are enabled and S6-7, S6-8, S7-5 and S7-6 on the PR-115 board are disabled regardless of the setting of S7-7 on the PR-115 board.
The orders of priority of the settings by the VTR's menu and the switches on the boards are as follows.

0 : OFF, 1 : ON × : OFF or ON

Selection of the reference signal & video input signal

S3-8 SG-151	S7-7 PR-115	Depends on
0	0	VTR's menu
0	1	Switches/PR-115
1	×	Switches/SG-151

Selection of the analog video in/out signals & monitor output signal

S1-8 ADA-12	S7-7 PR-115	Depends on
0	0	VTR's menu
0	1	Switches/PR-115
1	×	Switches/ADA-12

Selection of the function mode

S7-8 PR-115	S7-7 PR-115	Depends on
×	0	VTR's menu or control panel
0	×	
1	1	Switches/CI-05

Selection of the correction mode

S7-7 PR-115	Depends on
0	VTR's menu
1	Switches/PS-183, CF-39, VD-04, VE-18, SP-06

S7-8 : CI-05 board mode setting switch

When the video system boards mode select switch (S7-7/PR-115 : normally set to OFF) is set to ON, this switch is enabled.

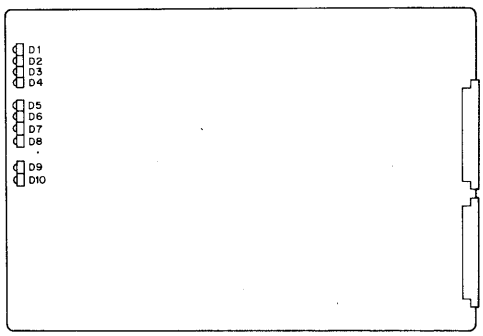
ON : The settings of the switches on the CI-05 board are enabled.
Even though the TEST ON/OFF switch (S2-8/CI-05 : normally set to OFF) is set to OFF, the setting of the switches on the CI-05 board are enabled. The red TEST MODE indicator on the front panel lights on.

OFF : The settings of the switches on the CI-05 board are disabled. The green TEST MODE indicator on the front panel lights on.

Set to OFF when shipped.

DA-28 Board (Slot No.15 : AUDIO D/A CONVERTER)

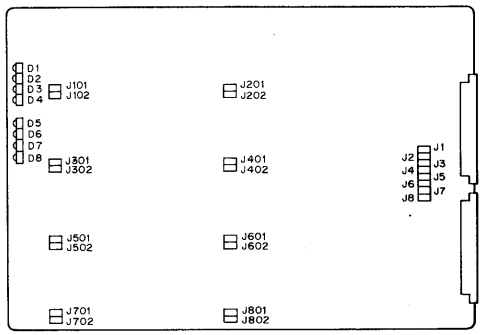
Component Side



D1 : CH-1 DE EMP (de-emphasis) indicator (red)
D2 : CH-2 DE EMP (de-emphasis) indicator (red)
D3 : CH-3 DE EMP (de-emphasis) indicator (red)
D4 : CH-4 DE EMP (de-emphasis) indicator (red)
D5 : CH-5 DE EMP (de-emphasis) indicator (red)
D6 : CH-6 DE EMP (de-emphasis) indicator (red)
D7 : CH-7 DE EMP (de-emphasis) indicator (red)
D8 : CH-8 DE EMP (de-emphasis) indicator (red)
Light on when the de-emphasis circuit for the analog audio output is enabled.
However, the color of these indicators is changed to be yellow from the DA-28 board with suffix -13.

AD-38 Board (Slot No.16 : AUDIO A/D CONVERTER)

Component Side



D1 : CH-1 EMP (emphasis) indicator (red)
D2 : CH-2 EMP (emphasis) indicator (red)
D3 : CH-3 EMP (emphasis) indicator (red)
D4 : CH-4 EMP (emphasis) indicator (red)
D5 : CH-5 EMP (emphasis) indicator (red)
D6 : CH-6 EMP (emphasis) indicator (red)
D7 : CH-7 EMP (emphasis) indicator (red)
D8 : CH-8 EMP (emphasis) indicator (red)
Light on when the emphasis circuit for the analog audio input is enabled.
However, the color of these indicators is changed to be yellow from the unit of serial number 10201.

J101/102 : CH-1 analog audio input impedance select jumper
J201/202 : CH-2 analog audio input impedance select jumper
J301/302 : CH-3 analog audio input impedance select jumper
J401/402 : CH-4 analog audio input impedance select jumper
J501/502 : CH-5 analog audio input impedance select jumper
J601/602 : CH-6 analog audio input impedance select jumper
J701/702 : CH-7 analog audio input impedance select jumper
J801/802 : CH-8 analog audio input impedance select jumper
These are the jumpers for selecting the analog audio input impedance.
Refer to section 1-9-1.

J1 to J8 : Spaces for inserting the short plugs of J101 to J802 which are not used.

SECTION 2
SERVICE INFORMATION

2-1. MAIN COMPONENTS LOCATION

CARD RACK

F1. PS-183 : PARALLEL/SERIAL CONVERTER
F2. CF-39 : CONCEAL FILTER
F3. VD-04 : VIDEO DECODER (CH-7, 8)
F4. VD-04 : VIDEO DECODER (CH-5, 6)
F5. VD-04 : VIDEO DECODER (CH-3, 4)
F6. VD-04 : VIDEO DECODER (CH-1, 2)
F7. CI-05 : CHANNEL INTERCHANGER
F8. TB-07 : TIME BASE CORRECTOR
F9. VE-18 : VIDEO ENCODER (CH-5, 6, 7, 8)
F10. VE-18 : VIDEO ENCODER (CH-1, 2, 3, 4)
F11. SP-06 : SERIAL/PARALLEL CONVERTER
F12-1. SG-151 : SYNC GENERATER
F12-2. SW-334 : PIGGYBACK BOARD OF SG-151 BOARD
F13. DEC-41 : AUDIO DECODER/ENCODER
F14. PR-115 : AUDIO PROCESSOR & SYSTEM CONTROLLER
F15. DA-28 : AUDIO D/A CONVERTER
F16. AD-38 : AUDIO A/D CONVERTER
F17. ADA-12 : VIDEO A/D, D/A CONVERTER

CONNECTOR PANEL

C1-1. IO-33 : ANALOG AUDIO I/O CONNECTOR (CH-1, 2, 3, 4)
C1-2. IO-33 : ANALOG AUDIO I/O CONNECTOR (CH-5, 6, 7, 8)
C3. IO-34 : DIGITAL AUDIO I/O BUFFER (XLR)
C4. IO-39 : DIGITAL AUDIO I/O BUFFER (D-SUB)
C5. IFA-5 : VTR INTERFACE (AUDIO & SYSTEM) & RS-232C INTERFACE
C6-1. SIF-4 : VTR INTERFACE (VIDEO OUT)
C6-2. PIF-3 : VTR INTERFACE (VIDEO IN)
C7. DIF-1 : DIGITAL VIDEO I/O BUFFER
C8. VM-08 : VIDEO MONITOR/WFM OUTPUT AMPLIFIER
C9. VIO-10 : ANALOG VIDEO I/O BUFFER

OTHERS

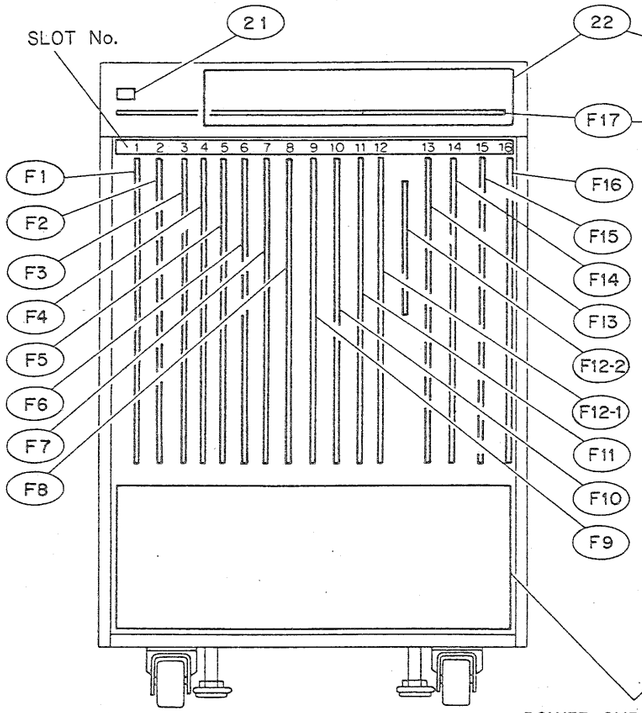
21. PE-18 : POWER LAMP
22. DP-95 : DISPLAY
23. MB-225 : MOTHER BOARD (MAIN)
24. MB-226 : MOTHER BOARD (ADA)
25. SMB-5 : MOTHER BOARD (CN PNL)
26. SMB-2 : MOTHER BOARD (CN PNL)
27. SMB-6 : MOTHER BOARD (CN PNL)

M1 MOTOR, FAN
M2 MOTOR, FAN
M3 MOTOR, FAN

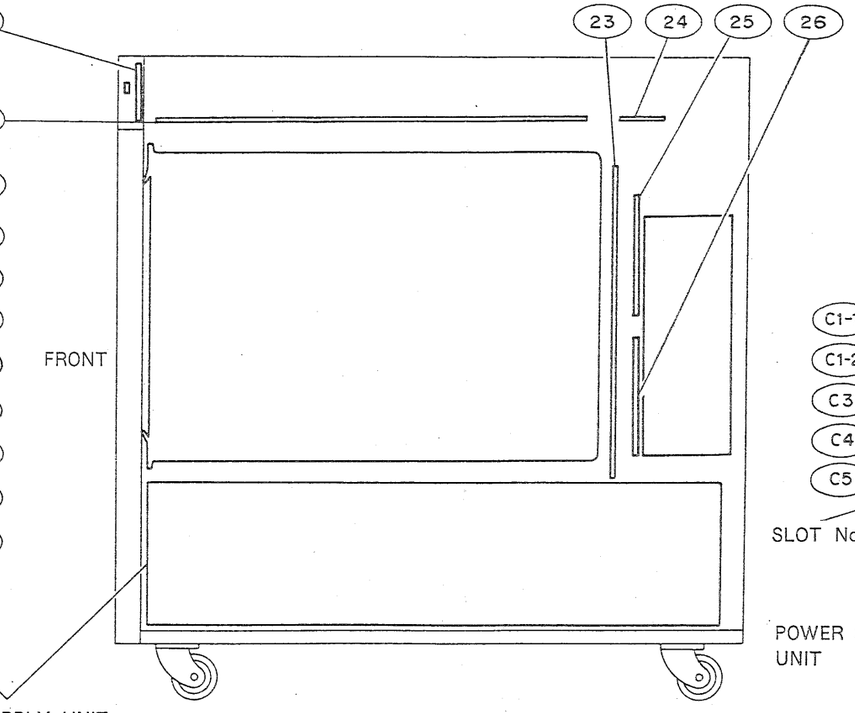
Note : The following boards are possible to be replaced within the following slot number. EX. The VD-04 boards are possible to be replaced within the slot numbers 3 to 6.

ID	BOARD	SLOT, NO
F3 to F6	VD-04	3 to 6
F9, F10	VE-18	9, 10
C1-1, C1-2	IO-33	1

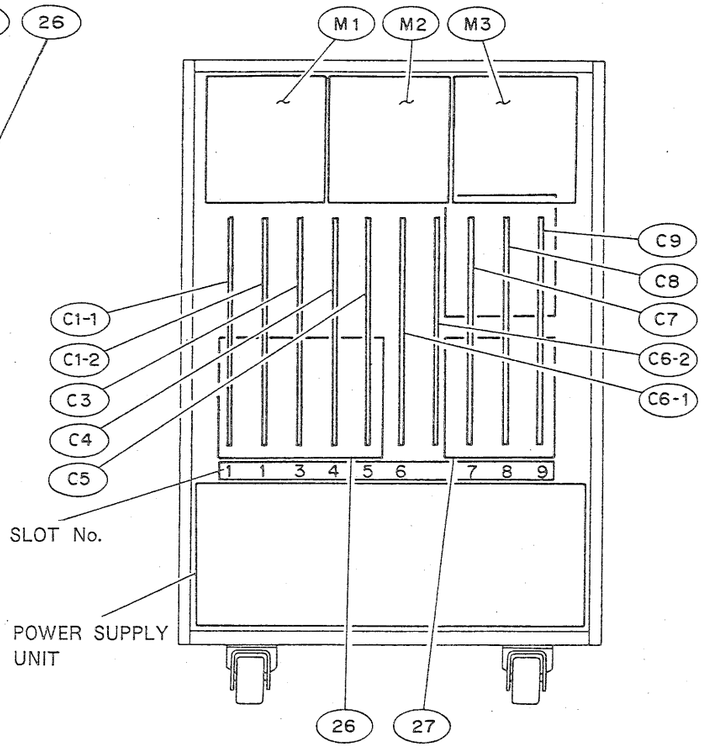
<FRONT VIEW>



<SIDE VIEW>



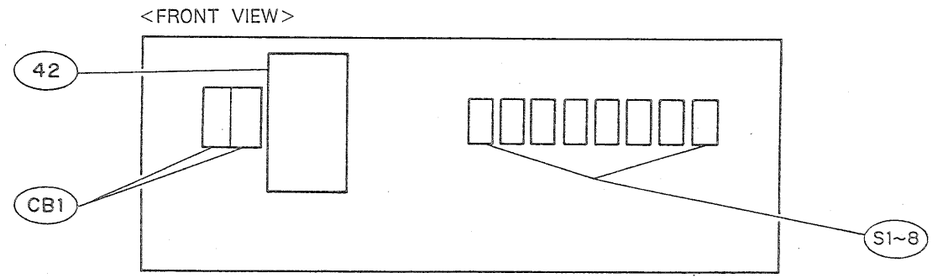
<REAR VIEW>



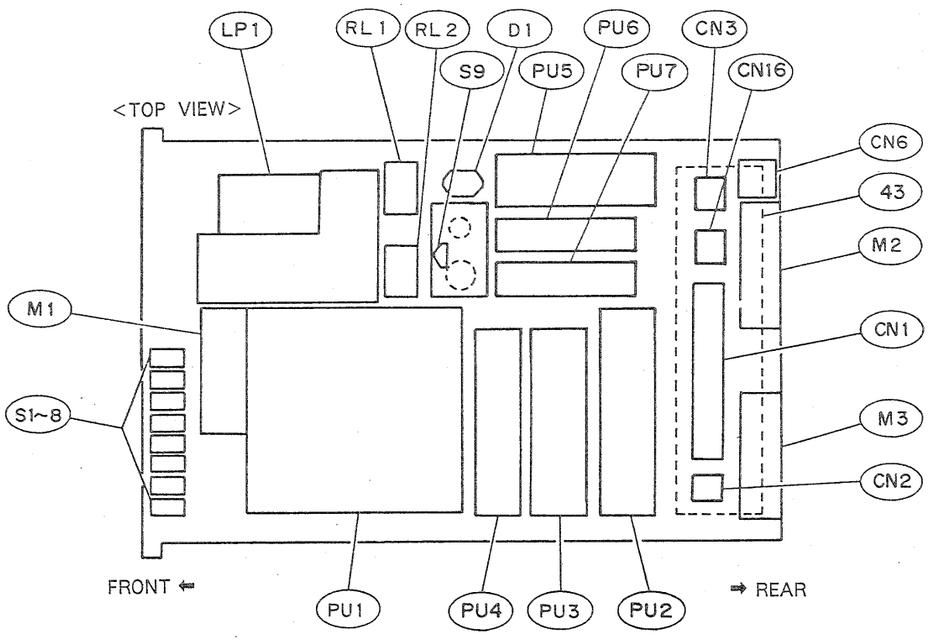
POWER SUPPLY

41.	AC-69 : RUSH CURRENT PROTECTOR	PU1	SWITCHING REG. KE-1000P +5V 1kW
42.	LE-71 : POWER INDICATOR	PU2	SWITCHING REG. EWS180S −5V 180W
43.	TX-13 : POWER SUPPLY RELAYING	PU3	SWITCHING REG. KRV060S −18V 60W
		PU4	SWITCHING REG. KRV060S +18V 60W
CB1	CIRCUIT BREAKER, 250V 20A	PU5	SWITCHING REG. KRV060P +12V 60W
CN1	TERMINAL BOARD, 12P	PU6	SWITCHING REG. KRV030S +12V 30W
CN2	CAP HOUSING, 9P	PU7	SWITCHING REG. KRV030S −12V 30W
CN3	CAP HOUSING, 15P		
CN6	TERMINAL BOARD, 2P	RL1	RELAY, DC12V JH2a-DC12V
CN16	CAP HOUSING, 12P	RL2	RELAY, DC12V JH1a-DC12V
D1	TRIAC, FSM30C4R or FSM30C6R	S1 to 8	SWITCH (VOLTAGE SELECTOR)
LP1	LINE FILTER, LF-215U	S9	SWITCH, THERMAL
M1	MOTOR, FAN		
M2	MOTOR, FAN		
M3	MOTOR, FAN		

<FRONT VIEW>



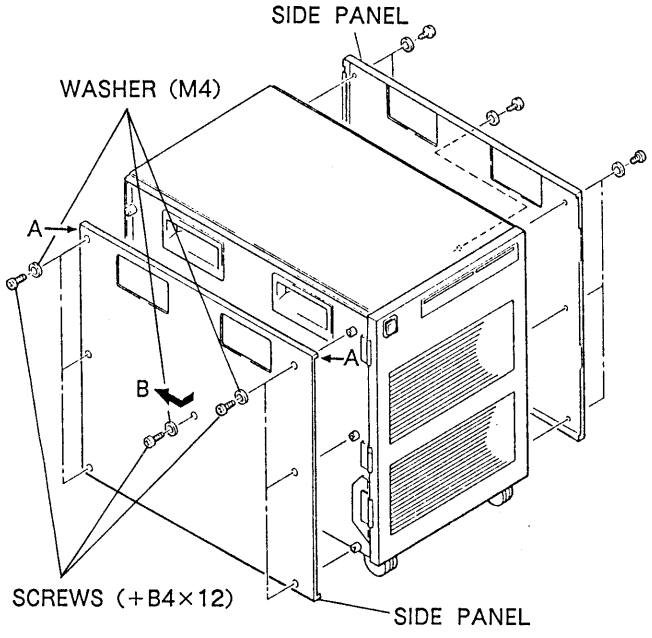
<TOP VIEW>



2-2. CABINET REMOVAL

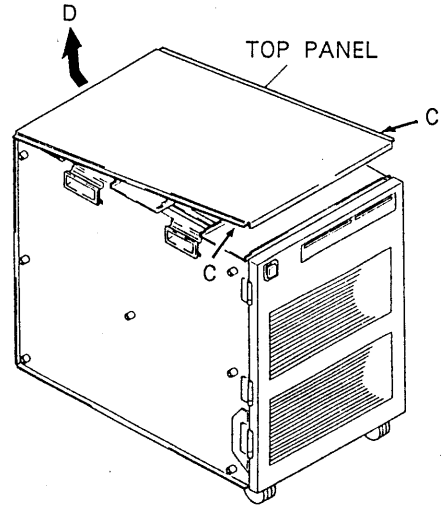
SIDE PANELS REMOVAL

1. Unscrew the seven screws (+B4×12) and seven washers (M4) from each side panel.
2. Hold the part indicated by arrow A, then pull it in direction B and remove it.



TOP PANEL REMOVAL

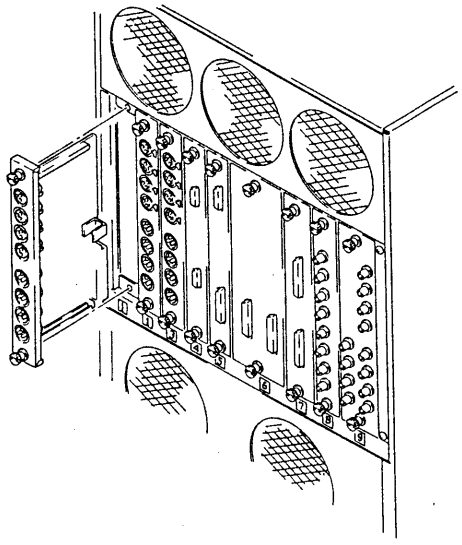
1. Remove the left and right side panels.
   Note : The top panel is held in place by the left and right panels.
2. Hold the part indicated by arrow C, then lift it in direction D.



CONNECTOR PANELS [1] TO [7] REMOVAL

Loosen the screws (two face screws) sufficiently, then pull out the panels to the front.

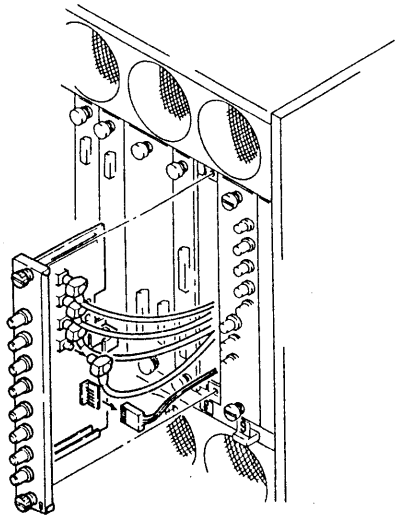
Note : The face screws have a design which makes it impossible for them to be removed discretely. This design prevents them falling inside the unit.



CONNECTOR PANELS [8] AND [9] REMOVAL

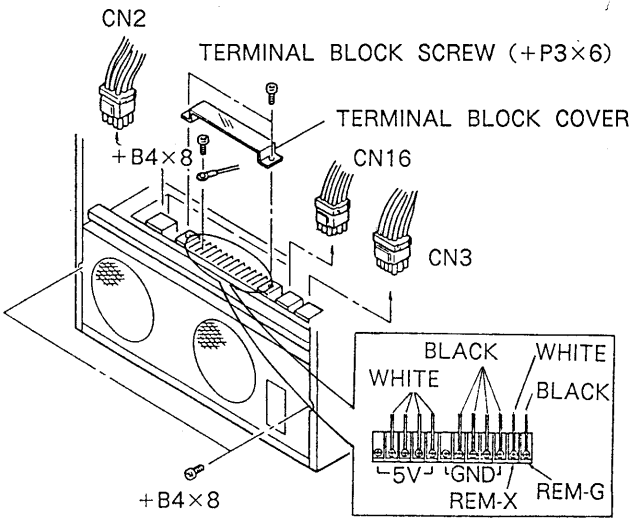
1. Loosen the screws (two face screws) sufficiently, then pull out the panels to the front.
2. Disconnect all connectors from the printed circuit board.

Note : The face screws have a design which makes it impossible for them to be removed discretely. This design prevents them falling inside the unit.

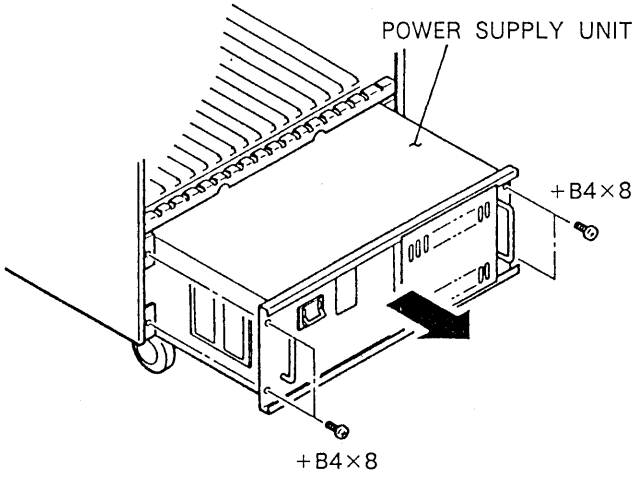


POWER SUPPLY UNIT REMOVAL

1. Remove the terminal block cover and also CN2, CN16, and CN3.
2. Disconnect the wires from the terminal block.
3. Remove the two screws (at rear) fixing the power supply unit.



4. Remove the four screws (marked by ↟) on the front of the power supply unit, then grasp the handles and pull out the power supply unit in the direction of the arrow.



Note :

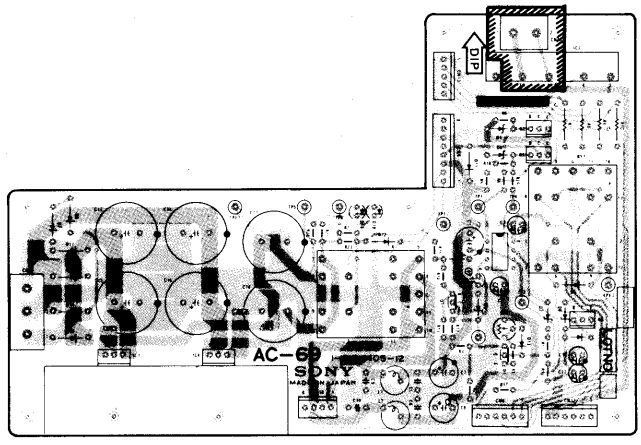
1. The weight of the power supply unit is approximately 30 kg. Be careful to pull it out.
2. Pull out the AC code with the unit.

2-3. POWER SUPPLY SECTION PRECAUTIONS

2-3-1. Primary Circuit & Electric Shock

The power supply unit consists of the AC-69, LE-71 and TX-13 boards, various switching regulators, and peripheral components on the primary side. It is contained entirely in a single case.
The shaded part of the AC-69 board is the primary side. Take great care never to touch the shaded part of the AC-69 board, the power relay, voltage selector or the primary side of the various switching regulators. This is because of the danger of electric shock.

AC-69 Board (Component Side)



2-3-2. Power Supply Board Removal

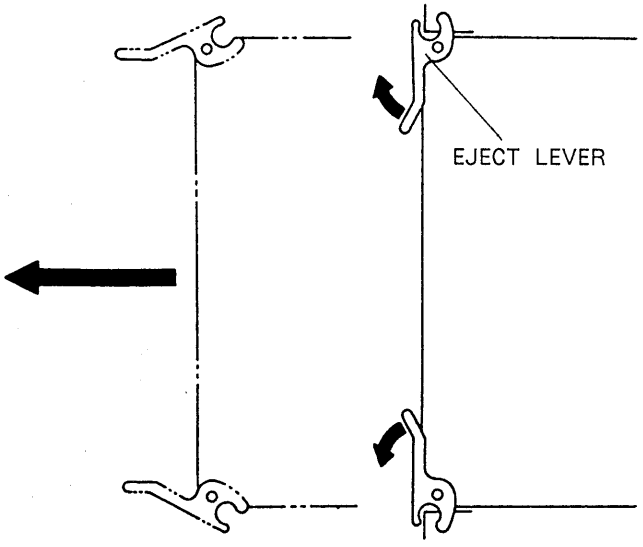
Before inspecting or adjusting the AC-69, LE-71 or TX-13 board in the power supply unit, refer to "POWER BLOCK ASSEMBLY" in chapter D, and then remove the board concerned.

2-4. PLUG-IN BOARDS PULLING OUT/ INSERTION

Note : After turning the power off, then pull out or insert the plug-in board.

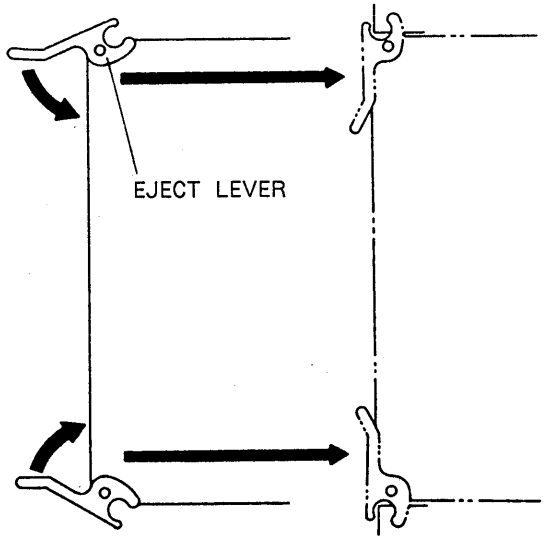
Plug-in boards pulling out

Pull up the eject levers on the board in the direction of the arrow for disconnecting the plug-in board from the connectors on the mother boards. Then, pull out the boards.



Plug-in boards insertion

Insert the boards while pulling up the eject levers. Then, firmly press the eject levers in the direction of the arrow for connecting the plug-in board to the connectors on the mother boards.



2-5. NOTES ON REPAIR PARTS

2-5-1. Notes on Repair Parts

(1) Safety Related Components Warning

Components marked with ⚠ on the schematic diagrams, exploded views and electrical spare parts list are critical to safe operation. Replace these components with Sony parts whose part numbers appear in this manual or in service bulletins and service manual supplements published by Sony.

(2) Standardization of Parts

Repair parts supplied from Sony Parts Center may not be always identical with the parts which actually in use due to "accommodating the improved parts and/or engineering changes" or "standardization of genuine parts". This manual's exploded views and electrical spare parts list are indicating the part numbers of "the standardized genuine parts at present".

(3) Change of Parts

Regarding engineering parts changes, refer to Section E. "CHANGED PARTS".

(4) Stock of Parts

Parts marked with "o" SP (Supply Code) column of the spare parts list are not normally required for routine service work. Orders for parts marked with "o" will be processed, but allow for additional delivery time.

(5) Units for Capacitors, Inductors and Resistors

The following units are assumed in schematic diagrams, electrical parts list and exploded views unless otherwise specified.

Capacitors : μF
Inductors : μH
Resistors : Ω

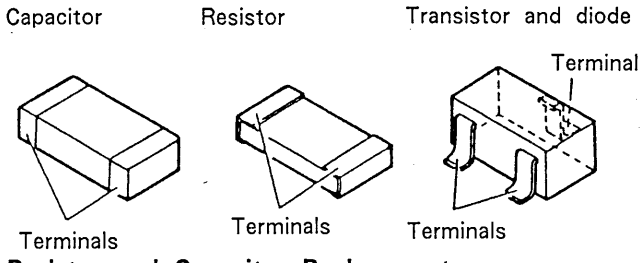
2-5-2. Replacement Procedure of Chip Parts

Required Tools

Soldering iron 20W ;
If possible, use the soldering iron tip heat-controller at 270±10℃.
Braided wire ;
SOLDER TAUL or equivalent
Sony part No. 7-641-300-81
Tweezers

Soldering Conditions

Soldering iron temperature ;
270±10℃
Soldering time ;
Less than two seconds per a pin



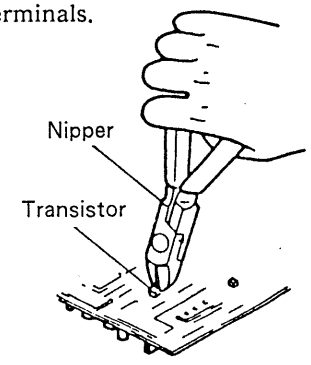
Resistor and Capacitor Replacement

1. Place the soldering iron tip onto the chip part and heat it up until the solder is melted. When the solder is melted, slide the chip part aside.
2. Make sure that there is no pattern peeling, damage and/or bridge around the desoldering positions.
3. After removing the chip part, presolder the area, in which the new chip part is to be placed, with a thin layer of solder.
4. Place new chip part in the desired position and solder both ends.

Note : Never use the chip part again once it has been removed.

Transistor and Diode Replacement

1. Cut the terminals of the chip part with nippers.
2. Remove the leads cut as above.
3. Make sure that there is no pattern peeling, damage and/or bridge around the desoldering positions.
4. After removing the chip part, presolder the area, in which the new chip part is to be placed, with a thin layer of solder.
5. Place new chip part in the desired position and solder the terminals.



IC Replacement

1. Using the braided wire, "SOLDER TAUL" Sony Part No. 7-641-300-81, remove the solder around the pins of the IC-chip to be removed.
2. While heating up the pins, remove the pins one by one using sharp-pointed tweezers.
3. Make sure that there is no pattern peeling, damage and/or bridge around the desoldering positions.
4. After removing the chip part, presolder the area, in which the new chip part is to be placed, with a thin layer of solder.
5. Place new chip part in the desired position and solder the pins.

2-5-3. Method of Replacing the Backup Battery

The PR-115 has a RAM backup battery. When this battery reaches the end of its life, the error message "PR BATT" will be displayed on the function control panel of the HDD-1000. The normal life of the battery is two years (guaranteed life). When the "PR BATT" message appears, replace the battery within seven days. (If you allow the battery to run down completely, the set mode will be completely erased.)

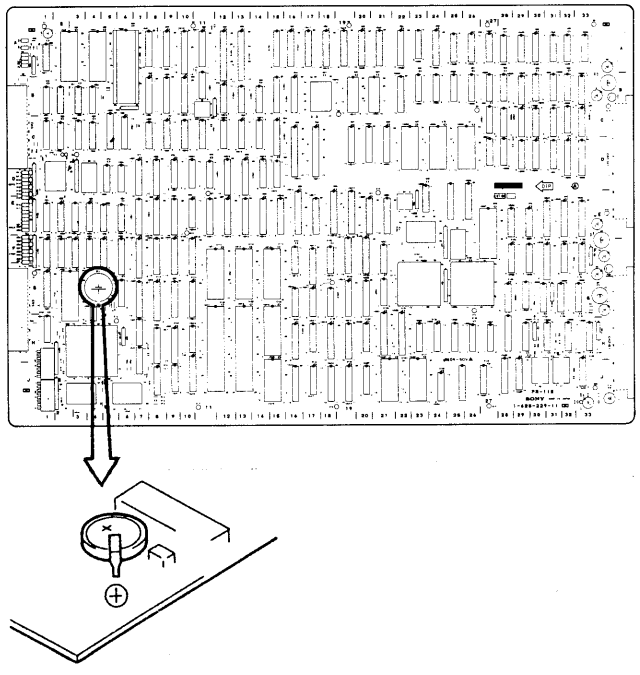
Backup battery : Lithium battery
Sony part No. : 1-528-218-12

Replacement Method

1. Switch OFF the HDD-1000 and the HDDP-1000.
2. Remove the PR-115 board (see section 2-4), and replace the battery with a new one.

Note : When installing the new battery, solder it as shown below.

PR-115 Board (Component Side)



3. Install the PR-115 board, then switch ON the HDD-1000 and HDDP-1000.
4. The error message "PR BATT" will appear on the function control panel of the HDD-1000. Switch the HDDP-1000 OFF then ON again, and confirm that the error message disappears.

Note : If the error message does not disappear after a new battery has been installed, the battery is either making faulty contact or may have already reached the end of its life. Check the battery in this case.

2-6. PERIODIC CHECK AND MAINTENANCE

The periodic check and maintenance are recommended to be performed in order to maintain performance and longer life of the unit.
For details, see the maintenance manual of HDD-1000 (Vol-1), section 5.

2-7. MAINTENANCE TOOLS AND EQUIPMENTS

When checking or repairing the unit, the maintenance tools and equipments are used.
For details, see the maintenance manual of HDD-1000 (Vol-1), section 2-7.

SECTION 3
DIAGNOSIS FUNCTION

3-1. GENERAL

The HDDP-1000 is a signal processor comprising the HD digital VTR system in combination with the HDD-1000 HD digital videocorder.
Setting up of the processor can usually be done by the menu system from the function control panel of the VTR using the 21 keys.
However, when using the processor alone, it is necessary to set it up independently.
This is achieved by selecting the switches on the printed circuit boards in the processor instead of setting up by the menu system on the VTR.
For details of how to set up the processor by selecting the switches on the printed circuit boards of the processor, see Section 3-5 Setting Up Controlled from both VTR & Processor.

3-2. ERROR MESSAGES

If an error occurs after turning the power on or during operation, the error in the processor is indicated by one or all of the following three ways :

- The error message is displayed on the function control panel of the VTR.
- The red indicator of the alarm lamps in the processor lights up.
- The indicator mounted on the boards in the processor corresponding to the error lights up.

The error message, which is displayed on the function control panel of the VTR, can be superimposed on the TV monitor by the menu setting of the VTR (S59. MIXED CHARA OUTPUT). For details of the menu setting of the VTR, see the operation manual for the HDD-1000, Section 1-4 Menu.
The error messages, alarm lamps and indicators on the boards of the processor, and the cause of the errors are as follows.

1. Error messages and the cause of the error which is displayed on the function control panel of the VTR

AD38 BD : The AD-38 board in the processor is not securely inserted, or the bus-interface of the board or the interface between the VTR and processor is defective.

ADA12 BD : The ADA-12 board in the processor is not securely inserted, or the bus-interface of the board or the interface between the VTR and processor is defective.

ADA12 SW : The LOCAL/REMOTE select switch (S1-8/ADA-12 board) in the processor is set to ON. When this message is displayed, set to OFF.

CF39 BD : The CF-39 board in the processor is not securely inserted, or the bus-interface of the board or the interface between the VTR and processor is defective.

CI05 BD : The CI-05 board in the processor is not securely inserted, or the bus-interface of the board or the interface between the VTR and processor is defective.

CI05 SW : The TEST ON/OFF switch (S2-8/CI-05 board) in the processor is set to ON. When this message is displayed, set to OFF.

COM REF : The reference signals for video and audio recording and for playback are not input. Select the correct reference signal with one of the menus of the VTR (S12 COMMON REF SELECT, and I80 INPUT ANALOG/DIGITAL), or the COM REFERENCE SELECT switch (S3-2/SG-151 board), ANALOG REFERENCE SELECT switch (S3-4/SG-151 board) or ANALOG/DIGITAL INPUT SELECT switch (S3-7/SG-151 board).
For details, see Section 3-5-2 Selection of the Video Input/Output Signal.

COM REF* : The frequency of the reference signals for the video and audio recording and for playback is incorrect. Select the correct input frequency with either the REF SYNC SELECT switch (S6/SG-151 board) or video input/output signal selection (see Section 3-5-2 Selection of the Video Input/Output Signal).

DA28 BD : The DA-28 board in the processor is not securely inserted, or the bus-interface of the board or the interface between the VTR and processor is defective.

DEC41 BD : The DEC-41 board in the processor is not securely inserted, or the bus-interface of the board or the interface between the VTR and processor is defective.

DEC41 SW : The NORM / TEST switch (SW2 / DEC-41 board) in the processor is set to TEST (1 to F). When this message is displayed, set to 0.

DP95 BD : The DP-95 board in the processor is not securely inserted, or the bus-interface of the board or the interface between the VTR and processor is defective.

IO33 BD : The IO-33, IO-34, IO-39 or IFA-5 board in the processor is not securely inserted, or the bus-interface of the board or the interface between the VTR and processor is defective.

PIF3 BD : The PIF-3 board in the processor is not securely inserted, or the bus-interface of the board or the interface between the VTR and processor is defective.

PR115 BD : The PR-115 board in the processor is not securely inserted, or the bus-interface of the board or the interface between the VTR and processor is defective.

PR115 SW : The AUDIO VTR CONTROL INHIBIT switch (S6-1/PR-115 board) and/or the VIDEO SYSTEM BOARDS MODE SELECT switch (S7-7/PR-115 board) are set to ON. When this message is displayed, set to OFF.

PR BATT : The battery voltage on the PR-115 board in the processor is below the reference level. See Section 2-5-3 Method for Replacing the Backup Battery.

PROC I/F : The interface between the VTR and processor or the VTR-processor connecting cable is defective.

PRO REF : The reference signal for video playback is not input. Select the correct reference signal from the menu of the VTR (S12 COMMON REF SELECT, I80 INPUT ANALOG/DIGITAL and I82 PROC PB REF SELECT), the PROC REFERENCE SELECT switch (S3-1/SG-151 board) or the ANALOG REFERENCE SELECT switch (S3-4/SG-151 board) or the ANALOG / DIGITAL INPUT SELECT switch (S3-7/SG-151 board). For details, see Section 3-5-2 Selection of the Video Input/Output Signal.

PRO REF* : The input frequency of the reference signal for video playback is incorrect. Select the correct input frequency of the reference signal with either the REF SYNC SELECT switch (S6 / SG-151 board) or the video input/output signal selection (see Section 3-5-2 Selection of the Video Input/Output Signal).

PS183 BD : The PS-183 board in the processor is not securely inserted, or the bus-interface of the board or the interface between the VTR and processor is defective.

SG151 BD : The SG-151 board in the processor is not securely inserted, or the bus-interface of the board or the interface between the VTR and processor is defective.

SG151 SW : The TEST ON/OFF switch (S3-8/SG-151 board) in the processor is set to ON. When this message is displayed, set to OFF.

SIF4 BD : The SIF-4 board in the processor is not securely inserted, or the bus-interface of the board or the interface between the VTR and processor is defective.

SP06 BD : The SP-06 board in the processor is not securely inserted, or the bus-interface of the board or the interface between the VTR and processor is defective.

TB07 BD : The TB-07 board in the processor is not securely inserted, or the bus-interface of the board or the interface between the VTR and processor is defective.

VD04 BD : The VD-04 board in the processor is not securely inserted, or the bus-interface of the board or the interface between the VTR and processor is defective.

VE18 BD : The VE-18 board in the processor is not securely inserted, or the bus-interface of the board or the interface between the VTR and processor is defective.

2. Red indicator of the alarm lamps in the processor and the cause of error

SYSTEM Indicator

- Interface between the VTR and processor is defective.
- Board-to-board interface in the processor is defective.
- Read/write error of the memory in the CPU has occurred.
- An error is detected in the diagnosis function which is executed after turning the power on.
- Overheating in the power unit of the processor has occurred. In this case, the red indicator blinks and an alarm sounds simultaneously.

TEST MODE Indicator

When the red TEST MODE indicator lights up, one or more of the following switches has been set to ON. Set to OFF.

- Both S7-7 and S7-8 on the PR-115 board
- S2-8 on the CI-05 board
- S3-8 on the SG-151 board
- S1-8 on the ADA-12 board

In addition to these switches, SW2 on the DEC-41 board could have set to TEST (1 to F). Set to 0.

ERROR RATE VIDEO Indicator

When the red ERROR RATE VIDEO indicator lights up, the error rate of the video data exceeds the allowable range. Adjust the tracking with the TRACKING control on the front panel of the VTR.

ERROR RATE AUDIO Indicator

When the red ERROR RATE AUDIO indicator lights up, the error rate of the audio data exceeds the allowable range. The audio might be muted.

AUDIO ASYNCH Indicator

When the red AUDIO ASYNCH indicator lights up, the audio input signals are not synchronized with the video signal, or their sampling frequency is not 48 kHz. Input a digital audio signal that is synchronized with the video signal whose frequency is 60 Hz.

3. The colored indicators on the boards in the processor and the cause of error

PS-183 Board

D1 : ALARM Indicator (red)
- When this light is on, the circuit operation of the PS-183 board is defective.

D2 : LOCAL Indicator (green)
- When this light is on, the PR-115 board is not securely inserted.
- When this light is on, the VIDEO SYSTEM BOARDS MODE SELECT switch (S7-7/PR-115 board) may be set to ON. Set to OFF.
- When this light is on, only the processor power may be turned on, while the power to both the VTR and processor may be off.

CF-39 Board

D1 : ALARM Indicator (red)
- When this light is on, the circuit operation of the CF-39 board is defective.

D2 : LOCAL Indicator (green)
- When this light is on, the PR-115 board is not securely inserted.
- When this light is on, the VIDEO SYSTEM BOARDS MODE SELECT switch (S7-7/PR-115 board) may be set to ON. Set to OFF.
- When this light is on, only the processor power may be turned on, while the power to both the VTR and processor may be off.

D3 : CONCEAL Indicator (green)
- When this light is on, the circuit for error concealment is active.

D4 : FLAG Indicator (yellow)
- When this light is on, the picture for error flag monitoring is output from the digital/analog video output connectors and the monitor output connectors. The error can be seen as a white dot on the TV monitor. To select the output of either the picture for error flag monitoring or the normal picture, use the FLAG switch (S6/CF-39 board).

VD-04 Board

D1 : ALARM Indicator (red)
- When this light is on, the circuit operation of the VD-04 board is defective.

D2 : LOCAL Indicator (green)
- When this light is on, the PR-115 board is not securely inserted.
- When this light is on, the VIDEO SYSTEM BOARDS MODE SELECT switch (S7-7/PR-115 board) may be set to ON. Set to OFF.
- When this light is on, only the processor power may be turned on, while the power to both the VTR and processor may be off.

D3 : INNER (inner correction) Indicator (green)
- When this light is on, the inner correction circuit is active. It does not light up when the circuit is only detecting an error. Use the menu T08. INNER CORRECTION ON/OFF of the VTR or the ERROR CORRECT switch (S4/CF-39 board) switches the inner correction circuit on or off.

D4 : OUTER (outer correction) Indicator (green)
- When this light is on, the outer correction circuit is active. It does not light up when the circuit is only detecting an error. Use the menu T09. OUTER CORRECTION ON/OFF of the VTR or the ERROR CORRECT switch (S4/CF-39 board) switches the inner correction circuit on or off.

D5 : ERROR (A) Indicator (yellow)

D6 : ERROR (B) Indicator (yellow)
- When either or both of these lights is on, the error of the video signal from the video heads is concealed without correcting in the error correct.

CI-05 Board

D1 : ALARM Indicator (red)
- When this light is on, the circuit operation of the CI-05 board is defective.
- When this light is on, the TEST ON/OFF switch (S2-8/CI-05 board) may be set to ON. Set to OFF.

TB-07 Board

D1 : ALARM Indicator (red)
- When this light is on, the circuit operation of the TB-07 board is defective.

VE-18 Board

D1 : ALARM Indicator (red)
- When this light is on, the circuit operation of the VE-18 board is defective.

D2 : LOCAL Indicator (green)
- When this light is on, the PR-115 board is not securely inserted.
- When this light is on, the VIDEO SYSTEM BOARDS MODE SELECT switch (S7-7/PR-115 board) may be set to ON. Set to OFF.
- When this light is on, only the processor power may be turned ON, while the power to both the VTR and processor may be off.

SP-06 Board

D1 : ALARM Indicator (red)

- When this light is on, the circuit operation of the SP-06 board is defective.

D2 : LOCAL Indicator (green)

- When this light is on, the PR-115 board is not securely inserted.
- When this light is on, the VIDEO SYSTEM BOARDS MODE SELECT switch (S7-7/PR-115 board) may be set to ON. Set to OFF.
- When this light is on, only the processor power may be turned ON, while the power to both the VTR and processor may be off.

SG-151 Board

D1 : ALARM Indicator (red)

- When this light is on, the circuit operation of the SG-151 board is defective.
- When this light is on, the TEST ON/OFF switch (S2-8/CI-05 board) may be set to ON. Set to OFF.

DEC-41 Board

D1 : CH-1 CRC ERR (CRCC error) Indicator (red)
D2 : CH-2 CRC ERR (CRCC error) Indicator (red)
D3 : CH-3 CRC ERR (CRCC error) Indicator (red)
D4 : CH-4 CRC ERR (CRCC error) Indicator (red)
D5 : CH-5 CRC ERR (CRCC error) Indicator (red)
D6 : CH-6 CRC ERR (CRCC error) Indicator (red)
D7 : CH-7 CRC ERR (CRCC error) Indicator (red)
D8 : CH-8 CRC ERR (CRCC error) Indicator (red)

- When any or all of these lights are on, a CRCC error is detected in the audio data playing back from the digital audio track.
  CRCC : cyclic redundancy check code

PR-115 Board

D8 : CH-1 MUTE Indicator (red)
D9 : CH-2 MUTE Indicator (red)
D10 : CH-3 MUTE Indicator (red)
D11 : CH-4 MUTE Indicator (red)
D12 : CH-5 MUTE Indicator (red)
D13 : CH-6 MUTE Indicator (red)
D14 : CH-7 MUTE Indicator (red)
D15 : CH-8 MUTE Indicator (red)

- When any or all of these lights are on, the audio signal is muted due to excessive uncorrected error of the audio playback signal or the system requires audio signal muting.

D16 : CH-1 HOLD Indicator (yellow)
D17 : CH-2 HOLD Indicator (yellow)
D18 : CH-3 HOLD Indicator (yellow)
D19 : CH-4 HOLD Indicator (yellow)
D20 : CH-5 HOLD Indicator (yellow)
D21 : CH-6 HOLD Indicator (yellow)
D22 : CH-7 HOLD Indicator (yellow)
D23 : CH-8 HOLD Indicator (yellow)

- When any or all of these lights are on, the audio playback error data, which could not be corrected, is replaced with one sample of preceding data.

D24 : CH-1 AVER Indicator (green)
D25 : CH-2 AVER Indicator (green)
D26 : CH-3 AVER Indicator (green)
D27 : CH-4 AVER Indicator (green)
D28 : CH-5 AVER Indicator (green)
D29 : CH-6 AVER Indicator (green)
D30 : CH-7 AVER Indicator (green)
D31 : CH-8 AVER Indicator (green)

- When any or all of these lights are on, the audio playback error data, which could not be corrected, is interpolated by the average value of the preceding and succeeding data..

3-3. SWITCH SETTINGS IN THE DIAGNOSING AND SETTING UP MODES

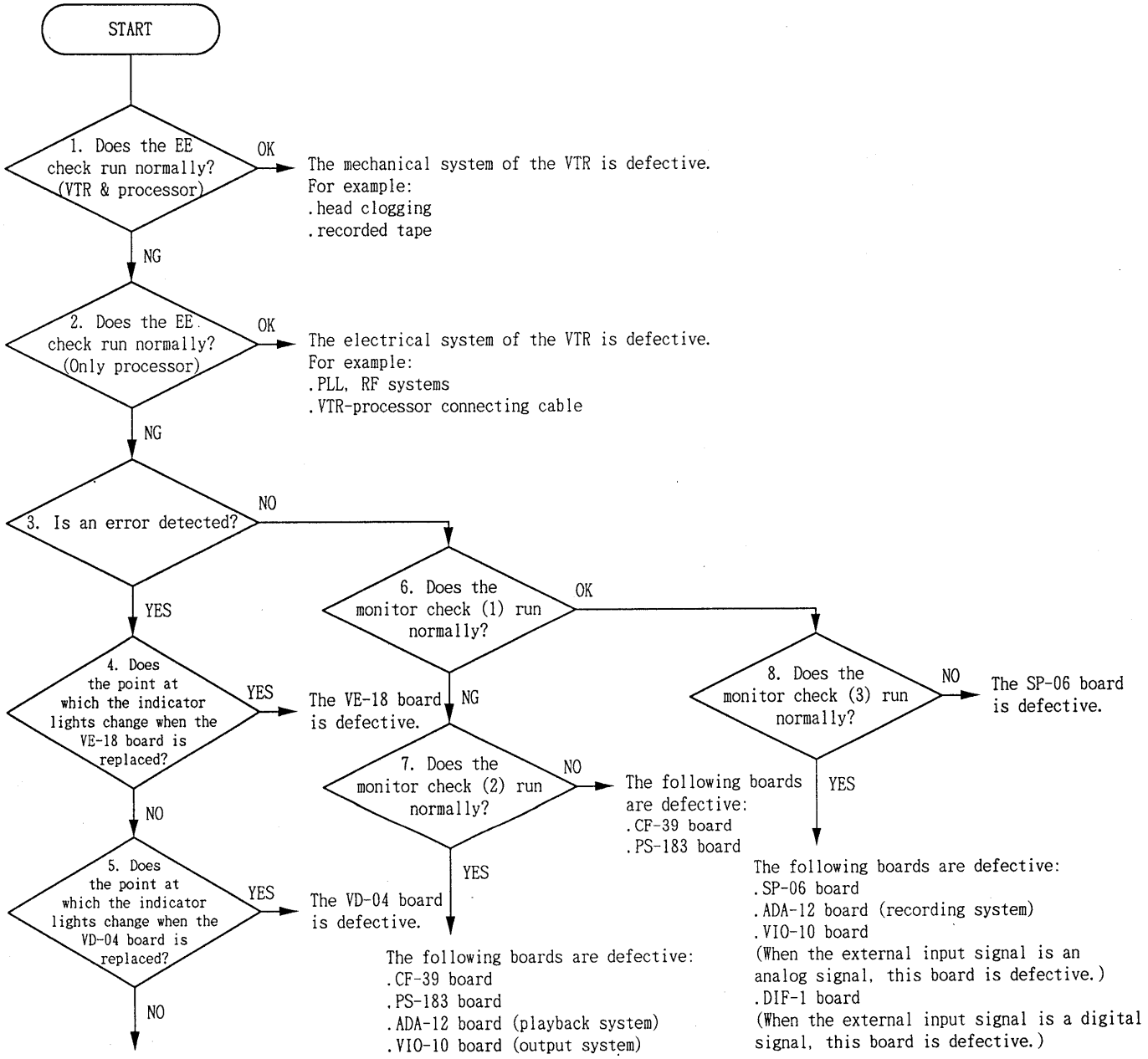
When diagnosing and setting up, set each switch/jumper on the boards in the processor to the same position at that of initial factory setting. (For details, see Section 1-9 Switch/Jumper Settings.)
In the following sections, switch settings which must be changed for only performing this program are explained.
After diagnosing and setting up, reset each switch whose setting has been changed to the original position. If not, other diagnosing and setting up might be effected, so the processor might not operate normally.
In addition, after diagnosing and setting up, reset the switches again according to that operating conditions.

3-4. DIAGNOSIS FUNCTION

3-4-1. Detecting the Cause of an Error in the Video Signal System

Basic knowledge

(1) When an error occurs in the video signal system (for example, the error rate exceeds the allowable range, or the normal picture is not output), the cause of error or the location where the error occurs can be located.



(2) Set the following switches to as follows :
S7-7/PR-115 board : VIDEO SYSTEM BOARDS MODE SELECT switch···ON
S4/CF-39 board : ERROR CORRECT (error correction circuits) switch .....OFF
After diagnosing, reset them to the original positions.

(3) Before detecting the cause of error, play back the alignment tape, and check whether the error occurs in the playback system or recording system. Then, step 5 can be easily detected.
When the error occurs in the recording system, it can be played back normally. When the error occurs in the playback system, it cannot be played back normally.

(4) When detecting the cause of error, use the color-bar signal as an external test signal.

Detailed Explanation of the Cause of Error

1. Does the EE check run normally? (VTR and processor)

Connect the processor to the VTR using the VTR-processor connecting cable, and turn on the power to both the VTR and processor.
In this case, when both the picture is output normally and neither the ERROR (A) indicator (D5/VD-04 board) nor the ERROR (B) indicator (D6/VD-04 board) of slot numbers 3 to 6 (two indicators on each VD-04 board, for a total of eight indicators) lights up, the mechanical system of the VTR is defective (for example, head clogging, or the recorded tape).
In either or both of the following cases, perform step 2.

- The picture is not output normally.
- Either or both the ERROR (A) indicator (D5/VD-04 board) and the ERROR (B) indicator (D6/VD-04 board) lights up.

2. Does the EE check run normally? (only processor)

Turn off the power to the processor, and set the following switches to ON :
S7-8/PR-115 board :
CI-05 BOARD MODE SELECT switch
S1-1/CF-39 board :
CHANNEL DE-INTERLEAVE OFF switch
S4-1/SP-06 board :
CHANNEL INTERLEAVE OFF switch
In this case, when both the picture is output normally and neither the ERROR (A) indicator (D5/VD-04 board) nor the ERROR (B) indicator (D6/VD-04 board) of slot numbers 3 to 6 (two indicators on each VD-04 board, giving a total of eight indicators) lights up, the electrical system of the VTR is defective (for example, PLL and RF systems, VTR-processor connecting cable).
In either or both of the following cases, perform step 3.

- The picture is not output normally.
- Either or both the ERROR (A) indicator (D5/VD-04 board) and the ERROR (B) indicator (D6/VD-04 board) lights up.

3. Is an error detected?

In step 3, check whether an error is detected on the monitor by operating the error correction circuit.
If an error is detected, either the ERROR (A) indicator (D5/VD-04 board) or the ERROR (B) indicator (D6/VD-04 board) of slot numbers 3 to 6 (two indicators on each VD-04 board, giving a total of eight indicators) lights up. Then, the video channel in which the error is occurring can be detected by the places where the ERROR (A) indicator or the ERROR (B) indicator lights up.
The relationship of the video channels and the indicators is as follows :

Slot No.	3		4		5		6	
Indicator which detects the error	D5	D6	D5	D6	D5	D6	D5	D6
Video channel	CH-7	CH-8	CH-5	CH-6	CH-3	CH-4	CH-1	CH-2

When either the ERROR (A) indicator or the ERROR (B) indicator lights up (that is, thte error is detected), perform step 4. When neither of the indicators light up (that is, the error is not detected), perform step 6.

4. Does the point at which the indicator lights change when the VE-18 board is replaced?

In step 4, change over the VE-18 board in slots number 9 and number 10. The VE-18 boards are video encoders ; The board if slot number 9 corresponds to channels 5 to 8, and that in slot number 10 corresponds to channels 1 to 4.
After changing over the VE-18 boards, the ERROR (A) and/or ERROR (B) indicators on the VD-04 board corresponding to the channels in which an error was detected in step 3 go out, and the ERROR (A) indicator and/or ERROR (B) indicators corresponding to the other channels light. This is considered to be due to a defect in the VE-18 board that processes the channel corresponding to the indicator which lights after the VE-18 boards are changed over.
For example, assume that the indicators on the VD-04 board in slot number 3 corresponding to channels 7 and 8 in step 3 are lit.
After VE-18 boards are changed over, the indicators on the VD-04 board in slot number 3 go out, and the indicators on the VD-04 board in slot number 5 corresponding to channels 3 and 4 light.
This is considered to be due to a defect in the VE-18 board in number 10 slot which processes channels 3 and 4 after the VE-18 boards are changed over. (In other words, it is considered that the VE-18 boards were changed over.)
The slot number of the board corresponding to the indicator that lights as a result of changing over the VE-18 boards and the slot number of the defective VE-18 board are shown in the table below. If the position at which the indicator lights does not move when the VE-18 board is changed over, perform step 5.

5. Does the point at which the indicator lights change when the VD-04 board is replaced?

In step 5, change over the VD-04 board corresponding to the ERROR (A) and/or ERROR (B) indicator that lights in step 4 with the VD-04 board on which none of the indicators light, and check whether or not the slot number of the VD-04 board on which the indicators light changes over.
If the slot number of the VD-04 board on which the indicators light changes over, it is considered that the VD-04 board on which the indicators lit after the boards were changed over is defective.
If the slot number corresponding to the indicator that lights does not change over when the boards are changed over, it is considered that one of the TB-07, CI-05, SIF-4 and PIF-3 boards is defective.
This does not apply, however, if a defect occurs in the playback system as described in Basic Knowledge (3) and the SIF-4 board is not defective.

6. Does the monitor check (1) run normally?

Set the SG (test signal) switch (S1/SP-06 board) to ON. Perform the monitor check using the internal test signal of the processor.
If an error cannot be observed on the monitor and the picture appears normally, perform step 8. If not, perform step 7.

Slot no. in which D5 & D6 light up in step 3	Slot no. in which D5 & D6 light up by changing VE board	Slot no. in which the defective VE-18 board is inserted (after changing the VE board)
Slot no. 3	Slot no. 5	VE-18 board in slot no. 10 (*1)
Slot no. 4	Slot no. 6	VE-18 board in slot no. 10 (*1)
Slot no. 5	Slot no. 3	VE-18 board in slot no. 9 (*2)
Slot no. 6	Slot no. 4	VE-18 board in slot no. 9 (*2)

(*1) Before changing the VE-18 boards, this VE-18 board should be inserted into slot number 9.
(*2) Before changing the VE-18 boards, this VE-18 board should be inserted into slot number 10.

7. Does the monitor check (2) run normally?

Set the SG (test signal) switch (S1/SP-06 board) to OFF. Perform the monitor check using the external test signal.
Divide the monitor screen into four blocks as shown in Fig. 1. If the error cannot be observed on all four blocks (that is, the error appears on one, two or three blocks among the four), either the CF-39 or PS-183 board is defective.
If the error can be observed on all four blocks (that is, it appears on the whole monitor screen), one of the CF-39, PS-183, ADA-12 (playback system) or VIO-10 boards (output system) is defective.

8. Does the monitor check (3) run normally?

Set the SG (test signal) switch (S1/SP-06 board) to OFF. Perform the monitor check using the external test signal.
Divide the monitor screen into four blocks as shown in Fig. 1. If the error cannot be observed on all four blocks (that is, the error appears on one, two or three blocks among the four), the SP-06 board is defective.
If the error can be observed on all four blocks (that is, it appears on the whole monitor screen), one of the SP-06, ADA-12 (recording system), VIO-10 (input system for the external analog test signal), or DIF-1 boards (external digital test signal) is defective.

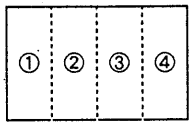


Fig. 1

3-4-2. Detecting the Cause of an Error in the Audio Signal System

When an error occurs in the audio signal system (for example, noisy or the audio output is muted), the cause of error or the location where the error occurs can be located.

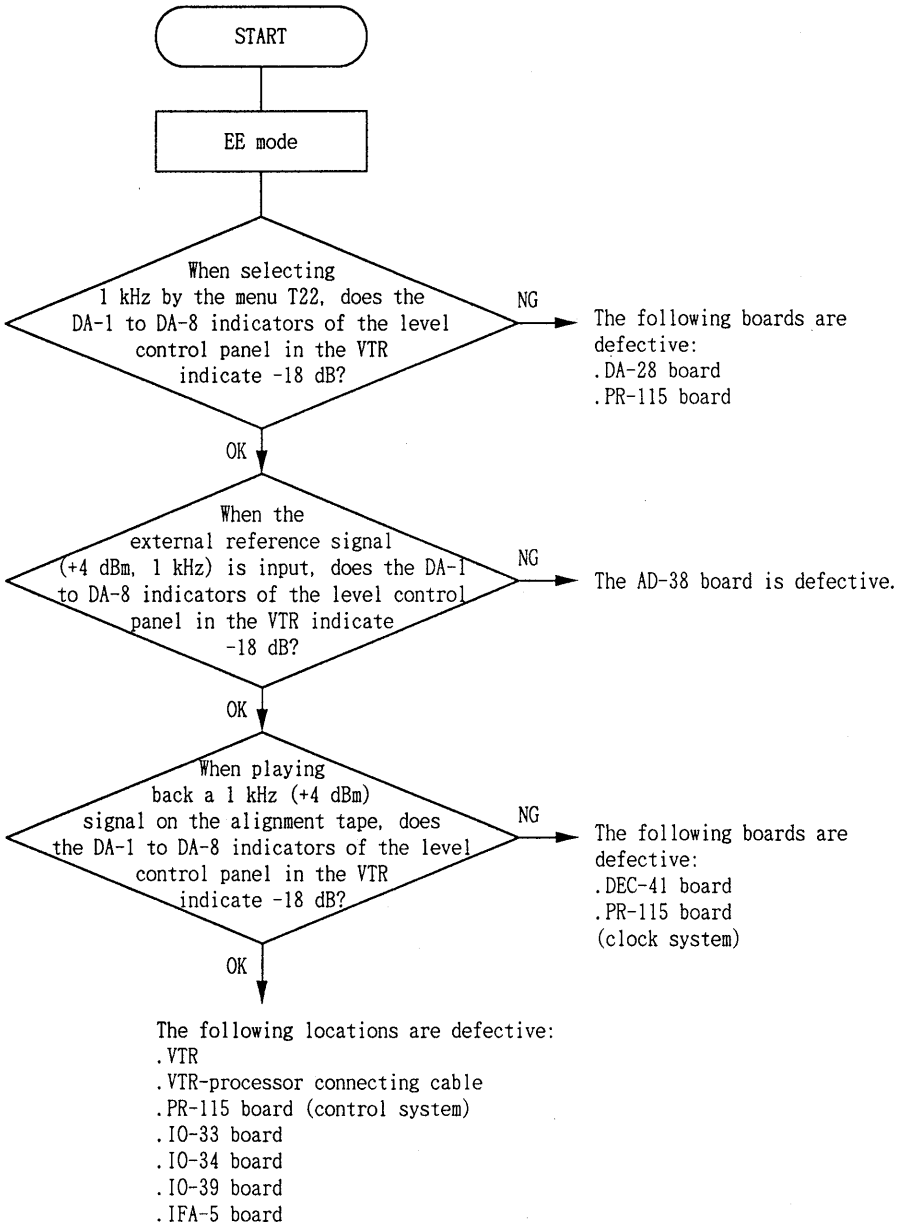
The audio signal is output normally described in the flow chart means the following conditions :

1. The audio monitor select buttons on the level control panel in the VTR operate normally.
2. The output signal of the headphones and the ANALOG OUT connector meets the specification.
3. When selecting 1 kHz in the menu of VTR T22 AUDIO TEST SG, the DA-1 to DA-8 level meters of the level control panel in the VTR indicate −18 dB.

• **When having the new board :**

The cause of error or the location where the error occurs can be located by the following flow.

• **When not having the new board :**



3-5. SETTING UP CONTROLLED FROM BOTH VTR & PROCESSOR

Setting up of the processor can also be done by operating the switches on the boards of the processor instead of by the menu system of the VTR.
When setting up of the processor is done by operating the switches on the boards of the processor, set S7-7 on the PR-115 board to ON so that the PROC. SW ENABLE indicator on the front panel of the processor is turned on.
In addition, set one of the following switches to ON so that the red of the TEST MODE indicator on the front panel of the processor lights up.

1. S3-8 on the SG-151 board
2. S1-8 on the ADA-12 board
3. S2-8 on the CI-05 board

When selecting setting by the menu of the VTR, the board switches of the processor must not be activated. In this case, set all of the above switches to OFF.

3-5-1. Video Test Signal Generator

The six types of video test signals in the processor can be selected by either the menu of the VTR, T20. VIDEO TEST SG, or by the switches on the SP-06 board of the processor. Control from either the menu of the VTR or the switch on the board is selected by the setting of the VIDEO SYSTEM BOARDS MODE SELECT switch (S7-7/PR-115 board).

S7-7/ PR-115	Selection of test signal
OFF	Selects by VTR menu
ON	Selects by switches S1 and S2/SP-06 board

The test signals which can be selected by the menu of the VTR or the switches on the board in the processor are shown below. These signals are used for video system alignment and circuit checks.
When selecting the test signals by the switch, be sure to set the SG (test signal) switch (S1/SP-06 board) to ON.

Menu T20	S2/SP-06	Test signal
COMP	0 or 8	Composite (color-bar, multi-burst, pulse & bar and 10-step linearity signals)
CB	1 or 9	Color bar
MB	2 or A	Multi-burst
10S	3 or B	10-step linearity
PULSE	4 or C	Pulse & bar
BB	5, 6, 7, D, E or F	Black burst

3-5-2. Selection of the Video Input/Output Signal

(1) Selection of the Source of the Video Reference Signal

The source of the video reference signal in the processor can be selected by the menu of the VTR (S12. REF SELECT, I80. INPUT ANALOG/DIGITAL and I82. PROC PB REF SELECT), by the switch on the PR-115 board in the processor or by the switches on the SG-151 board. (The switch on the PR-115 board is only selectable for an analog video input signal.)
The source selection method for the video reference signal is determined by setting the VIDEO SYSTEM BOARDS MODE SELECT switch (S7-7/PR-115 board) and TEST ON/OFF switch (S3-8/SG-151 board) as shown below.

S7-7/ PR-115	S3-8/ SG-151	Selection of reference signal
OFF	OFF	Selects by menu S12, I80, I82
ON	OFF	Selects by switch/PR-115 board
ON or OFF	ON	Selects by switches/ SG-151 board

The source of the COM REF signal (reference signal for the video REC system of the processor and VTR) and the PROC REF signal (reference signal for the video PB system of the processor) can be selected by the above menu and the setting of the switches on the boards of the processor.
The combination of the switches is shown in the next page. In the case of other settings, recording and/or playback is not performed correctly.
For details of the menu of the VTR, see the operation manual of the HDD-1000, Section 1-4 Menu.
For details of the switches on the boards in the processor, see the maintenance manual of the HDDP-1000, Section 1-9 Switch/Jumper Settings.

• **Selection by the menu of the VTR**

Settings			Source of reference signal	
I80	S12	I82	Source of COM REF signal	Source of PROC REF signal
ANALOG	INPUT	COM REF	ANALOG VIDEO G/Y IN signal	ANALOG VIDEO G/Y IN signal
		EXT REF	ANALOG VIDEO G/Y IN signal	ANALOG VIDEO G/Y IN signal
		INPUT	ANALOG VIDEO G/Y IN signal	ANALOG VIDEO G/Y IN signal
		DIGITAL	ANALOG VIDEO G/Y IN signal	DIGITAL VIDEO IN signal (*1)
	EXT REF	COM REF	ANALOG VIDEO SYNC IN signal	ANALOG VIDEO SYNC IN signal
		EXT REF	ANALOG VIDEO SYNC IN signal	ANALOG VIDEO SYNC IN signal
		INPUT	ANALOG VIDEO SYNC IN signal	ANALOG VIDEO SYNC IN signal
		DIGITAL	ANALOG VIDEO SYNC IN signal	DIGITAL VIDEO IN signal (*1)
	AUTO	Source of the reference signal is the same as INPUT of S12 during recording and editing, and as EXT REF of S12 during playback.		
DIGITAL	INPUT	COM REF	DIGITAL VIDEO IN signal	DIGITAL VIDEO IN signal
		EXT REF	DIGITAL VIDEO IN signal	ANALOG VIDEO SYNC IN signal (*1)
		INPUT	DIGITAL VIDEO IN signal	ANALOG VIDEO G/Y IN signal (*1)
		DIGITAL	DIGITAL VIDEO IN signal	DIGITAL VIDEO IN signal
	AUTO (*2) (during recording/ editing)	COM REF	DIGITAL VIDEO IN signal	DIGITAL VIDEO IN signal
		EXT REF	DIGITAL VIDEO IN signal	ANALOG VIDEO SYNC IN signal (*1)
		INPUT	DIGITAL VIDEO IN signal	ANALOG VIDEO G/Y IN signal (*1)
		DIGITAL	DIGITAL VIDEO IN signal	DIGITAL VIDEO IN signal
	AUTO (*2) (during playback)	COM REF	ANALOG VIDEO SYNC IN signal	ANALOG VIDEO SYNC IN signal
		EXT REF	ANALOG VIDEO SYNC IN signal	ANALOG VIDEO SYNC IN signal
		INPUT	ANALOG VIDEO SYNC IN signal	ANALOG VIDEO SYNC IN signal
		DIGITAL	ANALOG VIDEO SYNC IN signal	DIGITAL VIDEO IN signal (*1)

• **Selection by the switch on the PR-115 board**

S6-7	Source of COM REF signal
ON	ANALOG VIDEO SYNC IN signal
OFF	ANALOG VIDEO G/Y IN signal

• **Selection by the switches on the SG-151 board**

See the next page.

• **Selection by the switches on the SG-151 board**

S3-1	(*5) S3-2	S6	S3-3	S3-4	Source of reference signal		Note
					Source of COM REF signal	Source of PROC REF signal	
OFF	OFF	OFF	OFF	OFF	ANALOG VIDEO G/Y IN signal	ANALOG VIDEO G/Y IN signal	(*3)
OFF	OFF	OFF	OFF	ON	ANALOG VIDEO SYNC IN signal	ANALOG VIDEO SYNC IN signal	(*3)
OFF	OFF	ON	OFF	OFF	ANALOG VIDEO G/Y IN signal	ANALOG VIDEO G/Y IN signal	(*4)
OFF	OFF	ON	OFF	ON	ANALOG VIDEO SYNC IN signal	ANALOG VIDEO SYNC IN signal	(*4)
OFF	ON	OFF	OFF	OFF	DIGITAL VIDEO IN signal	ANALOG VIDEO G/Y IN signal	(*1)
OFF	ON	OFF	OFF	ON	DIGITAL VIDEO IN signal	ANALOG VIDEO SYNC IN signal	(*1)
ON	OFF	OFF	OFF	OFF	ANALOG VIDEO G/Y IN signal	DIGITAL VIDEO IN signal	(*1)
ON	OFF	OFF	OFF	ON	ANALOG VIDEO SYNC IN signal	DIGITAL VIDEO IN signal	(*1)
ON	ON	×	×	×	DIGITAL VIDEO IN signal	DIGITAL VIDEO IN signal	

× : any position (ON or OFF)

(*1) The field frequency of both the digital video input signal and the analog video (G/Y or SYNC) input signal must be 60 Hz, and they must be synchronized. The phase difference must be less than 50 μ sec.
(*2) When the S12 menu is set to EXT REF, AUTO is automatically set.
(*3) The field frequency of the analog video (G/Y or SYNC) input signal must be 60 Hz.
(*4) The field frequency of the analog video (G/Y or SYNC) input signal must be 59.94 Hz. In this case, only playback can be performed.
(*5) The COM REF SELECT switch (S3-2) must be set to the same position as that of the ANALOG/DIGITAL INPUT SELECT switch (S3-7).

(2) Selection of the Video Input Signal

The video input signal can be selected by the menu of the VTR (I80. INPUT ANALOG/DIGITAL), the ANALOG/DIGITAL INPUT SELECT switch (S6-8/PR-115 board) or the ANALOG/DIGITAL INPUT SELECT switch (S3-7/SG-151 board).
The selection method for the video input signal is determined by setting the VIDEO SYSTEM BOARDS MODE SELECT switch (S7-7/PR-115 board) and TEST ON/OFF switch (S3-8/SG-151 board) as shown below.

S7-7/ PR-115	S3-8/ SG-151	Selection of video input signal
OFF	OFF	Selects by menu I80
ON	OFF	Selects by S6-8/PR-115 board
ON or OFF	ON	Selects by S3-7/SG-151 board

For details of the menu of the VTR, see the operation manual of the HDD-1000, Section 1-4 Menu.
For details of the switches on the boards in the processor, see the maintenance manual of the HDDP-1000, Section 1-9 Switch/Jumper Settings.

- Selection by the menu of the VTR
  Select the video input signal with the menu, I80. INPUT ANALOG/DIGITAL.
  When menu I80 is set to DIGITAL, a digital video signal is input.
  When menu I80 is set to ANALOG, an analog video signal is input.

- Selection by the switch on the PR-115 board
  Select the video input signal with the ANALOG/DIGITAL INPUT SELECT switch (S6-8).
  When this switch is set to ON, a digital video signal is input.
  When this switch is set to OFF, an analog video signal is input.

- Selection by the switch on the SG-151 board
  Select the video input signal with the ANALOG/DIGITAL INPUT SELECT switch (S3-7).
  When this switch is set to ON, a digital video signal is input.
  When this switch is set to OFF, an analog video signal is input.

(3) Selection of an Analog Video Input Signal (GBR/YPBPR)

The analog video input signal (GBR/YPBPR) can be selected by the menu of the VTR (I81. INPUT G.B.R./Y.PB.PR.), the ANALOG VIDEO INPUT SELECT switch (S7-5/PR-115 board) or the ANALOG VIDEO INPUT SELECT switch (S1-2/ADA-12 board). The selection method for the analog video input signal is determined by setting the VIDEO SYSTEM BOARDS MODE SELECT switch (S7-7/PR-115 board) and the LOCAL/REMOTE select switch (S1-8/ADA-12 board) as shown below.

S7-7/ PR-115	S1-8/ ADA-12	Selection of analog video input signal
OFF	OFF	Selects by menu I81
ON	OFF	Selects by S7-5/PR-115 board
ON or OFF	ON	Selects by S1-2/ADA-12 board

For details of the menu of the VTR, see the operation manual of the HDD-1000, Section 1-4 Menu.
For details of the switches on the boards in the processor, see the maintenance manual of the HDDP-1000, Section 1-9 Switch/Jumper Settings.

- Selection by the menu of the VTR
  Select the analog video input signal with the menu, I81. INPUT G.B.R./Y.PB.PR.
  When menu I81 is set to G.B.R., the GBR signal is input.
  When menu I81 is set to Y.PB.PR., the YPBPR video signal is input.

- Selection by the switch on the PR-115 board
  Select the analog video input signal with the ANALOG VIDEO INPUT SELECT switch (S7-5).
  When this switch is set to ON, the YPBPR signal is input.
  When this switch is set to OFF, the GBR signal is input.

- Selection by the switch on the ADA-12 board
  Select the analog video input signal with the ANALOG VIDEO INPUT SELECT switch (S1-2).
  When this switch is set to ON, the YPBPR video signal is input.
  When this switch is set to OFF, the GBR video signal is input.

(4) Selection of the Analog Video Output Signal (GBR/YPBPR)

The analog video output signal (GBR/YPBPR) can be selected by the menu of the VTR (I83. OUTPUT G.B.R./Y.PB.PR.), the ANALOG VIDEO OUTPUT SELECT switch (S7-6/PR-115 board) or the ANALOG VIDEO OUTPUT SELECT switch (S1-4/ADA-12 board).
The selection method for the analog video output signal is determined by setting the VIDEO SYSTEM BOARDS MODE SELECT switch (S7-7/PR-115 board) and the LOCAL/REMOTE select switch (S1-8/ADA-12 board) as shown below.

S7-7/ PR-115	S1-8/ ADA-12	Selection of analog video input signal
OFF	OFF	Selects by menu I83
ON	OFF	Selects by S7-6/PR-115 board
ON or OFF	ON	Selects by S1-4/ADA-12 board

For details of the menu of the VTR, see the operation manual of the HDD-1000, Section 1-4 Menu.
For details of switches on the boards in the processor, see the maintenance manual of the HDDP-1000, Section 1-9 Switch/Jumper Settings.

- Selection by the menu of the VTR
  Select the analog video output signal with the menu, I83. OUTPUT G.B.R./Y.PB.PR.
  When menu I83 is set to G.B.R., the GBR signal is output.
  When menu I83 is set to Y.PB.PR., the YPBPR video signal is output.

- Selection by the switch on the PR-115 board
  Select the analog video output signal with the ANALOG VIDEO OUTPUT SELECT switch (S7-6).
  When this switch is set to ON, the YPBPR signal is output.
  When this switch is set to OFF, the GBR signal is output.

- Selection by the switch on the ADA-12 board
  Select the analog video output signal with the ANALOG VIDEO OUTPUT SELECT switch (S1-4).
  When this switch is set to ON, the YPBPR video signal is output.
  When this switch is set to OFF, the GBR video signal is output.

3-5-3. Selection of the Tape Path System Mode of the VTR

The processor can be set to the mode which corresponds to the tape path system mode of the VTR. When setting the processor to the tape path system mode of the VTR, perform either of the following operations :

- Set the VIDEO SYSTEM BOARDS MODE SELECT switch (S7-7) and CI-05 BOARD MODE SELECT switch (S7-8) on the PR-115 board to ON.
- Set the TEST ON/OFF switch (S2-8) on the CI-05 board to ON.

1. Setting the slow stunt playback mode
   Set the NOR/STUNT select switch (S1-4/CI-05 board) to ON.

2. Setting the fast playback mode
   Set the NOR/FAST select switch (S1-5/CI-05 board) to ON.

3. Setting the direction for tape transport
   Select the direction of tape transport with the FOW/REV select switch (S1-6/CI-05 board).
   When this switch is set to ON, the processor is put into the REVERSE mode.
   When this switch is set to OFF, the processor is put into the FORWARD mode.

4. Setting the REC or PB mode
   Select this mode with the REC/PB select switch (S1-7/CI-05 board).
   When this switch is set to ON, the processor is put into the PB mode.
   When this switch is set to OFF, the processor is put into the REC mode.

5. Setting the bidirectional playback mode
   Set the NOR/MOV select switch (S1-8/CI-05 board) to ON.

6. Output of a frozen picture
   The relationship between the setting of switches and the type of the frozen picture is shown below.

S2-1/ CI-05	S2-2/ CI-05	Type of frozen picture
ON	ON	FIELD 1 FREEZE
ON	OFF	FIELD 2 FREEZE
OFF	ON	FRAME (FIELD 1 & 2) FREEZE
OFF	OFF	Non-frozen playback picture

7. Setting the EE mode
   Set the EE/TAPE select switch (S2-3/CI-05 board) to OFF.

3-5-4. How to Operate the Inner & Outer Correction Circuits

The inner and outer correction circuits are usually operated by setting the menu of the VTR (T08. INNER CORRECTION and T09 . OUTER CORRECTION). Therefore, errors in the video signal are corrected by these circuits to obtain a high-quality playback picture.
The inner and outer correction circuits can be operated not only by the menu of the VTR but also by the switches on the PR-115 board and CF-39 board in the processor.
The selection method for the inner and outer correction circuits is determined by the setting of the VIDEO SYSTEM BOARDS MODE SELECT switch (S7-7/PR-115 board).
The operation of the inner and outer correction circuits by the menu of the VTR and switches is shown below.

1. Inner correction

S7-7/ PR-115	Selection of inner correction circuit
ON	Selects by S4/CF-39 : ECC2 or ECC1
OFF	Selects by menu of VTR, T08 : ON

2. Outer correction

S7-7/ PR-115	Selection of outer correction circuit
ON	Selects by S4/CF-39 : ECC2
OFF	Selects by menu of VTR, T09 : ON

3-5-5. How to Operate the Conceal Circuit

The conceal circuit compensates a signal which could not be corrected in the inner and outer correction circuits. This circuit is usually operated by setting the menu of the VTR (T07. CONCEAL).
The conceal circuit can be operated not only by the menu of the VTR but also by the switches on the PR-115 board and CF-39 board in the processor.
The selection method for the conceal circuit is determined by the setting of the VIDEO SYSTEM BOARDS MODE SELECT switch (S7-7/PR-115 board).
The operation of the conceal circuit by the menu of the VTR and switches is shown below.

S7-7/ PR-115	Selection of conceal circuit
ON	Selects by S5/CF-39 : ON
OFF	Selects by menu of VTR, T07 : ON

SECTION 4
THEORY OF OPERATION

4-1. VIDEO SIGNAL SYSTEM

4-1-1. Outline

1. ADA-12 Board

There are two kinds of input video signal. One is analog input, and the other one is digital input. As for the analog input signals, both Y/PB/PR and G/B/R can be accepted. G/B/R analog input signal is, however, are converted into Y/PB/PR before A/D conversion. Digital signals are Y/PB/PR only.
The VIO-10 board is the video input and video output buffer amplifiers.

In the ADA-12 board, the level of video signal is controlled before A/D conversion. There are three AD converters for Y, PB and PR channels. The Y signal is output at the sampling rate of 74.25 MHz. As for the chroma signal, PB and PR are output alternately through multiplexing at the data rate of 37.125 MHz, resulting in the data rate of 74.25 MHz. A/D converted signals are sent to the SP-06 board with ECL level. In addition, the ADA-12 board has D/A converter and matrix amplifier which work in the playback stage.

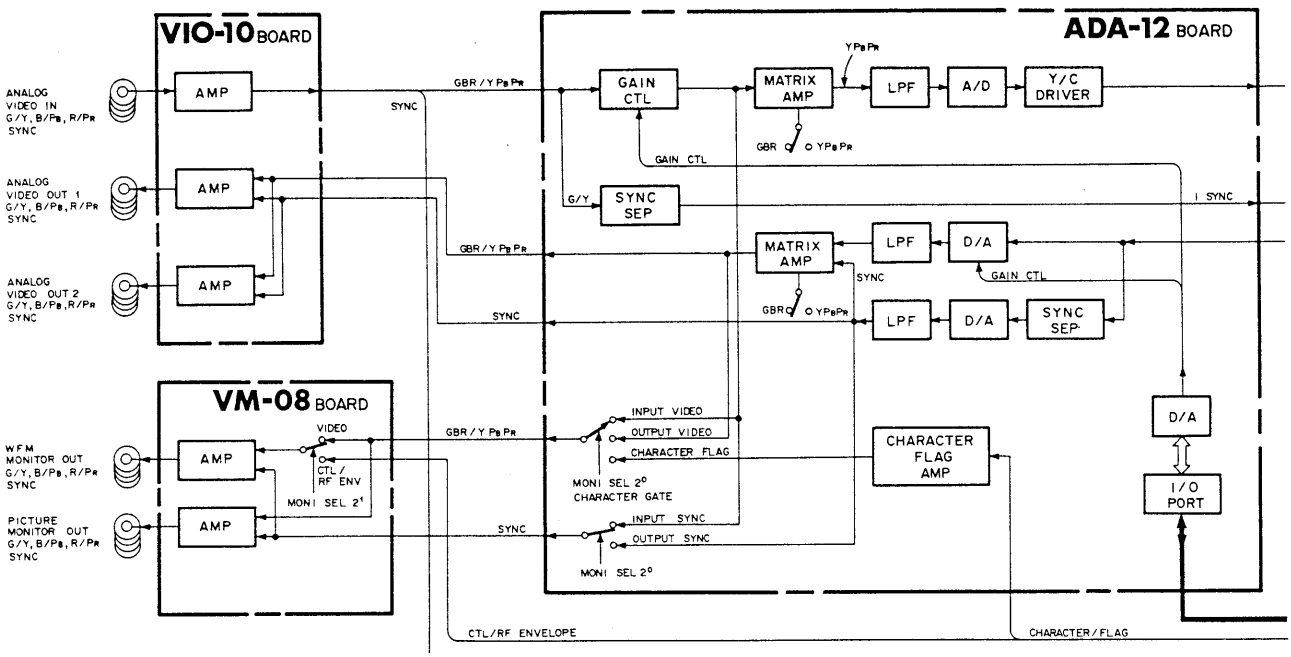


Fig. 4-1-1. ADA-12 Borad Block Diagram

2. DIF-1 Board

The DIF-1 board is located behind the processor boards. It works for digital interface, and consists of input and output buffer amplifiers and the PLL circuit for regenerating clock signal.

3. SP-06 Board

The SP-06 board firstly switches the digital data converted from the analog input signals sent from the ADA-12 board and the digital input signals sent from the DIF-1 board.
These input signals have the clock rate of 74.25 MHz. Therefore Y and Chroma signals are stepped down to 1/4 clock rate for 8-channel processing for the reasons of signal processing speed and recording tape speed in the VTR. The signal processing adopts a unique processing which assigns vertically-quartered data of the picture screen to each channel. This processing method facilitates error correction (concealment) processing. To be concrete, a serial-parallel converter converts 1-phase signal into 4-phase signal. Memory is also used for this processing.
This board incorporates an internal signal generator whose test signal, together with the above-mentioned serial-parallel converted signal, is switched and sent to the following channel interleave circuit. This channel interleave circuit mixes four-paralleled Y signal and four-paralleled chroma signal (P_B/P_R) to arrange them into each channel for improved error correction capability in the playback stage.
Outer code for playback error correction is added to the data, and then the data is sent to the following VE-18 board.
In addition, the SP-06 board is provided with the sync detector circuit necessary when digital input signal is selected, input/output port for SP-06 board control by the CPU on the PR-115 board, and timing signal generator for signal processing control.

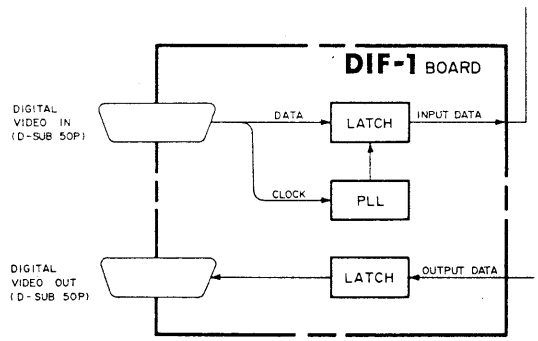


Fig. 4-1-2. DIF-1 Board Block Diagram

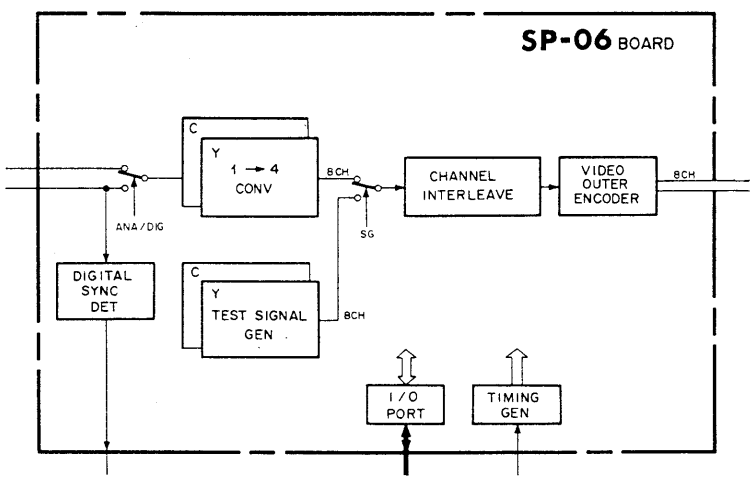


Fig. 4-1-3. SP-06 Board Block Diagram

4. VE-18 Board

One VE-18 board processes 4-channel signals. The HDDP-1000 is, therefore, provided with two VE-18 boards for processing 8-channel signals.

Data sent from the SP-06 board is written in the frame memory, and shuffled in units of field. This shuffling is performed for the dispersion of burst errors in the playback stage. Because it is able to improve the inner and outer error correction capability and the error concealment capability. I.e., error correction is made easier, and concealed data is hard to be noticed visibly.

For this shuffling, 1 Mbit DRAM is used as the frame memory. It functions as 2-frame memory for the reason of memory capacity. Shuffling is performed in units of 8-byte aggregate because of memory speed. Then, the sync code, ID data and block addresses necessary for playback are added to data. Inner code is also added.

Then, sync block shuffling, 8-8 conversion and bit exchange processing are performed. The 8-8 conversion is a recording modulation system which suppresses the low-frequency components in the record signals utilizing the correlation of the video signal. The 8-8 conversion does not have sufficient suppression efficiency of the low-frequency components in the parity period where adjacent data have no correlation with each other, and may result in deteriorated error rate in the parity period.

Thus, data are shuffled again in unit of the sync block to disperse the video data and parity data evenly ; by this, the error rates in the video data period and parity period are made equal.

Finally, the timing of data in each channel is different since each channel has different timing of recording on tape by the head. This board controls timing of four heads in a base. Timing difference of 1/2 segment for channel 1 to 4 and channel 5 to 8 is adjusted by the frame memory.

The VE-18 board is controlled by the CPU on the PR-115 board. For this communication, the VE-18 board is provided with the input/output ports. Also the VE-18 board has a timing signal generator for signal processing control, etc.

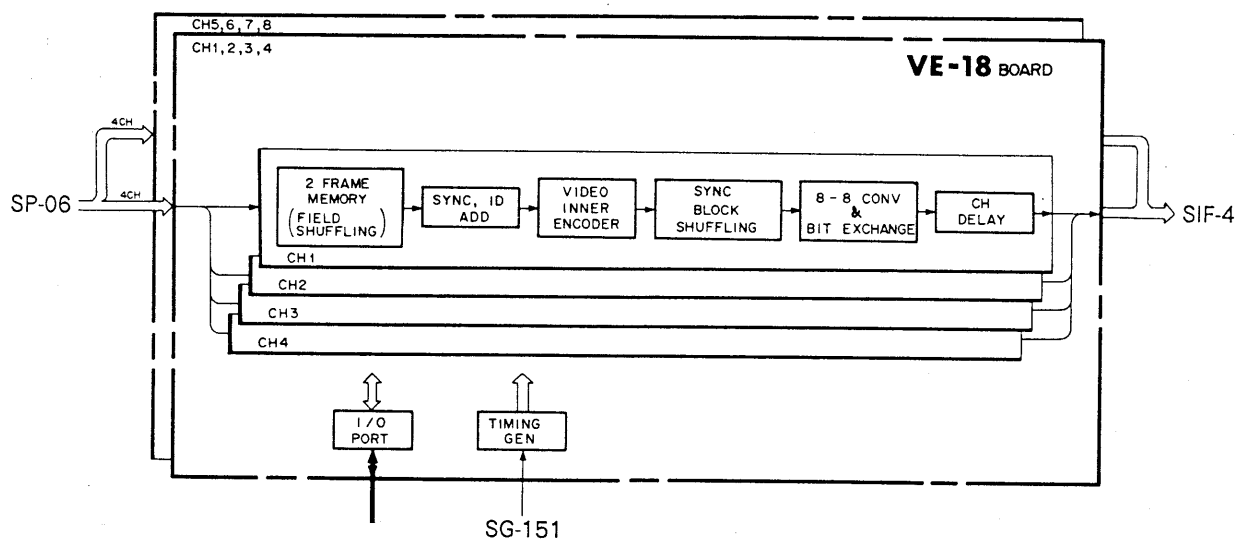


Fig. 4-1-4.

5. SIF-4 and PIF-3 Boards

8-channel 8-bit parallel signal is input to the SIF-4 board at the data rate of 18.6 MHz. This board converts the 8-bit parallel signal into the bit serial signal. That is, it converts the input signal into those at the data rate of 148.5 MHz and outputs them to the VTR and the PIF-3 board. The signal sent to the PIF-3 board is for processor unit test mode bypass line.

The PIF-3 board selects the signals sent from the VTR or SIF-4 board, and converts them into bit parallel signals, i.e., 4-bit parallel signals in this stage. The data rate of the signal is approx. 37 MHz.

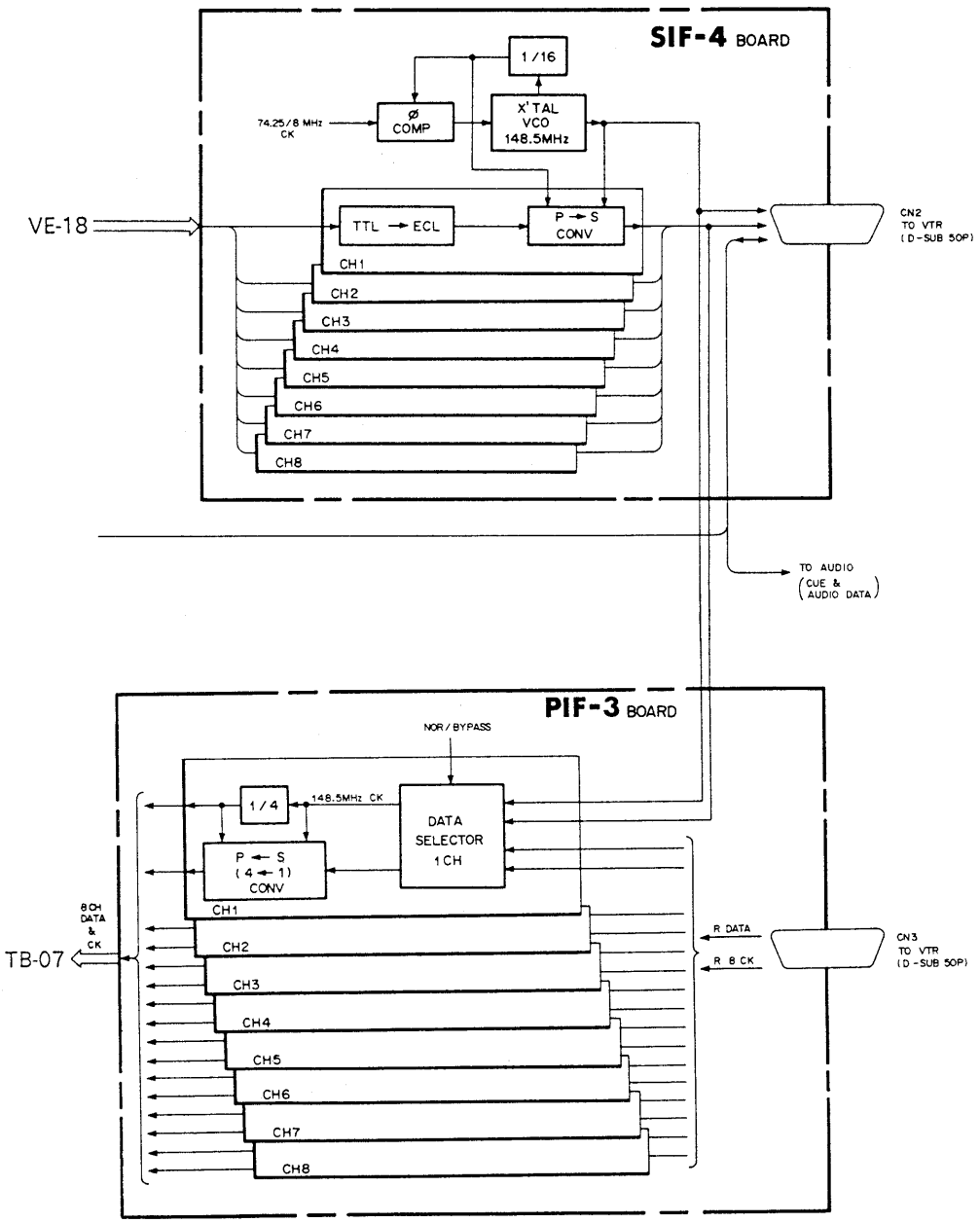


Fig. 4-1-5

6. TB-07 Board

8-channel 4-bit parallel signal (at the data rate of 37.1 MHz) is input to the TB-07 board. This board firstly coverts the input 4-bit parallel signal into 8-bit parallel signal (at the data rate of 18.6 MHz), and then the signal is undergone the time base correction to reject the jitter component.
Then, the TP-07 board detects block sync and obtains the bit shift value. The barrel shifter performs bit shift correction.
Since the ID data added to the sync block is 4-8 converted in the recording stage, the 4-byte ID data is converted into 2 bytes through 8-4 conversion. At the same time, ID correction is performed here utilizing redundancy of 4-8 conversion.

7. CI-05 Board

8-channel signals input to the CI-05 board independently pass through 1-block de-shuffling, bit exchanger, and 8-8 converter. The following channel exchanger functions during variable speed playback operation such as slow playback, shuttle playback, etc. During shuttle playback operation, playback signals of each channel include non-home-channel signals. The above channel exchanger exchanges each channel's playback signals appropriately and returns these playback signals to their home channels to facilitate further signal processing. Channel ID data in the playback signal is used to generate the exchange control signal. The playback signals of channels 1 to 4 and channels 5 to 8 include skew with respect to the sync block. Skew occurs when these signals are exchanged. The block skew corrector corrects this skew.

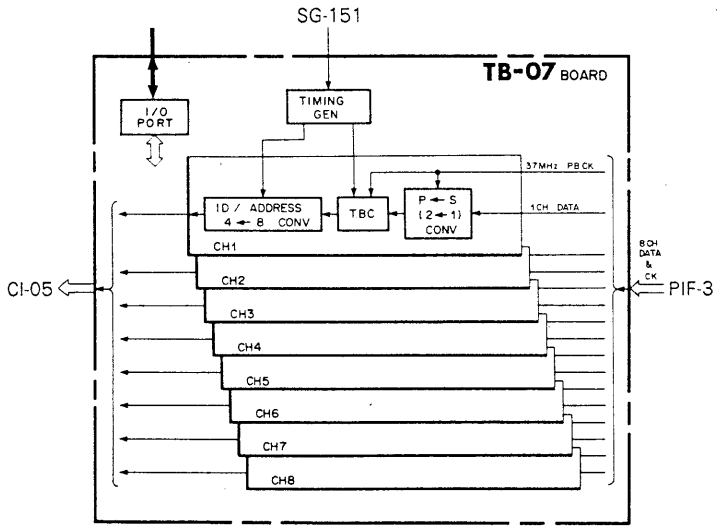


Fig. 4-1-6. TB-07 Board Block Diagram

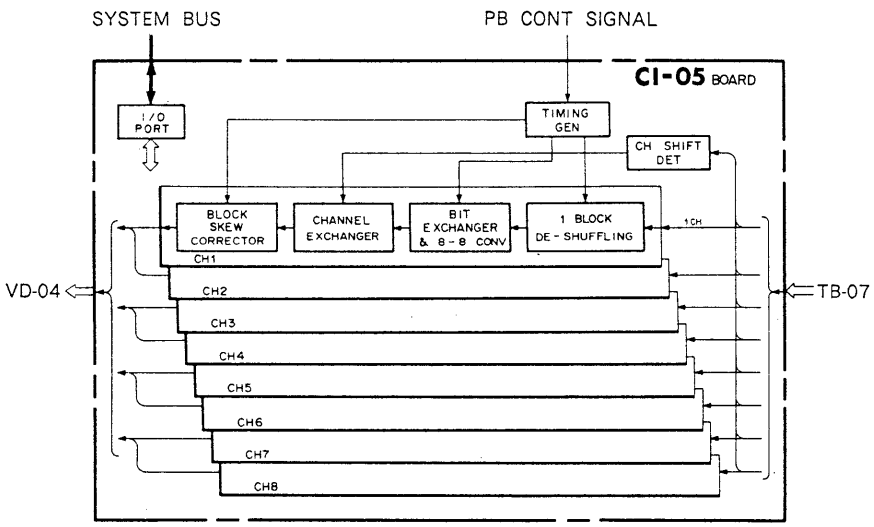


Fig. 4-1-7. CI-05 Board Block Diagram

8. VD-04 Board

The HDD-1000 incorporates four VD-04 boards ; one board covers 2-channel signals. These four boards are identical.

Input signals pass through the inner corrector first. Though 6-byte parity codes are added and up to 3 bytes error can be corrected, 2-error correction is performed because of avoiding an erroneous correction. Error flags are added to all the blocks with uncorrected errors in the inner correction.

Then, the main memory carries out deshuffling for outer correction. Since the outer code consists of 4 bytes, it is possible to perform 4-byte erasure correction.

The VD-04 board has 2 frames memory. Especially in the slow playback mode, it stores data in suitable addresses in accordance with the field ID and frame ID added to the sync block and outputs noise-less continuous picture.

9. CF-39 Board

In the CF-39 board, the 8-channel data sent from the VD-04 board is input to the channel de-interleave circuit. 4-parallel Y signal and 4-parallel chroma signal (P_B and P_R) are input to this circuit with the mixed data form. They are completely separated when being output. This deinterleave is the reverse to the channel interleave in the SP-06 board.

Since each of the 4-parallel signal is vertically-quartered signal of the picture screen, error correction at the either end of the divided picture screen requires its adjacent data. Thus, contiguous data are added to the data at both ends of the divided picture screen. This processing is called overlap addition.

Then, error concealment is performed for the 4-parallel Y signal and 4-parallel chroma signal independently. This error concealment consists of two methods ; averaging adjacent data in the vertical, horizontal or either diagonal direction of an error data, and replacement with one of eight peripheral data. It is carried out by selecting one from these methods according to the certain priority.

In addition, the CF-39 board is controlled by the CPU on the PR-115 board. For this communication, the CF-39 board is provided with the input/output ports.

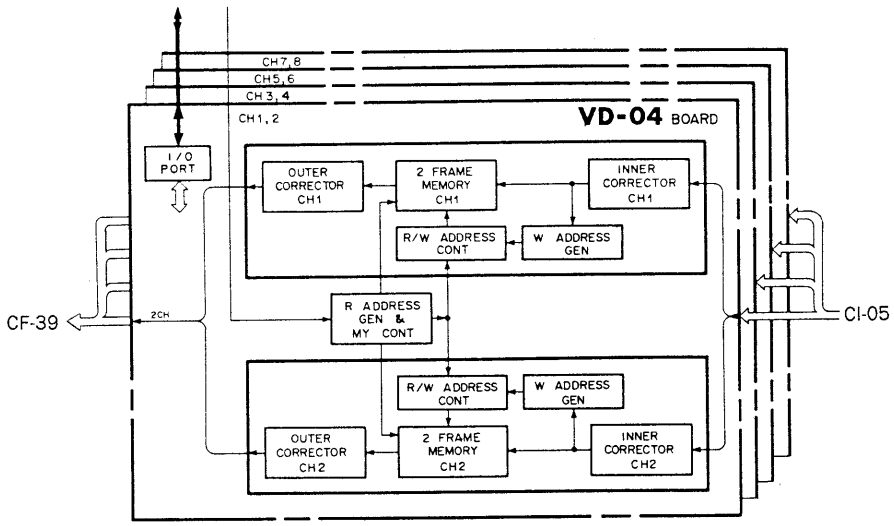


Fig. 4-1-8. VD-04 Board Block Diagram

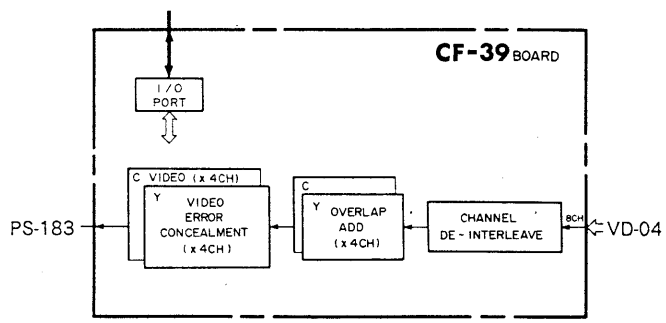


Fig. 4-1-9. CF-39 Board Block Diagram

10. PS-183 Board

In the PS-183 board, 4-parallel Y and chroma signals sent from the CF-39 board are firstly returned to the original Y and chroma signals at the clock rate of 74.25 MHz through parallel-serial conversion. The tri-level sync digital data is inserted to the H blanking and V blanking periods of Y signal.

One line of signal is sent to the ADA-12 board and D/A converted to be analog output signal. Since the group delay time of the interpolating filter is different for the Y signal and chroma signal, the Y/C delay adjust circuit delays the Y signal to control the time difference in units of clock.

Another line of signal is sent to the DIF-1 board and made into digital output signal. For this purpose, Sync code and ID data for digital transmission are added to the Y signal. The PS-183 board is controlled by the CPU on the PR-115 board. For this communication, the PS-183 board is provided with the input/output ports.

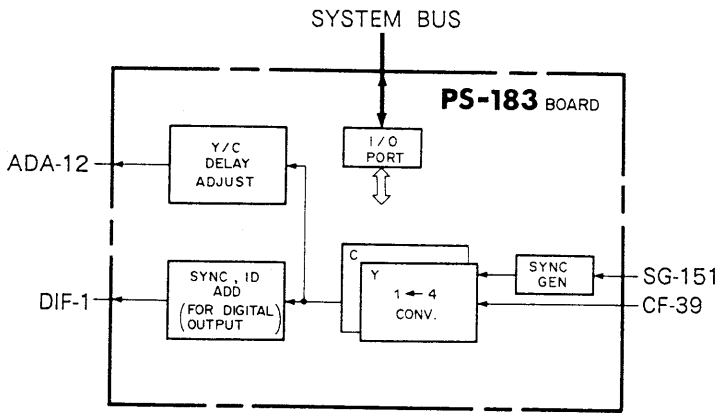


Fig. 4-1-10. PS-183 Board Block Diagram

11. SG-151 Board

The SG-151 board generates various timing clock pulses necessary for the system. The sync of the digital video input or analog video input signal is used as the reference signal. In the case of analog input, the input sync and external sync are selectable. The PLL circuit is locked based on the selected sync signal, generating the reference signal. This reference signal and the digital reference signal sent from the SP-06 board are supplied to the common reference selector and process reference selector.
Timing pulses for the video recording system, VTR system and audio system are generated based on the reference signal selected by the common reference selector. The timing pulses for the video playback system are generated based on the reference signal selected by the process reference selector. The phase of output video signals is determined by this reference signal. In the recording stage, the common reference selector selects the same reference signal as the record signal (analog or digital input). The process reference selector can select the reference signal independently. If the reference sync is not supplied in the playback mode, this board operates in the internal mode.
In addition, the SG-151 board is provided with a video level control, whose output is A/D converted and output to the ADA-12 board via the bus interface.

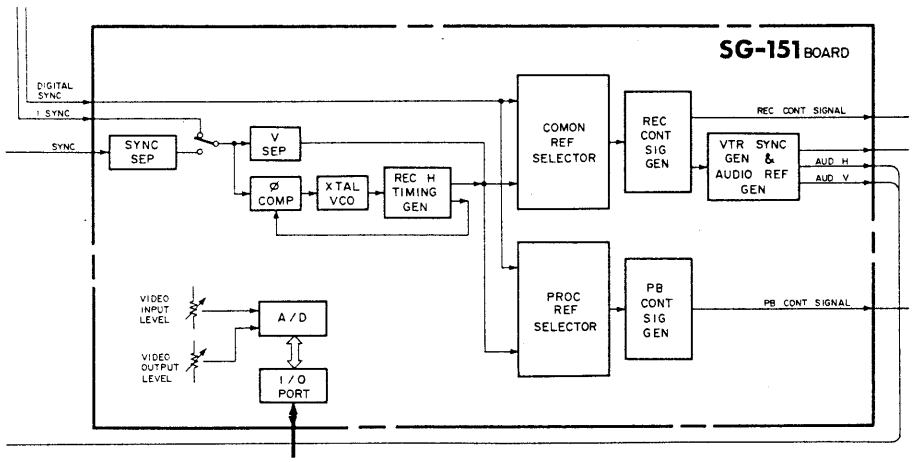


Fig. 4-1-11. SG-151 Board

4-1-2. VIO-10 Board

The VIO-10 board has one analog video input buffer amplifier and two analog output buffer amplifier. Input video signal is attenuated by approx. 3.5 dB by R13, R14, R15 and R2 so that the amplifier IC1 does not saturate in case of APL fluctuation when the sync signal is extracted from the video signal at the G/Y connector. The output of the input buffer amplifier is supplied to the ADA-12 board.
The output video signal from the ADA-12 board is amplified double by IC5, then output from the buffer IC6 and IC7 as two lines of video output signal. The output resistors R87 and R90 of IC6 and IC7 and capacitors C80 and C180 are improving the output return loss.

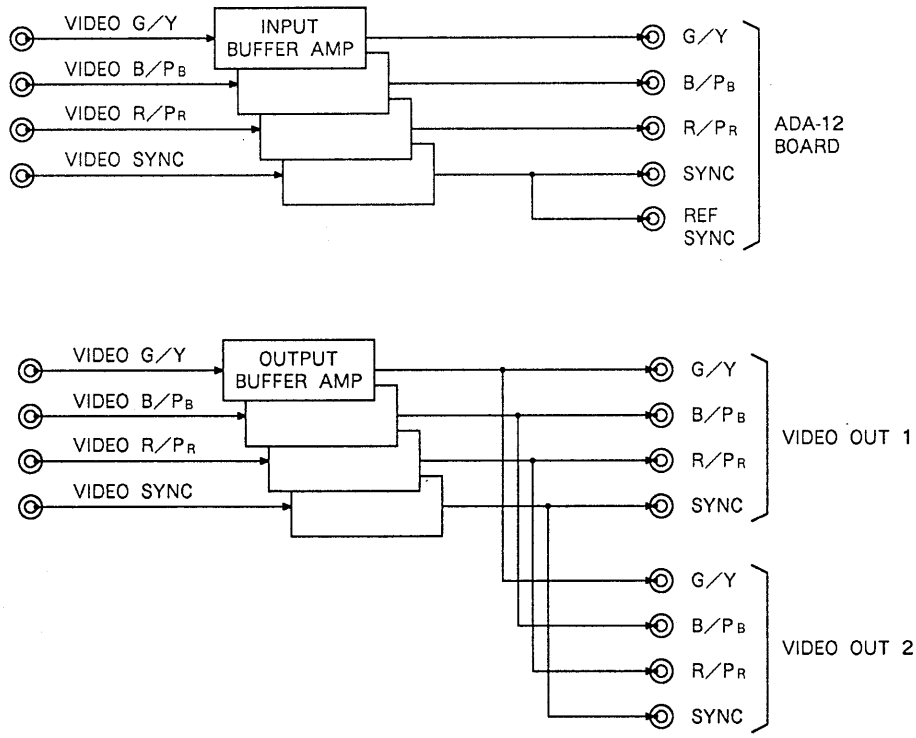


Fig. 4-1-12. VIO-10 Board Block Diagram

4-1-3. ADA-12 Board

1. A/D Converter and Sync Separator

The G, B, R or Y, P_B/, P_R analog video signals from the VIO-10 board is input the input gain control circuit first. This circuit controls the input within +2 dB.
The input G, B, R or Y, P_B/, P_R signals adjusted to 1 Vp-p by the gain control circuit is then supplied to the matrix amplifier. This matrix amplifier converts the G, B, R signals into the Y, P_B, P_R signals. It does not execute matrix operation for the Y, P_B, P_R signals input.
The band widths of the Y, P_B, P_R signals are limited by the low-pass filter ; the Y signal is limited to 30 MHz, and the P_B and P_R signals are to 15 MHz. Then, they are input to the A/D converter and digitalized. Then, the P_B and P_R signals are multiplexed into one chroma signal. The Y signal and resultant chroma signal are sent to the following SP-06 board as two digital signals with the same data rate.
The sync signal added to the G/Y signal is separated by the sync separator circuit and is supplied to the SG-151 board.

2. D/A Converter

On the contrary to the input line, two Y and chroma digital playback signals from the PS-183 board are made into three-channel Y, P_B and P_R signals, through separation of P_B and P_R signals from the chroma signal, which are sent to the D/A converters respectively. The sync signal is separated from the Y signal by the sync separator circuit and is sent to the dedicated D/A converter and converted into analog signal.
The output video level is controlled by changing the REF voltage of each D/A converter within the range of +2 dB. The D/A-converted video signal passes through the low-pass filter also serving as the aperture compensator and are converted into analog signal, then sent to the matrix amplifier. The matrix amplifier converts the Y, P_B, P_R signal into the G, B, R signals. It does not execute matrix operation for the Y, P_B, P_R signals output. This matrix amplifier also adds the sync signal to the output video signal. The output of the matrix amplifier is supplied to the VIO-10 board as the analog video output signal.

3. Character Insertion Circuit

In addition, the ADA-12 board is provided with a character flag amplifier for issuing the character signal and flag signals to the processor. These signals can be superimposed onto the output video signal. The superimposed signals are output to the VM-08 board as the WFM/PICTURE MONITOR output signal. The character signal can be superimposed onto the input video signal to be recorded as a special use.
To the MONITOR OUT, the input video signal can be directly output for checking the input video signal. The input and output gain control and selection of various operations on the board can be digitally controlled from outside using the input and output ports.

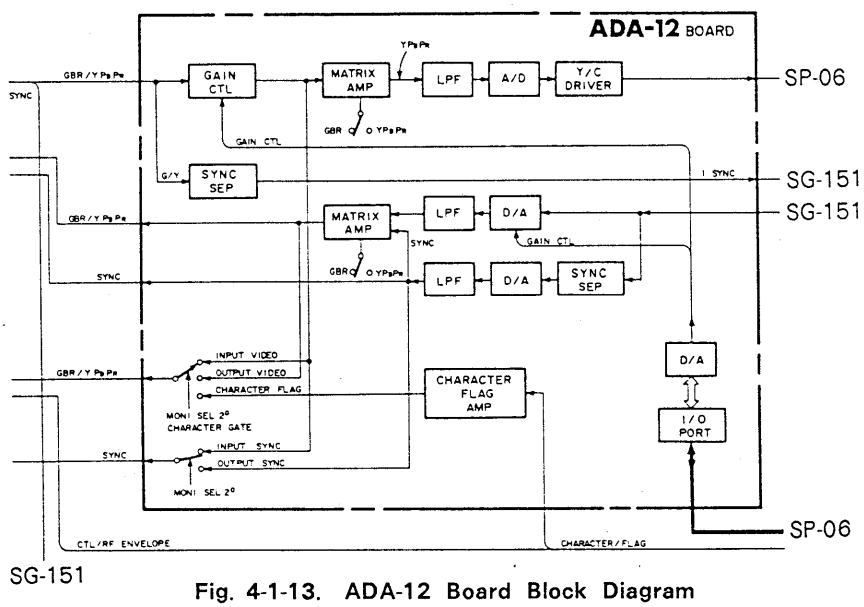


Fig. 4-1-13. ADA-12 Board Block Diagram

4-1-4. SG-151 Board

1. Outline

The SG-151 board produces timing pulse and clock signals for the processor from the input reference signal. It produces the timing reference and clock signals for both recording and playback.
Though accurate timing signal for the audio system is produced by the PR-115 board, its reference H and V signals are produced by this SG-151 board.
The sync separator shown in the Fig. 4-1-14 is for the external sync signal. Since the R, G, B also has the sync, the external sync signal is needless. However, the EXT SYNC connector is provided since it may be used for playback with no input video signal.
For the input video signal, the sync separator circuit is provided in the ADA-12 board.
A switch is provided in the next stage of sync separator. It works for the selection of the external sync and the I sync (i.e., the sync separated by the ADA-12), and then the selected sync is divided into V and H.
The V signal is directly fed to the common reference selector and process reference selector for producing the timing signal.
The H signal serves as the reference signal for the PLL loop consisting of the comparator, crystal VCO, and REC H timing generator. The output of the H timing generator is fed to the common reference selector and process reference selector.
Two crystal VCOs are mounted so that the reference signal suits to both 60 Hz and 59.94 Hz. Recording is available at 60 Hz only. Playback adapts to both of them. The lower circuit in Fig. 4-1-12 is an A/D converter of the control voltage of the input video level and output video level. Its data is supplied to the ADA-12 board via the input/output port.
There are eight volume controllers in all which are the input level of G/Y, B/P_B, R/P_R and master, and the output level of G, B, R and master.
The common reference selector selects digital reference for digital input, or input video sync or external sync (analog line reference) for analog input. The audio reference, servo reference, and video recording reference signals are generated based on the selected reference.
The process reference selector selects the video playback reference signal, i.e., digital or analog reference signal the same as the common reference selector.
These ca be selected independently.
The sync output from the processor (video phase, etc.) is matched to the reference signal selected with the process reference selector.

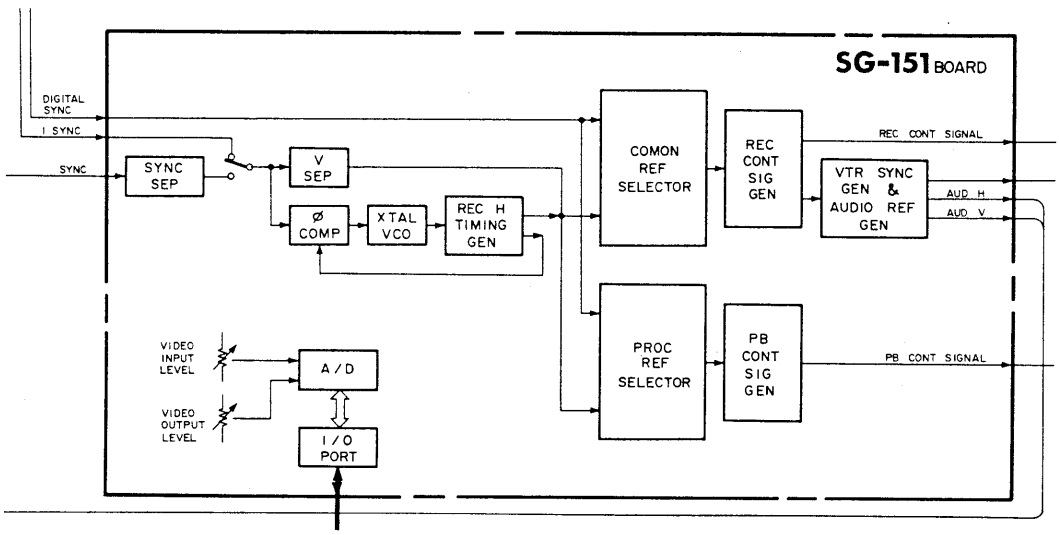


Fig. 4-1-14. SG-151 Board Block Diagram

2. Recording System

The SG 4CK, SG LNP and SG FP (SG feed pulse) signals in the Fig. 4-1-15 upper left are the reference signals separated from digital video input signals in case the digital video signal is input to the SP-06 board.

The I sync is standing for input sync signal which is separated in the ADA-12 board. The REF sync is external sync signal input. Its sync is separated and sent to reference sync selector.

From the signal selected with the reference sync selector, V signal is separated by the V separator circuit, and then the field pulse is generated by the field detector circuit. This signal is fed to both of the common reference selector and the process reference selector.

The H signal is also separated here and is supplied to the lock phase adjustment circuit. The RV8 works as a fine-adjustment of the video phase to compensate the variation of the filter in the ADA-12 board. Its output is supplied to the phase comparator in ICC12. Another input to the phase comparator is the divided VCO output signal via the window control circuit. The window control circuit is able to pass the only signal in the window of the phase comparator. It does not pass the signal which is out of the window such as pseudo pulse. It does not establish the window if this PLL circuit does not lock. Once locked, it outputs the only signal in the window but does not output the signal out of the window. The lock detector checks whether the PLL is locked or not. The output of the phase comparator is passed through the INT/EXT selector and supplied to the VCO. Unless the reference is supplied to the processor, the INT mode is established and the fixed voltage is applied to the VCO. The INT mode frequency can be adjusted with RV9. It is adjusted for VCO2 (60 Hz) in the exfactory setting. That is, 59.94 Hz is not guaranteed in the INT mode. The reference signal is required for using at 59.94 Hz.

The actual oscillation frequencies of VCO1 and VCO2 are 74.1758 MHz and 74.25 MHz respectively. These VCOs can be selected with the selector in the next stage. The H timing generator generates the clamp pulse, lock detector pulse, window pulse, phase comparator timing pulse, etc.

To the common REF selector, the digital input reference and analog input reference are supplied, which are selected in accordance with the mode. The reference for video recording, audio timing, and the VTR reference are produced from the selected signal.

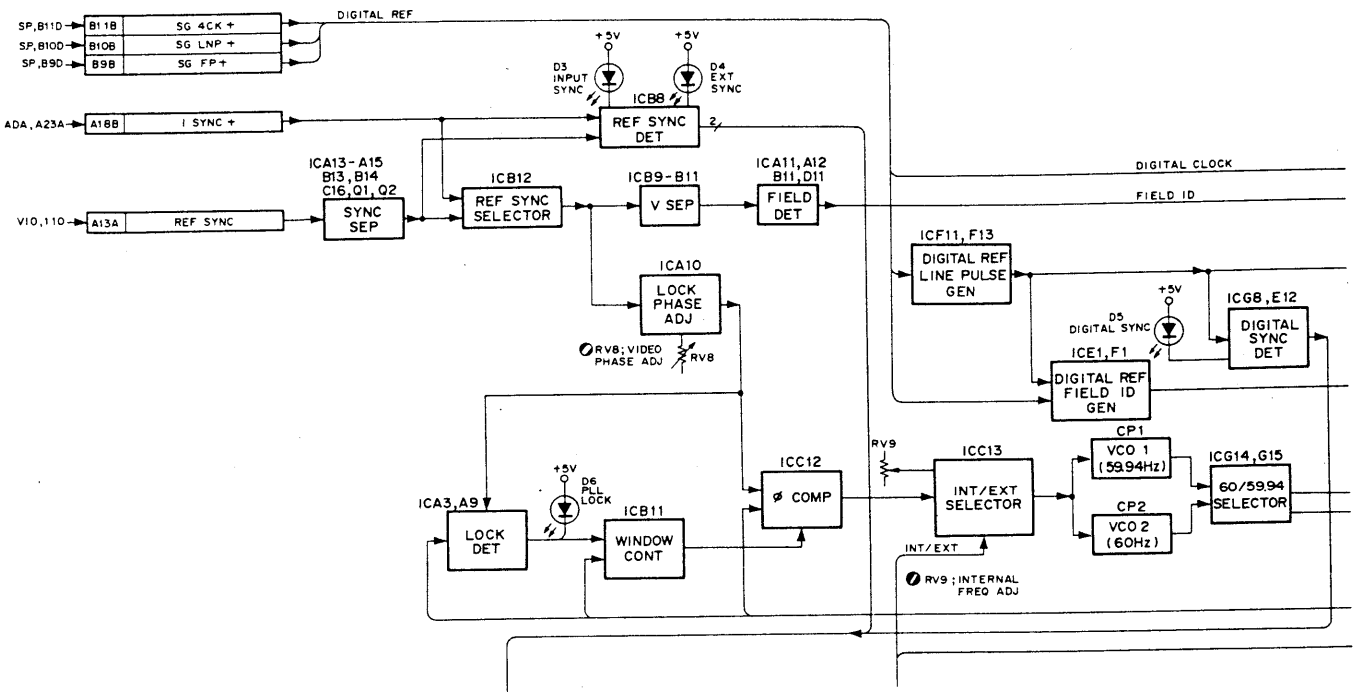


Fig. 4-1-15. Recording System Block Diagram

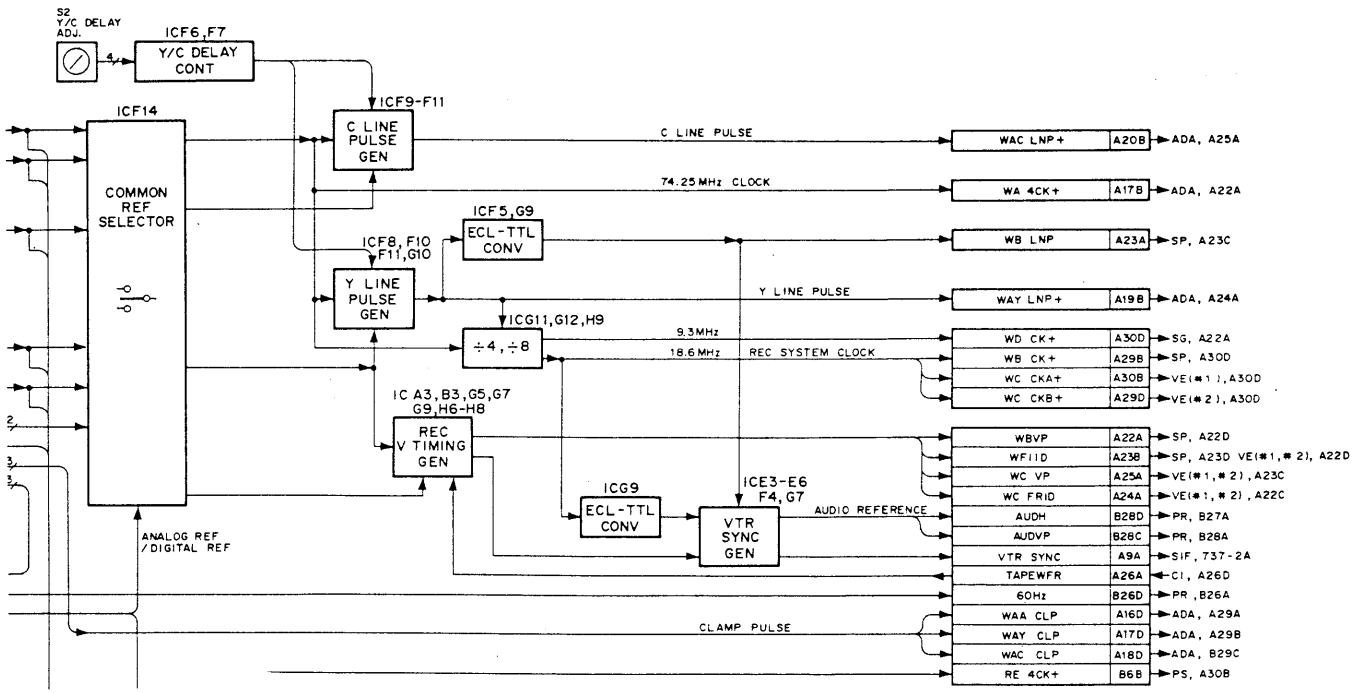


Fig. 4-1-16. Recording System Block Diagram

3. Playback System

The analog and digital reference signals are supplied to the process reference selector as well. This selector has the same function as the common reference selector. The digital signal or the analog signal is selected here, and it outputs the 74.25 MHz clock, field pulse, and line pulse. The line pulse is common to Y and C.

Two Y and C are provided in the recording side in order to compensate the delay due to difference in the band width of ADA filters for Y and R−Y (B−Y). The delay is canceled here in units of clocks (13.5 nsec). Fine difference is adjusted by the analog delay line in the ADA-12 board. To be concrete, the phases of the Y/C line pulses is changed, and according to this, the timing for writing in the picture division memory is changed to eliminate the delay. On the playback side, the PS-183 board has the Y/C delay compensation function.

In the playback side the block pulse and segment pulse are generated in addition to the line pulse and V timing pulse. A block SYNC is added to every 226-sample recorded signals. A segment (i.e., data recorded every drum rotation) consists of 640 blocks. Signals must be processed in the data form above by the time they are recorded into the deshuffling memory. Therefore, the above block pulse and segment pulse are used for the reference signals.

The memory read FR (frame), FI (field), write FR and FI generator below are the address generators for the deshuffling memory which generate the field and frame addresses for reading and writing. These addresses are required since two frames capability of main memory are provided. The video data restored by the deshuffling memory is controlled at the timing of H and V.

The process H timing generator generates the line pulse and clamp pulse for playback circuit in the ADA-12 board.

The sync phase is controlled by changing the phase of the process H timing generator (ICE9 to ICE11). Two controls, i.e., fine and coarse controls, are provided for sync phase. The coarse control is variable at 160 nsec steps. The fine control is variable at 13 nsec steps. These are adjusted with the controls on the front of the SG-151 board. Maximum variable ranges are +1.5 μ sec for advance and −0.5 μ sec for delay.

The center can be shifted by rotating the SYNC PHASE OFFSET switch (S1) on the SG-151 board. To delay the center, for example, setting this switch to 6 adds offset of 0.85 μ sec, changing the variable range to +0.65 μ sec to −1.35 μ sec. If it is set to 4, the advance offset of 0.85 μ sec is added. If wider control range is required, this switch may be rotated to shift the center. The ÷ 10 circuit divides the system clock of 18.6 MHz into one-tenth frequency, which is used as the clock of the level control A/D converter, and the clock of the level control D/A converter for the ADA-12 board.

The alarm lamp connected to the system bus input/output port goes on if an error occurs on the CPU bus. The LOCAL REMOTE selector is used to select whether the various modes are to be operated on the VTR control panel or with the DIP switches on the SG-151 board.

The local mode is mainly used when adjusting the processor independently.

In addition, 8-bit sync phase control signal is supplied to the system bus input/output port in order to enable the SYNC phase to be remote controlled externally in the future.

The SW-334 board is piggyback board mounted on the SG-151 board. It is provided with a preset switch for the video level control.

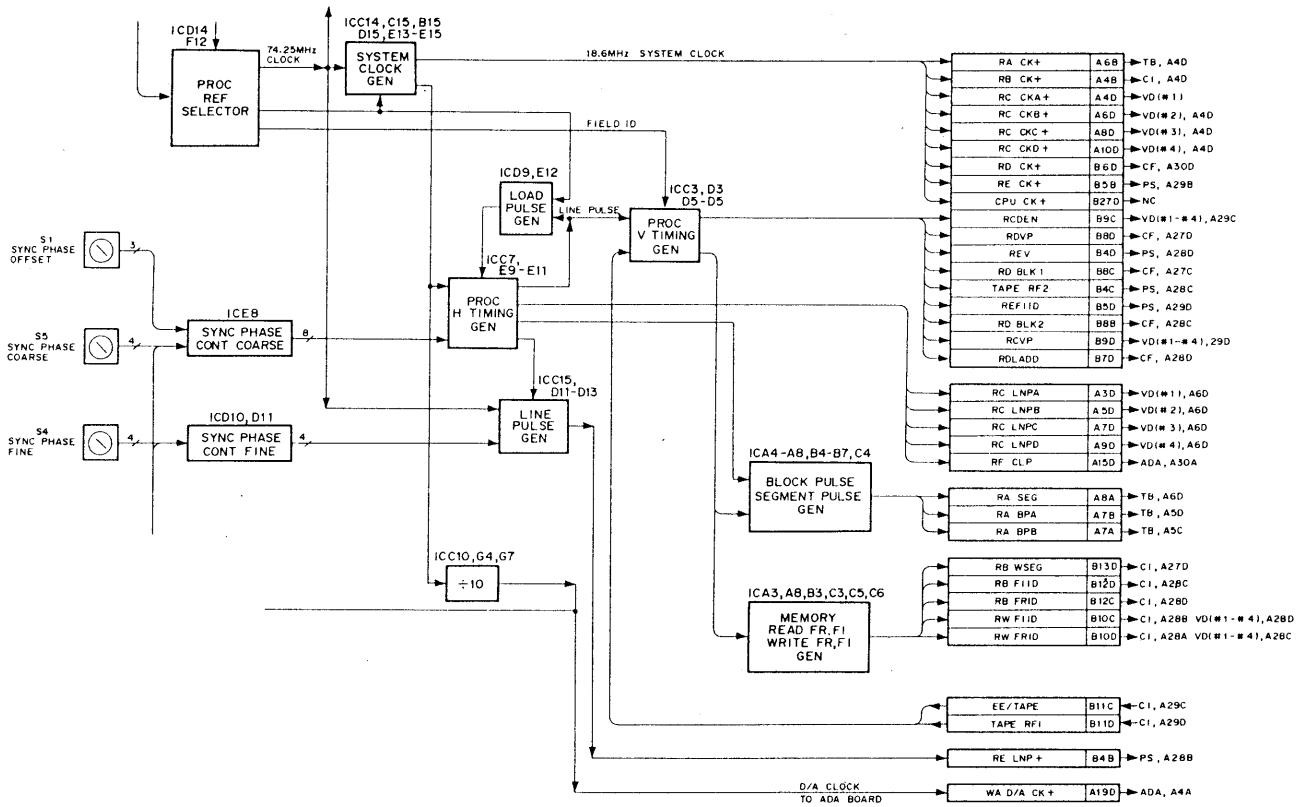


Fig. 4-1-17. Playback System Block Diagram

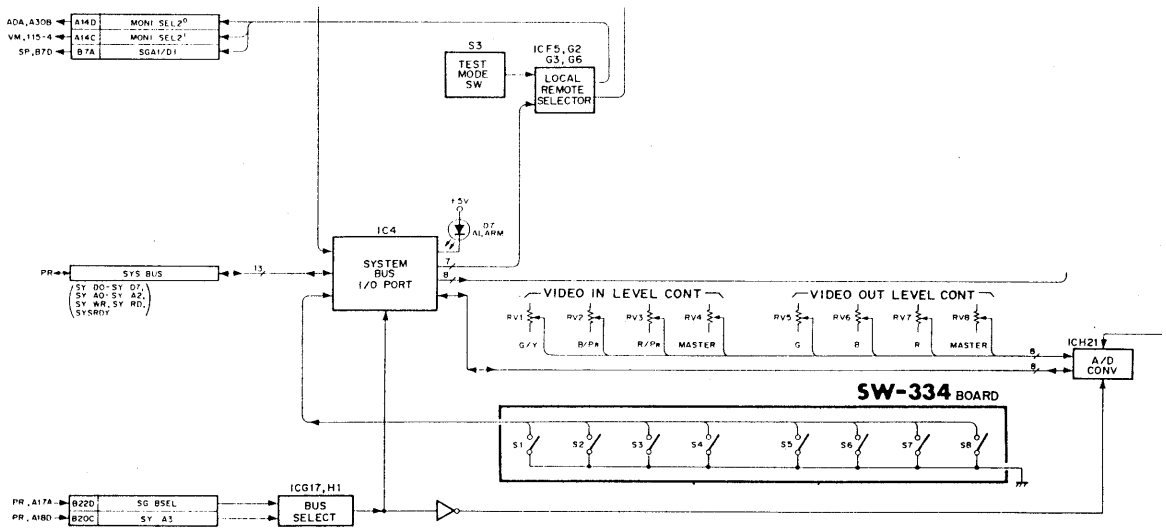


Fig. 4-1-18. Playback System Block Diagram

4-1-5. SP-06 Board

1. Outline

In the SP-06 board, either the A/D converted data in the ADA-12 board or the data from the digital video interface in the DIF-1 board is selected. And then it processes and transfers the data to the VE-18 board in the next stage.
Processing of this board is roughly classified into the following four :

- Quarters the input frequency rate 74.25 MHz signal into 18.56 MHz with serial/parallel conversion.
- Generates internal test signal.
- Channel interleave.
- Adds the outer parity using the parity encoder for error correction.

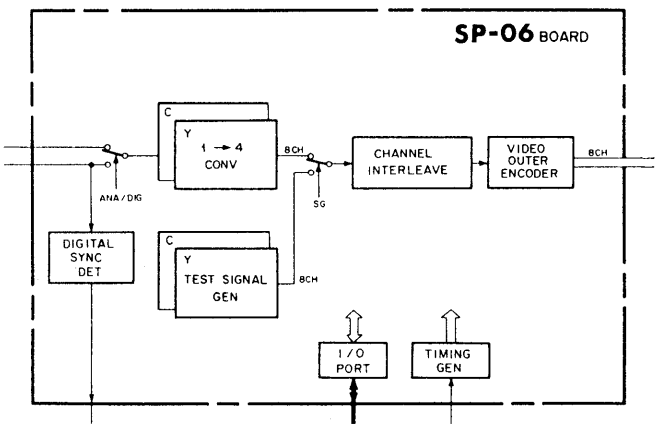


Fig. 4-1-19. SP-06 Board Block Diagram

2. Serial/Parallel Conversion

There are two kinds of input signals in this board. WBYD7 to WBYD0 are data from the ADA-12 board. WXYD7 to WXYD0 are data from the DIF-1 board. These are Y signal which is the ECL differential level. WBCD7-0 and WXCD7-0 are the chroma data. These four data are input at the frequency rate of 74.25 MHz.
They are sent to the input selector first. The input selector selects which signal to process, the analog or digital input.
Data selected by the input selector is supplied to the serial / parallel converter, which quarters the 74.25 MHz frequency rate to 18.56 MHz. To be concrete, the Y and chroma signals are divided into four channels respectively to quarter the frequency rate. The cycle time for signal processing is decreased from 13 nsec to 53 nsec.
Then, these data are supplied to the parallel/parallel converter.

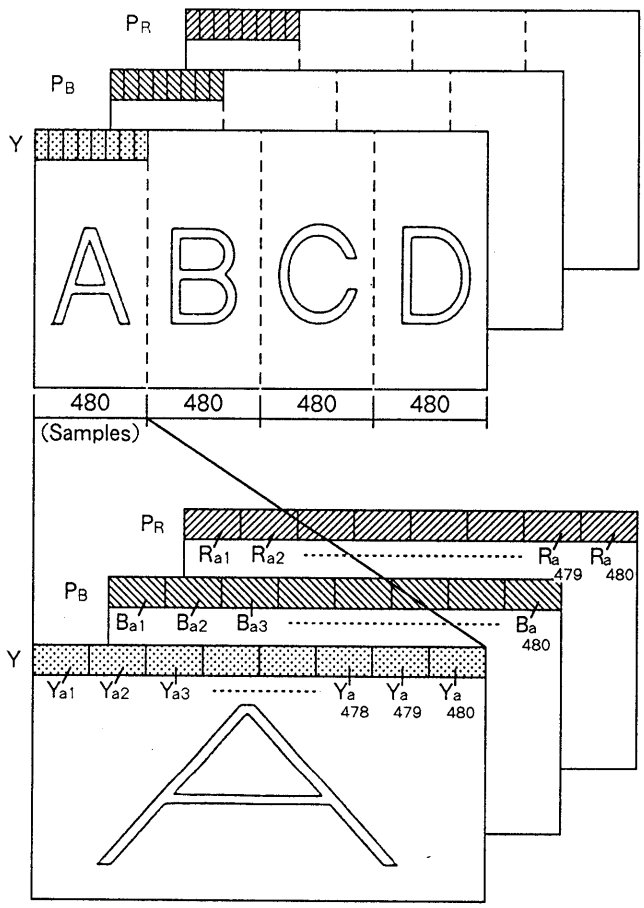


Fig. 4-1-20. Serial/Parallel Conversion

The screen division processing arranges the FIFO-structure line memory in the form of 4×4, divides the 1 line data into four parts A, B, C and D, and then writes data into the memory. As for the order of writing data, the 1st phase data of data divided into 4 phases by serial/parallel conversion is written in the leftmost column of 4×4 memory, the 2nd phase data is written in the next memory, the 3rd phase data is written in the third memory, and the 4th phase data is written in the rightmost memory. The data at positions A, B, C and D are read out from the memory simultaneously for picture division processing.

The above shows the outline of the 4-4 parallel/parallel conversion. Each one parallel/parallel conversion circuit is used for the Y and chroma signals.

3. User Data Adder and Internal Test Signal Generator

Next to the 4-4 converter, there are the circuits for adding the user data and generating the internal test signal.

The user data is supplied to the user data memory from the PR-115 board via the data bus, and is added to 38, 39, 40, 601, and 602 lines via the buffer. The internal test signal is output from the test signal generator circuit by changing the transmission from the main bus SW1.

4. Channel Interleave Circuit

Following the test signal generator circuit, there is the channel interleave circuit. If the signal of the previous stage is recorded as is, it is effective for concealment and digital matrix processing using the digital filter. However, for VTR recording, the output picture may not appear on any part of one of four divided portion in the picture if the head clogging or circuit failure occurs. To avoid such a phenomenon, data is distributed for each channel where data is recorded. Such recording is called channel interleave, for which this circuit is provided.

Note that the channel interleave is also called shuffling or distribution.

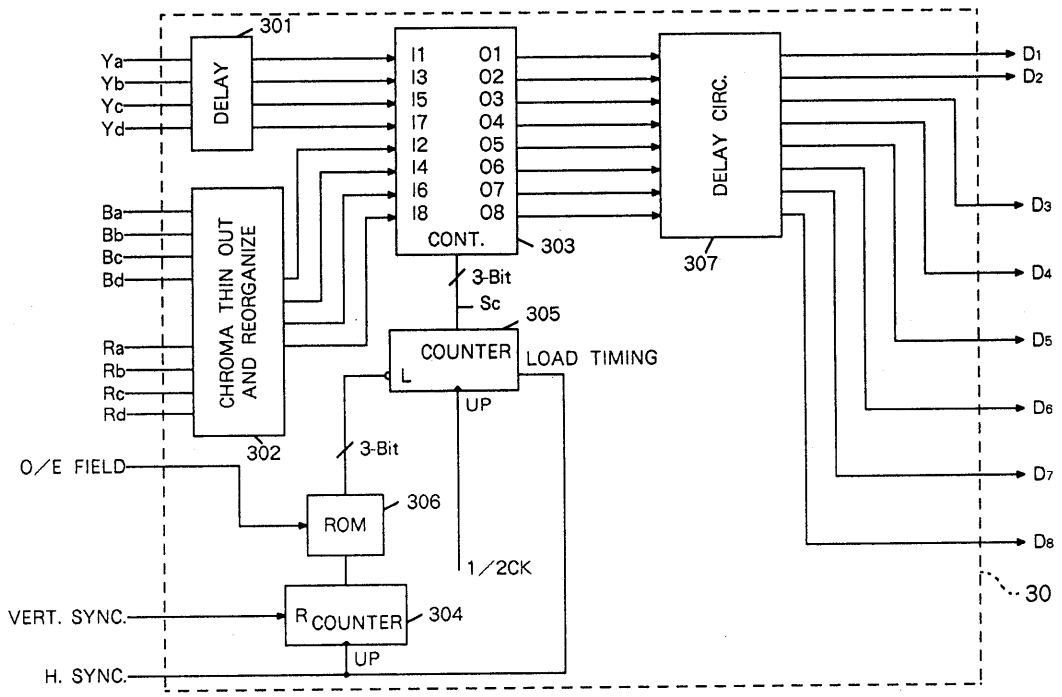


Fig. 4-1-21.

Ya to Yd in the Fig. 4-1-21 are the 4-channel Y data picture-divided by the above-mentioned parallel/parallel conversion circuit. Ya indicates the first 480 samples ; Yb indicates samples from 481 to 960, and so forth. They are read out from the FIFO line memory. Likewise, Ba to Bd and Ra to Rd indicate the picture-divided 4-channel chroma signals read out as P_B (B−Y) and P_R (R−Y) respectively. Different from the Y data, the data is half of that of the Y data since it is divided into P_B and P_R. 303 in the Fig. 4-1-21 is called barrel shifter, which circulates the output O1 to O8 against the input I1 to I8 and using the 3-bit control signal (CONT.).
Correspondence between input and output using the control signal is as shown in the Table 4-1-1.

OUTPUT \ CONT.	0	1	2	3	4	5	6	7
O1	I1	I2	I3	I4	I5	I6	I7	I8
O2	I2	I3	I4	I5	I6	I7	I8	I1
O3	I3	I4	I5	I6	I7	I8	I1	I2
O4	I4	I5	I6	I7	I8	I1	I2	I3
O5	I5	I6	I7	I8	I1	I2	I3	I4
O6	I6	I7	I8	I1	I2	I3	I4	I5
O7	I7	I8	I1	I2	I3	I4	I5	I6
O8	I8	I1	I2	I3	I4	I5	I6	I7

Table 4-1-1 (A). Barrel Shifter Operation

BARREL SHIFTER INPUT	
I1	Ya 1, Ya 2, Ya 3, Ya 4, Ya 5, Ya 6, Ya 7, Ya 8, Ya 9, Ya10, Ya11, Ya12, Ya13, Ya14
I2	Ba 1, Ba 3, Ba 5, Ba 7, Ra 1, Ra 3, Ra 5, Ra 7, Ba 9, Ba11, Ba13, Ba15
I3	Yb 1, Yb 2, Yb 3, Yb 4, Yb 5, Yb 6, Yb 7, Yb 8, Yb 9, Yb10, Yb11, Yb12, Yb13, Yb14
I4	Bb 1, Bb 3, Bb 5, Bb 7, Rb 1, Rb 3, Rb 5, Rb 7, Bb 9, Bb11, Bb13, Bb15
I5	Yc 1, Yc 2, Yc 3, Yc 4, Yc 5, Yc 6, Yc 7, Yc 8, Yc 9, Yc10, Yc11, Yc12, Yc13, Yc14
I6	Bc 1, Bc 3, Bc 5, Bc 7, Rc 1, Rc 3, Rc 5, Rc 7, Bc 9, Bc11, Bc13, Bc15
I7	Yd 1, Yd 2, Yd 3, Yd 4, Yd 5, Yd 6, Yd 7, Yd 8, Yd 9, Yd10, Yd11, Yd12, Yd13, Yd14
I8	Bd 1, Bd 3, Bd 5, Bd 7, Rd 1, Rd 3, Rd 5, Rd 7, Bd 9, Bd11, Bd13, Bd15

Table 4-1-1 (B). Barrel Shifter Input

Since the 8-8 conversion is adopted, the control data input to the barrel shifter is counted up in units of 2 samples like 0, 0, 1, 1, 2, 2, 3, 3, 4, 4, 5, 5, 6, 6···.
As result, data output to each channel (8 channels in all) is repeated like Y, P_B, Y, P_R, Y, P_B, Y, P_R··· in units of 2 samples. Refer to the Table 4-1-2.
Output data are arranged finally as shown in Table 4-1-3 through the delay circuit 307 to make each channel in phase.

3-BIT CONTROL DATA	0	0	1	1	2	2	3	3	4	4	5	5	6	6	···
01	Ya 1	Ya 2	Ba 1	Ba 3	Yb 5	Yb 6	Rb 1	Rb 3	Yc 9	Yc10	Bc 9	Bc11	Yd13	Yd14	···
02			Yb 3	Yb 4	Bb 5	Bb 7	Yc 7	Yc 8	Rc 5	Rc 7	Yd11	Yd12	Bd13	Bd15	···
03	Yb 1	Yb 2	Bb 1	Bb 3	Yc 5	Yc 6	Rc 1	Rc 3	Yd 9	Yd10	Bd 9	Bd11	Ya13	Ya14	···
04			Yc 3	Yc 4	Bc 5	Bc 7	Yd 7	Yd 8	Rd 5	Rd 7	Ya11	Ya12	Ba13	Ba15	···
05	Yc 1	Yc 2	Bc 1	Bc 3	Yd 5	Yd 6	Rd 1	Rd 3	Ya 9	Ya10	Ba 9	Ba11	Yb13	Yb14	···
06			Yd 3	Yd 4	Bd 5	Bd 7	Ya 7	Ya 8	Ra 5	Ra 7	Yb11	Yb12	Bb13	Bb15	···
07	Yd 1	Yd 2	Bd 1	Bd 3	Ya 5	Ya 6	Ra 1	Ra 3	Yb 9	Yb10	Bb 9	Bb11	Yc13	Yc14	···
08			Ya 3	Ya 4	Ba 5	Ba 7	Yb 7	Yb 8	Rb 5	Rb 7	Yc11	Yc12	Bc13	Bc15	···

Table 4-1-2. Barrel Shifter Output

3-BIT CONTROL DATA TO SHIFTER	0	0	1	1	2	2	3	3	4	4	5	5	6	6	···
D1	Ya 1	Ya 2	Ba 1	Ba 3	Yb 5	Yb 6	Rb 1	Rb 3	Yc 9	Yc10	Bc 9	Bc11	Yd13	Yd14	···
D2	Yb 3	Yb 4	Bb 5	Bb 7	Yc 7	Yc 8	Rc 5	Rc 7	Yd11	Yd12	Bd13	Bd15	Ya15	Ya16	···
D3	Yb 1	Yb 2	Bb 1	Bb 3	Yc 5	Yc 6	Rc 1	Rc 3	Yd 9	Yd10	Bd 9	Bd11	Ya13	Ya14	···
D4	Yc 3	Yc 4	Bc 5	Bc 7	Yd 7	Yd 8	Rd 5	Rd 7	Ya11	Ya12	Ba13	Ba15	Yb15	Yb16	···
D5	Yc 1	Yc 2	Bc 1	Bc 3	Yd 5	Yd 6	Rd 1	Rd 3	Ya 9	Ya10	Ba 9	Ba11	Ya13	Ya14	···
D6	Yd 3	Yd 4	Bd 5	Bd 7	Ya 7	Ya 8	Ra 5	Ra 7	Yb11	Yb12	Bb13	Bb15	Yc15	Yc16	···
D7	Yd 1	Yd 2	Bd 1	Bd 3	Ya 5	Ya 6	Ra 1	Ra 3	Yb 9	Yb10	Bb 9	Bb11	Yc13	Yc14	···
D8	Ya 3	Ya 4	Ba 5	Ba 7	Yb 7	Yb 8	Rb 5	Rb 7	Yc11	Yc12	Bc13	Bc15	Yd15	Yd16	···

Table 4-1-3. Delay Circuit Output

The above shows the outline of the channel interleave. However, the above description applies to the data in one line only (1920 samples of Y data and 960 samples of P_B and P_R data). If the same data in each line is distributed, the portions not output are arranged vertically when any channel becomes defective. To avoid this, circuits 304 and 305 in the Fig. 4-1-21 change the initial value of the control signal for every line. For details of control in units of line, see the Table 4-1-4 and Table 4-1-5. Table 4-1-4 shows data assignment, and the Table 4-1-5 indicates which data is supplied to which channel.

Data distribution is changed depending on whether the field is 1 or 2, not only in units of line. To be concrete, when the 1st line corresponds to data 1, the beginning of the second field is dislocated by half, i.e., the second field starts from the 5th line in the 1st field. By the method above, data distribution is changed between fields.

5. Outer Parity Encoder

After rearranging the data through the above processing, outer parity is added to the data of each channel.

Data of 1920 samples per line is quartered ; accordingly, data per line of each channel consists of 480 samples. Since eight-interleave processing is applied to these 480 samples, four parities are added to 60 samples. Thus, 32 parities ($4 \times 8 = 32$) are inserted in every H blanking period.

This board covers up to addition of the above parities. Data are transferred to the VE-18 board hereafter.

DATA 1	Y_{a3}	Y_{a4}	B_{a5}	B_{a7}	Y_{b7}	Y_{b8}	R_{b5}	R_{b7}	Y_{c11}	Y_{c12}	B_{c13}	B_{c15}	Y_{d15}	Y_{d16}	• •
DATA 2	Y_{a1}	Y_{a2}	B_{a1}	B_{a3}	Y_{b5}	Y_{b6}	R_{b1}	R_{b3}	Y_{c9}	Y_{c10}	B_{c9}	B_{c11}	Y_{d13}	Y_{d14}	• •
DATA 3	Y_{b3}	Y_{b4}	B_{b5}	B_{b7}	Y_{c7}	Y_{c8}	R_{c5}	R_{c5}	Y_{d11}	Y_{d12}	B_{d13}	B_{d15}	Y_{a15}	Y_{a16}	• •
DATA 4	Y_{b1}	Y_{b2}	B_{b1}	B_{b3}	Y_{c5}	Y_{c6}	R_{c1}	R_{c3}	Y_{d9}	Y_{d10}	B_{d9}	B_{d11}	Y_{a13}	Y_{a14}	• •
DATA 5	Y_{c3}	Y_{c4}	B_{c5}	B_{c7}	Y_{d7}	Y_{d8}	R_{d5}	R_{d7}	Y_{a11}	Y_{a12}	B_{a13}	B_{a15}	Y_{b15}	Y_{b16}	• •
DATA 6	Y_{c1}	Y_{c2}	B_{c1}	B_{c3}	Y_{d5}	Y_{d6}	R_{d1}	R_{d3}	Y_{a9}	Y_{a10}	B_{a9}	B_{a11}	Y_{b13}	Y_{b14}	• •
DATA 7	Y_{d3}	Y_{d4}	B_{d5}	B_{d7}	Y_{a7}	Y_{a8}	R_{a5}	R_{a7}	Y_{b11}	Y_{b12}	B_{b13}	B_{b15}	Y_{c15}	Y_{c16}	• •
DATA 8	Y_{d1}	Y_{d2}	B_{d1}	B_{d3}	Y_{a5}	Y_{a6}	R_{a1}	R_{a3}	Y_{b9}	Y_{b10}	B_{b9}	B_{b11}	Y_{c13}	Y_{c14}	• •

Table 4-1-4.

	LINE 1	LINE 2	LINE 3	LINE 4	LINE 5	LINE 6	LINE 7	LINE 8	• •
CH_1	DATA 1	DATA 4	DATA 7	DATA 2	DATA 5	DATA 8	DATA 3	DATA 6	• •
CH_2	DATA 2	DATA 5	DATA 8	DATA 3	DATA 6	DATA 1	DATA 4	DATA 7	• •
CH_3	DATA 3	DATA 6	DATA 1	DATA 4	DATA 7	DATA 2	DATA 5	DATA 8	• •
CH_4	DATA 4	DATA 7	DATA 2	DATA 5	DATA 8	DATA 3	DATA 6	DATA 1	• •
CH_5	DATA 5	DATA 8	DATA 3	DATA 6	DATA 1	DATA 4	DATA 7	DATA 2	• •
CH_6	DATA 6	DATA 1	DATA 4	DATA 7	DATA 2	DATA 5	DATA 8	DATA 3	• •
CH_7	DATA 7	DATA 2	DATA 5	DATA 8	DATA 3	DATA 6	DATA 1	DATA 4	• •
CH_8	DATA 8	DATA 3	DATA 6	DATA 1	DATA 4	DATA 7	DATA 2	DATA 5	• •

Table 4-1-5.

4-1-6. VE-18 Board

1. Outline

The analog signal from the ADA-12 and the digital signal from the DIF-1 are selected and undergone the picture-division and addition of the outer parity in the SP-06 board, and then supplied to the VE-18 board. The VE-18 board has four-channel circuits. Since the signal process is carried out on the 8-channel, two VE-18 boards are used in HDDP-1000. The VE-18 board has four functions mainly ; field shuffling, addition of inner parity, 8-8 conversion, and sync block shuffling.

2. Field Shuffling

WCD17 to WCD10 indicate channel-1 signal. Likewise, WCD27 to WCD20 indicate channel-2 signal ; WCD37 to WCD30 indicate channel-3 signal ; WCD47 to WCD40 indicate channel-4 signal. These are covered by the 1st VE-18 board. On the 2nd board, WCD57 to WCD50, WCD67 to WCD60, WCD77 to WCD70, and WCD87 to WCD80 indicate channel-5 to channel-8 signals respectively.

First, 8-bit data are input to the field shuffling memory block. This field shuffling distributes video data which is continuous on real time using memory in accordance with a certain principle and records the distributed data on the tape. By this, if a burst error occurs during playback and continuous data is lost, two-stage error correction is able to correct greater burst error. Even if a burst error exceeding the correction capability occurs, the error is prevented from concentrating in one position on the picture. It makes error correction and concealment easier.

DRAM is actually used as memory. Data is read and written at the data processing speed reduced to 1/8 for the reason of operation speed of this circuit. Data is thus shuffled in units of 8 bytes (sample). Shuffling in units of 8 bytes causes no problem since data input to the VE-18 board has been distributed in units of 2 bytes (sample) by the channel interleave circuit in the SP-06 board.

Data is also converted into the signal format for recording using the field shuffling memory. Input signals (on the writing side) have the H and V cyclicity of TV signals. On the output side (i.e., reading side), 1-field data is divided into two-segment data for the purpose of recording on tape. The segment data is further converted into the signal format consisting of 640 sync blocks, each of which is 226 bytes. Data read out from the memory has a space for adding the sync, ID, and inner parity.

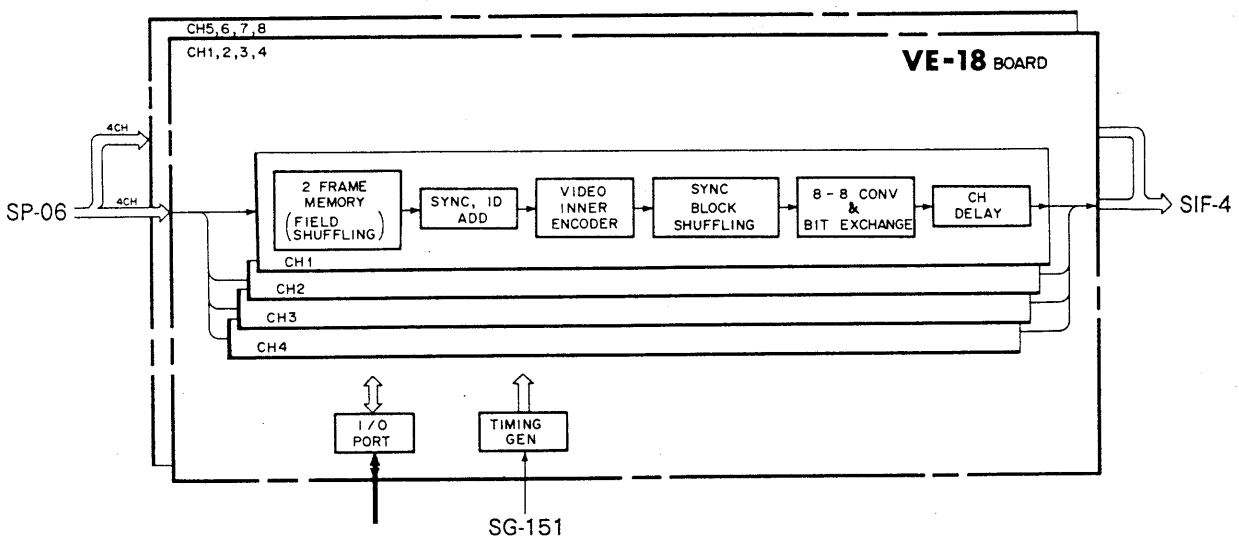


Fig. 4-1-22. VE-18 Board Block Diagram

3. Sync and ID Adder

The following sync and ID adding circuit adds 2-byte sync word and 4-byte ID address data to the space of read out data. The ID address data consists of the frame ID, field ID, channel ID and address data of sync block. The ID address data is included in the inner code, enabling error detection and correction in the playback stage.

4. Inner Encoder

The video inner encoder adds 6-byte parity to 105-byte data including the ID address. However, this encoder adds 12-byte parity to 210-byte data every sync block since an inner code is calculated and added to 2-interleaved data.

5. Block Shuffling/8-8 Conversion/Bit Exchange

The sync block shuffling circuit distributes the inner parities in units of 2 bytes into the video data. The 8-8 conversion adopted for the modulation system in the HDD/HDDP-1000 suppresses the low-frequency components utilizing correlation of the video signal. And the 8-8 conversion, however, has little low-frequency suppression effects on random data such as the parity. Therefore it is easy to occur the error at the parities portion. To prevent it, parities are distributed to the video signal. Further, bits are replaced between continuous 2-sample data. This is called bit exchange. Then, channel data are transferred to the SIF-4 board.

6. Channel Delay

For channel 2 (6) to channel 4 (8), the channel delay circuit is provided in each channel for compensating the difference in timing when the head chip contacts the tape. The VTR is provided with a head of one-base and four-chip, which has a little time lag when channels 1 to 4 or channels 5 to 8 contact the tape. The channel delay circuit compensates this time lag.
(Numbers enclosed in parentheses indicate those of the VE-18 #2 board.)
Besides, heads of channels 1 to 4 and channels 5 to 8 are located at the 180° opposite sides on the drum, causing a great time lag, i.e., 1/2 segment. This time lag is adjusted using the frame memory for shuffling.

7. Input/Output Port

Data for controlling the signal processing on the VE-18 board are supplied to the input/output ports from the CPU on the PR-115 board via the data bus. The same control is enabled with the switches on the VE-18 board in the local mode.

8. Timing Generator

The timing generator produces various timing signals necessary for signal processing from various timing signals such as V, H, etc.

4-1-7. SIF-4 Board

8-channel signals with the sync, ID, parity, etc. added are input to the SIF-4 board. Since these signals are in units of word (8 bits), it is necessary to convert 8-bit signals into bit serial signals for recording them. The SIF-4 board is provided with the clock generator (148.5 MHz) necessary for the above conversion. This 148.5 MHz clock is generated from the PLL based on the half of the 18.6 MHz system clock as the reference.

The 8-1 converted signal by the shift register is supplied th the VTR via CN2. This signal is also supplied to the PIF-3 board in the bypass mode, enabling the E-E picture to be confirmed using the processor only without connecting the VTR.

The signals for interface with the VTR passe through this board ; they are VTR sync, character signal, cue signal, RS-422 line, WFM signal, etc.

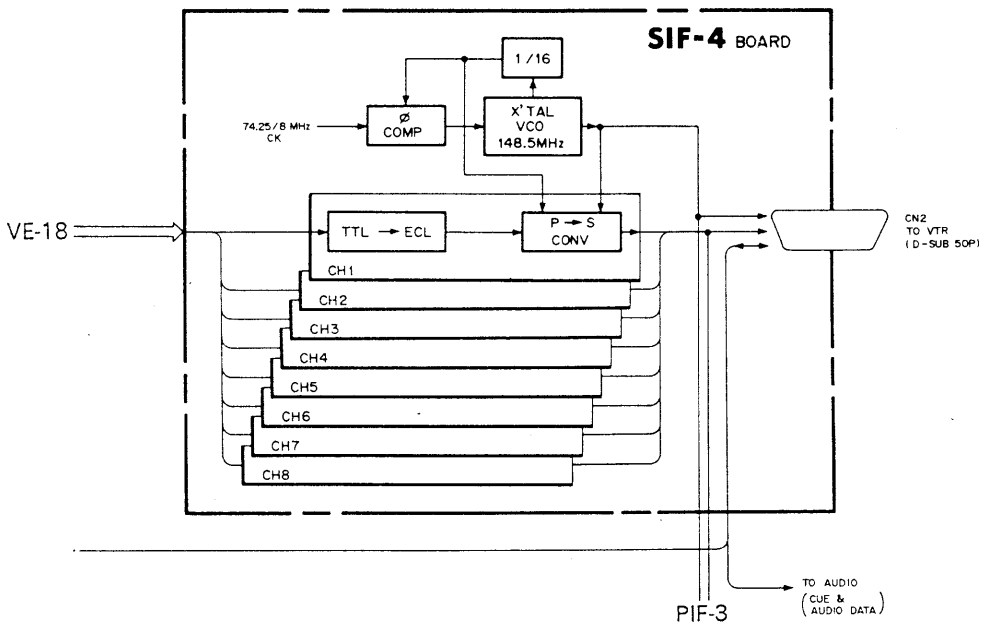


Fig. 4-1-23. SIF-4 Board Block Diagram

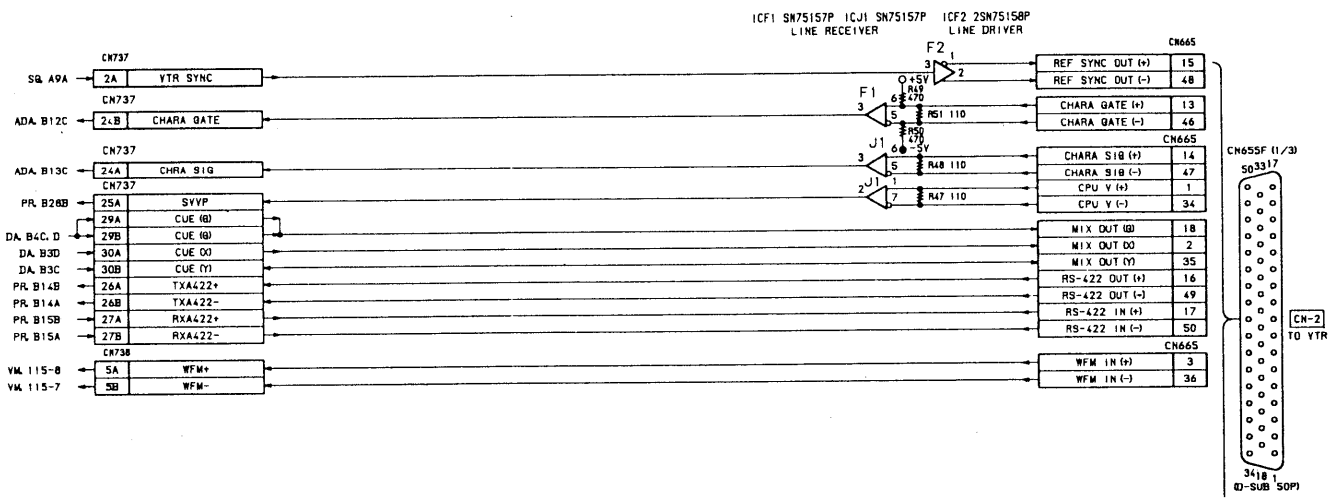


Fig. 4-1-24. Interface Signal

4-1-8. PIF-3 Board

On the contrary to the SIF-4, the PIF-3 board restores the 148.5 MHz bit serial data into bit parallel data. This board performs 1-4 conversion. The following TB-07 board converts data into 8-bit data.
The playback signal from the VTR via CN3 is sent to the data selector where playback signal and bypass signal from the SIF-4 board are switched. The shift pulse is supplied from the SIF-4 board in order to match the start phase of 8-bit data with that of the original signal in the bypass mode. This pulse can be turned on and off. It is normally turned off (i.e., start phases are not matched).
Signals with bit shift, that means parallel-converted signal with different phase from that of the 1-8 converted signal in the SIF-4 board, are corrected by the following TB-07 board.

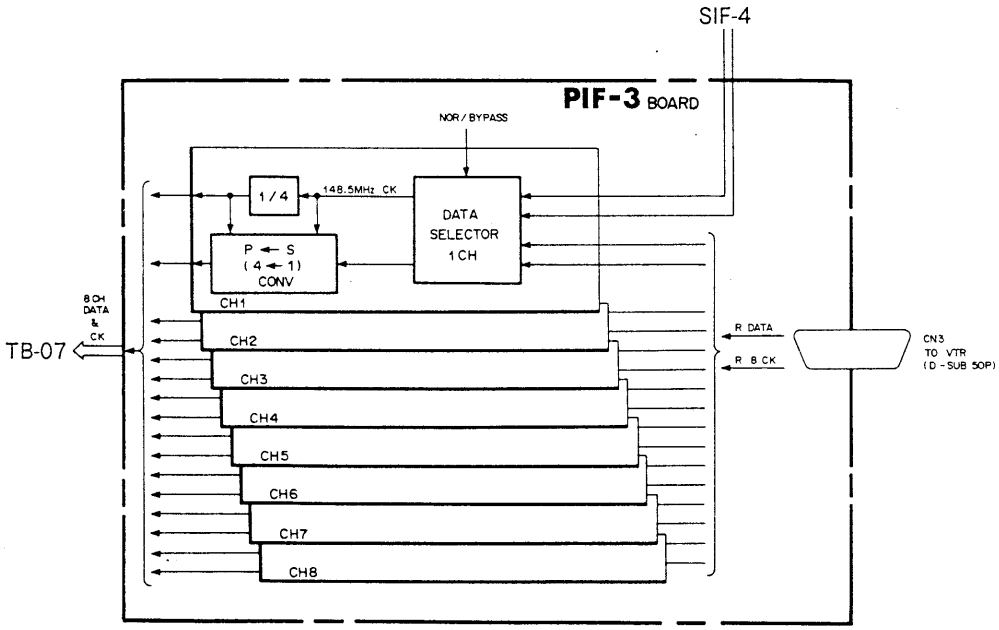


Fig. 4-1-25. PIF-3 Board Block Diagram

4-1-9. TB-07 Board

1. Outline

The TB-07 board has the following circuits. These are the common circuit to 8 channels except timing generator.

- Serial/Parallel converter
- TBC1 (Clock exchanger)
- Bit rotation
- Sync detector
- TBC2 (Block exchanger)
- ID/address 8-4 converter
- Timing generator

2. Serial/Parallel Converter

The 37.2 MHz data transferred from the PIF-3 board is converted into 18.6 MHz word (8-bit) structure data by the 1-2 serial/parallel converter.

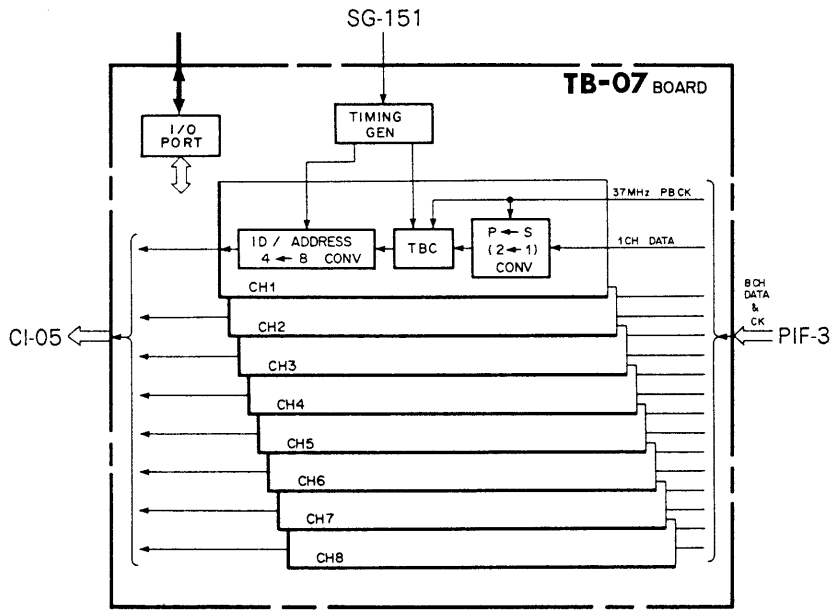


Fig. 4-1-26. TB-07 Board Block Diagaram

3. Clock Exchanger

The TBC-1 is FIFO memory in the next stage which compensates jitters. Data are written in this FIFO memory based on the clock extracted from the playback data by the PLL and read out based on the reference clock, enabling data with stabilized phase to be output. The write and read addresses in the FIFO are reset in the head blanking period. The phase difference between the input and output signals is approx. 22 blocks at this time. The capacity of the FIFO memory is approx. 44 blocks.

4. Sync Detector

The sync pattern detector detects the sync from the FIFO output signal, and then bit shift detection is performed. The sync and bit shift detection is regarded as being valid only when the syncs are detected twice continuously at the interval of 226 samples to prevent erroneous sync detection. Since the sync detection needs a delay by 1 block, the data is also delayed by 1 block.

5. Bit Rotation Circuit

The bit rotation circuit (barrel shift circuit) restores data to the same construction as recorded data, which is supplied to the second-stage of TBC block skew corrector.

6. Block Skew Corrector

The TBC-2 skew corrector resets the write address in the FIFO memory at the detected sync and also resets the read address at the reference sync (block pulse), matching the block phase of playback data to that of the reference.
This resetting is performed only when skew takes place in the playback signal. It is not performed for continuous signals.
The skew detection is performed by comparing the output of the counter running freely and the phase of the detected sync. Normally the counter is reset by the detected sync.

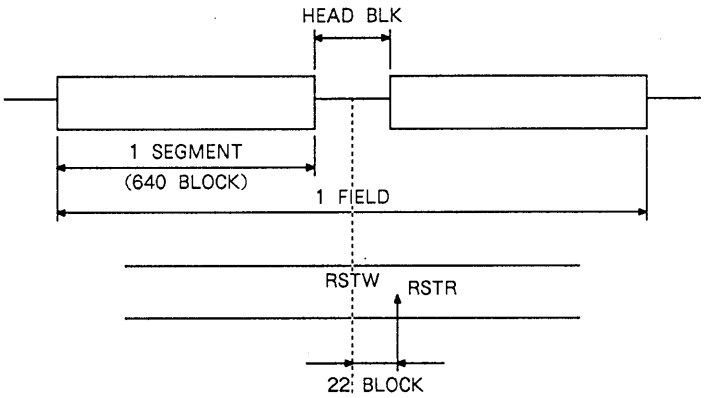


Fig. 4-1-27. Clock Exchanger

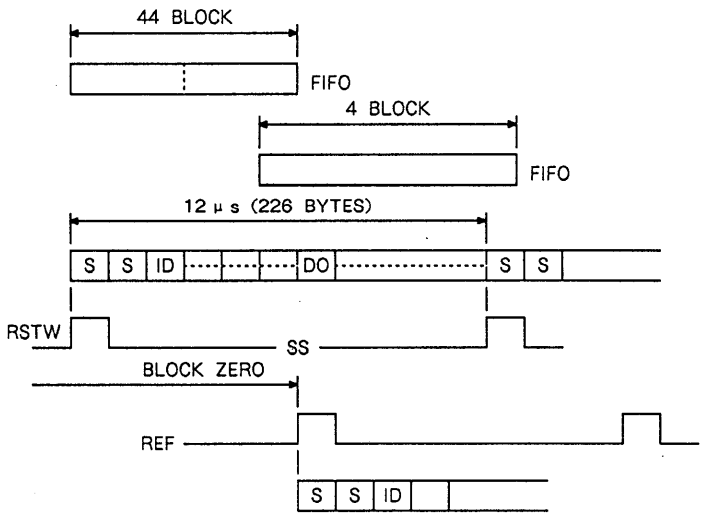


Fig. 4-1-28. Sync Detector

7. ID/Address 8-4 Converter

The output of the TBC2 is supplied to the ID/address 8-4 converter, which performs 8-4 conversion of the ID/address area (4 bytes).

8. Timing Generator

The circuit generating the timing pulse for controlling the above operations is roughly divided into two systems (A and B). The playback heads for channel 1 to channel 4 signals or channel 5 to channel 8 signals are adjacent to each other on the playback heads, allowing these signals to be handled at the same timing. The timing pulse for channel 1 to channel 4 signals is marked as A. That for channel 5 to channel 8 signals is marked as B.

4-1-10. CI-05 Board

1. Outline

The channel interchanger CI-05 board performs playback processing other than the normal playback such as fast forward, reverse, slow playback and still modes.
In the normal playback mode, channel 1 to channel 8 signals from the VTR heads bypass the channel interchange function and are output to the next stage.
In the fast forward, reverse and slow playback modes, the VTR boards do not trace the home tracks but cross other tracks and reproduce signals in them, making it impossible to reproduce proper picture. To avoid the above phenomenon, the CI-05 board returns signals to their home channels.
In addition, this board performs 1 block deshuffling and 8-8 conversion, etc.

This board mainly consists of the following five circuits :
- Channel shift detector
- 1 block deshuffling circuit
- Bit exchanger & 8-8 converter
- Channel exchanger
- Block skew corrector

Signals returned to their home channels by the above circuits are output to the VD-04 board.

2. Input Signal

The 8-channel signals input to CI-05 board are latched. The block pulses A and B are also input, which control the above-mentioned each 4 channels of signals. Because each 4 channels of signals have different phases, two lines of block pulses are necessary. The block pulse delay circuit directly following the above causes a delay in the block pulse to produce timing necessary for each line.

3. Channel Shift Detector

Each 3 bits per channel of 8-channel input data are input to the mid-stage channel shift detector circuit immediately before the 1 block deshuffling circuit. This circuit detects the channel ID (0 to 7) from these 3-bit data to check whether data of each channel is not shifted from signals of other channels. This shift originates from tracing across other channels' tracks of the VTR heads during special playback modes as described above. The heads, however, pick up only data with the same azimuth (e. g. , the 1-channel head picks up data of channels 1, 3, 5 and 7 only). Data of each channel do not get out of order, but always shift in parallel.
This detector detects the shift amount of data by 4 channels for the reason of ROM capacity and outputs the detected shift amount to the following ROM for judgment.

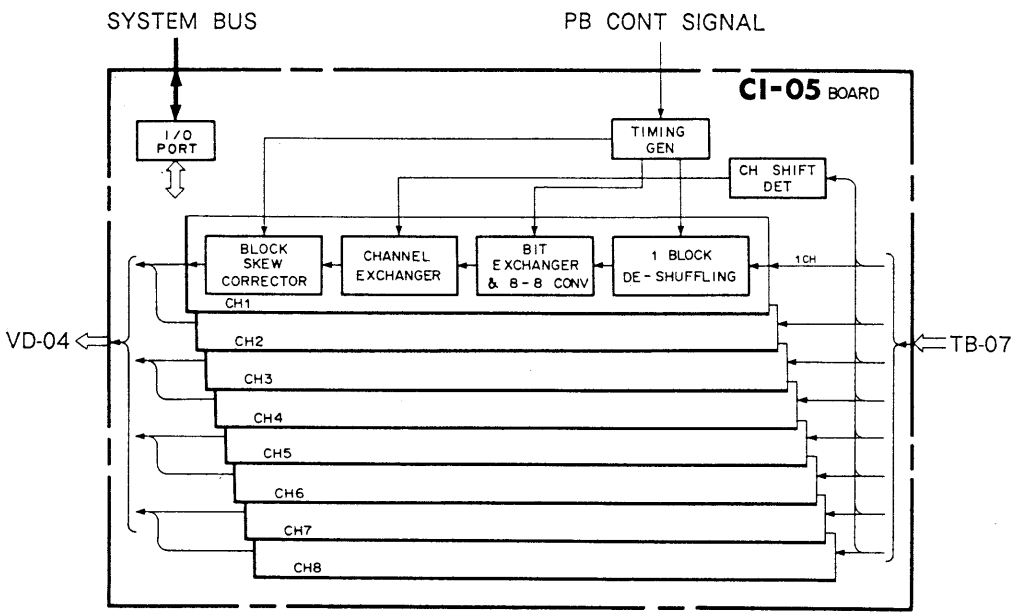


Fig. 4-1-29. CI-05 Board Block Diagram

4. 1 Block Deshuffling Circuit

Each 4 channels of upper and lower latched on the left side are supplied to the 1 block deshuffling circuit (for 8 channels). This circuit restores these data shuffled when recording to the original state.

5. Bit Exchanger/8-8 converter

Following the 1 block deshuffling circuit, there is a bit exchanger & 8-8 converter, which restores bit exchanging and 8-8 conversion performed when recording to the original state. This circuit thus outputs the normal sampled video signals.

6. Channel Exchanger

The channel exchanger restores 1 to 8 channel data shifted during special playback modes to their home channels using a set of barrel shifters.

7. Block Skew Corrector

This circuit adjusts the phases of data shifted at the time of channel exchanging. Since the 1 to 4 channel VTR heads and 5 to 8 channel heads are located 180° opposite to each other, the phase shifts if the channel-5 signal is input to channel 1, disabling processing in the following stage. To prevent such a phenomenon, this circuit reads out data, once written in the FIFO memory, with correct phases.

8. Frame Memory Control Signal Insert Switch

This ciucuit inserts the read/write control data for four frame memory (0 to 3) on the VD-04 board in the areas of unnecessary SYNC data (2 bytes) and output it to the VD-04 board.
This circuit produces the read and write addresses in the field memory and mode signals (freeze, slow stunt, normal playback, etc.) and insert them in the clearances between data (i.e., SYNC areas) to transmit to the VD-04 board. The VD-04 board writes data to the memory based on the block addresses, frame IDs, field IDs, and tape directional signals (detected by the direction detector) received from the CI-05 board. Likewise, it reads out data based on the signals received from the CI-05 board.
The CI-05 board also controls to avoid overlap of writing and reading in/from the memory. It identifies from the channel-1 signal only, as a matter of convenience, in which memory data are written and determines read-out. Since the read address cannot be known if the channel-1 recording head is clogged when recording, it uses channel-2 signal in such a case. If channel-2 head is also clogged, it uses channel-3 signal. Detection against clogging are taken up to channel 3 only since, if heads of channels 1 to 3 are all clogged, the VTR is practically useless.

4-1-11. VD-04 Board

1. Outline

The signal corrected its time base with TB-07 board and restored each channel's data in the stunt mode with CI-05 board is input to the VD-04 board. Four VD-04 boards are used in one VTR to cover 8 channels since one board incorporates circuits for 2 channels. The VD-04 board performs two-stage error corrections ; the inner correction and outer correction. It also has deshuffling function since data are 1 shuffled. It has 2 frames of frame memory for this deshuffling processing. By controlling this memory, it enables picture reproduction even for slow and shuttle modes (to the extent that an picture can be confirmed in the shuttle operation).

2. Inner Correction

The RCD17 through RCD10 on the VD-04 (# 1) board indicates 1 channel 8-bit data of two channels. The RCD27 through RCD20 on the VD-04 (# 1) board indicates the 8-bit data of another channel. This signal is output from the CI-05 board.

First, input 8-bit data is latched, then input to the deinterleave circuit. Since the data has been added codes to every other samples of data as the inner correction parities, interleaved data should be once restored to the original state. Thus, deinterleave circuit cancels the interleave and the Reed Solomon decoder corrects errors. This operation is called inner correction. The following interleave circuit restores the deinterleaved signals to interleaved signals again.

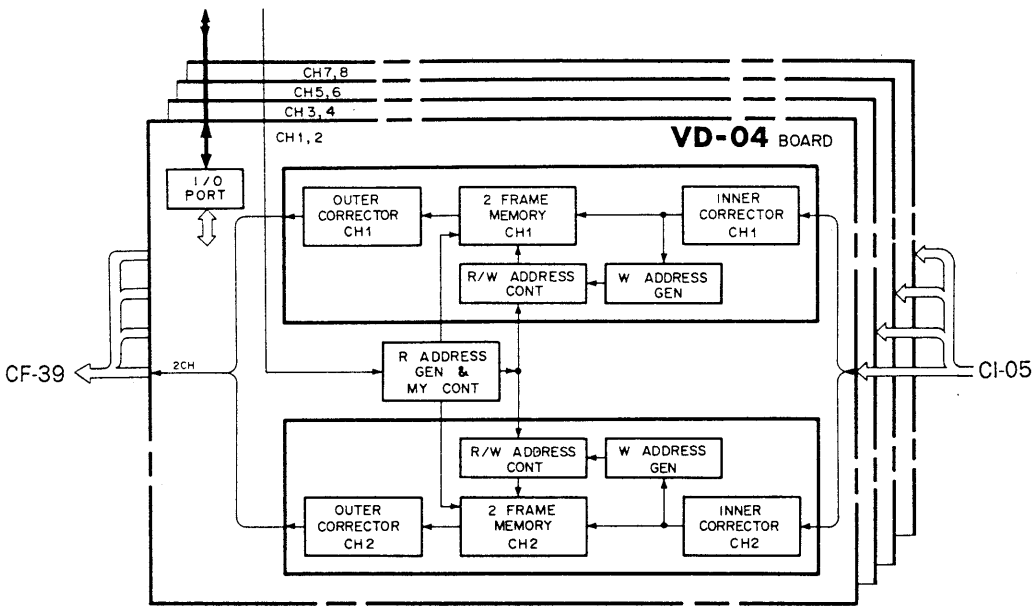


Fig. 4-1-30. VD-04 Board Block Diagram

The following describes why the interleave must be canceled.
Arrangements of interleaved and deinterleaved data are shown in the Fig. 4-1-31. 2-byte IDs, 208-byte data, then each six parities, 12 in all, are assigned in the input data. The 4-byte ID data are converted to 2 bytes, and the read/write addresses in the frame memory and status data are in the emptied 2 bytes. By the way, as shown in Fig. 4-1-31 (B), odd-numbered parities correspond to odd-numbered data and even-numbered parities correspond to even-numbered data. Therefore the decoder LSI cannot correct errors if parities and data are positioned in a group like this. Thus, the odd-numbered and even-numbered IDs, data, and parities should be rearranged together respectively. That is, the decoder IC cannot be available for the interleaved condition. Thus, data, parities, etc. are once deinterleaved here.
There is another same circuit in the lower part for another channel.

3. 2-frame Memory

The error-corrected data having passed through the deinterleave, decoder, and interleave circuits is input to the S-P-S (serial-parallel-serial) conversion circuit, which converts data into parallel (8-channel) data and writes them in the 2-frame memory. It performs the field-deshuffling.
By the way, the inner parity block must be complete in a relatively short unit since the head crosses the video tracks in the special playback mode (slow or shuttle) and, if the inner parity block has too long unit, is hard to read all the data in the block.
In a word, if the parity, which is used to check whether one block is correct or not, is too long, all data in the block cannot be read. Thus, the inner parity block should be as short as possible. On the contrary, the outer parity is used for correcting burst errors ; continuously-lost data should be distributed in as large units as possible. However, taking account of operation such as editing, exceeded large distribution up to several frames causes troubles. After all, a field is the largest unit for easy picture processing. Therefore, shuffling is performed in units of fields.

4. Outer Correction

Data read from the 2-frame memory is input to the second-stage error correction circuit. Though the inner correction is 2-interleave based, the outer correction is based on 8 interleave. To process data by the decoder like the inner correction, the interleave should be restored to the original state. Since the outer correction is 8-interleave based, every 8th data are read out in sequence. Data having passed the de-interleave processing is input to the Reed Solomon decoder LSI, which performs the outer correction. Data is then interleaved again, and is output from the VD-04 board.

5. Inner and Outer Corrections

The inner correction mainly corrects the random errors. Since 6 parities are added to 105 samples, including the ID, it can corrects up to 3 errors. However, 2-error correction is adopted since correction of 3 errors raises the mis-correction rate.
The outer is added by 4 parities to 60 samples for erasure correction. Since the inner has been corrected the random errors and detected the burst errors, the outer correction performs erasure correction using the error flags. It can correct up to approx. 6% of burst errors.
If the error flag is less than 4, the erasure correction is possible since 4 parities are added to 60 samples for the outer correction. If the errors flags is more than 5, the detection mode is established.

Input Data Allocation

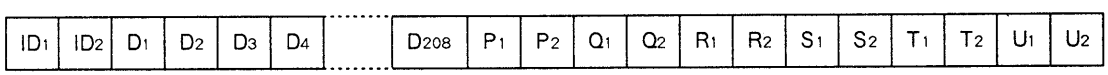


Fig. 4-1-31 (A). Input Data Allocation

Data Allocation after Deinterleaved

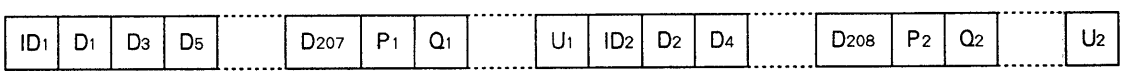


Fig. 4-1-31 (B). Data Allocation after Deinterleaved

6. Input/Output Port

This VD-04 board is also controlled by the CPU on the PR-115 board. It is thus provided with the bus I/O port. It may be controlled by the CPU via this bus or controlled with the switches S1 and S2 on the board.
The error correction mode can be changed for the manual test using the switches on the board. Switch S1 controls and sets up the inner and outer decoder correction modes. S2 selects the decoder output : through output, all zero, and error pattern output.

7. Main Memory Block

The main memory block consists of 2 MB memory, read/write address generator for controlling this memory, memory control for flags detected by inner correction, address circuit (common to 2 channels), etc. Flags are not output if data are corrected. If errors are not corrected and exceed the correction capacity, a flag is output corresponding to all data of the inner code block. For erasure correction by the outer correction, 1 : 1 timing of data and flags should be input to the outer correction circuit. 2-frame capacity is therefore given to flag memory similarly to data capacity.
From ICA8 to ICA12 is a memory write address generator (block address generator). The channel ID, frame ID, field ID, segment ID and block address (0 to 639) can be known by latching the 2-byte ID added to the beginning of the 1 sync block data.
ICF11, ICF13 and ICF15 form a circuit controlling the block address generator. If errors cannot be corrected by the inner correction circuit, the block address added to the data is not used. This counter is used in such a case.
ICA13 and ICA14 form a circuit for separating the above-mentioned channel ID and frame memory write ID (channel ID memory frame/field separator).
ICB31 and ICC31 (memory read frame/field mode signal separator) form a block for separating data inserted by the CI-05 board. Signals are supplied from ICC32 (latch). These data includes the frame memory read address, read frame and field address, mode signal, etc.
ICF10 and ICF14 generate write addresses in the sync block (0 to 225).
ICH14 latches the flags transmitted from the inner correction circuit at certain timing.
ICE15 (channel ID detector) adds IDs to four VD-04 boards using 2 pins to classify them according to the slot of the mother board. The slot No. can be known by inserting the board and observing its signal. It compares the ID (channel) of the transmitted data and the slot No. (channel), and if they are different, writing into the memory is stopped. During normal playback, only the home channel signals are supplied. During the stunt playback, however, signals of each channel are returned to the home channel by the CI-05 board. In some case, signals of incorrect channels may be transmitted due to erroneous detection caused by noises. ICE15 (channel ID detector) detects the channel ID and slot No. to prevent incorrect signals from being written in the frame memory by misdetection.
ICF4 and ICH2 generate the memory write pulse. It judges from the signal from the channel ID detector, inner error flag, etc. whether or not to write data in the frame memory. If data is not to be written, write pulse is not generated. All data are written during the normal playback, as a matter of fact. During the slow and shuttle playback modes, only the inner code blocks, which is no error, 1-error, or 2-error, are accumulated in the memory gradually.
ICE3 and ICE4 are 2-frame flag memory. This memory has relatively small capacity of one block since the flag is in either condition : one inner code block is set to high, or low.
ICH5 is a buffer for inputting and outputting the flag memory data (flag memory buffer).
ICH3 and ICK2 are the P-S converter for flags. It is required for matching the main memory data and flags in 1-to-1 correspondence since the main memory is controlled according to 8 samples (8 channels).
ICB6, ICD6 and ICF6 (row/column selector) is a selector for writing addresses in the DRAM by time sharing. It changes the row addresses and column addresses.
The write/read address selector changes addresses by time sharing when writing or reading the 2-frame memory. The read address is generated by the counter and ROM from the H and V timing in the reference.

4-1-12. CF-39 Board

1. Outline

The signal having passed through error correction and 1-field deshuffling by the VD-04 board are input to the CF-39 board. The CF-39 board mainly performs concealment for this signal which includes errors.
If errors exceeding the correction capability of the VD-04 occur, the CF-39 receives the flags corresponding to the data to correct the errors.
See Fig. 4-1-32 block diagram. First, since 8-channel data are processed all together before the CF-39, and Y and chroma are mixed in data of each channel, the CF-39 separates Y and chroma respectively.
This separation is called channel de-interleave. Y and chroma are completely separated in this circuit and made into vertically quartered Y and chroma on the picture screen.
For the reason of quartering the screen vertically and in order to correct data at the beginning and at the end at the time of error correction, it is necessary to overlap data in front of and behind data in another channel. The overlapping circuit follows the channel de-interleave circuit.
Then, errors are concealed in the next stage. There are 4-channel Y and 4-channel chroma, which are sent to the following PS-183 board.

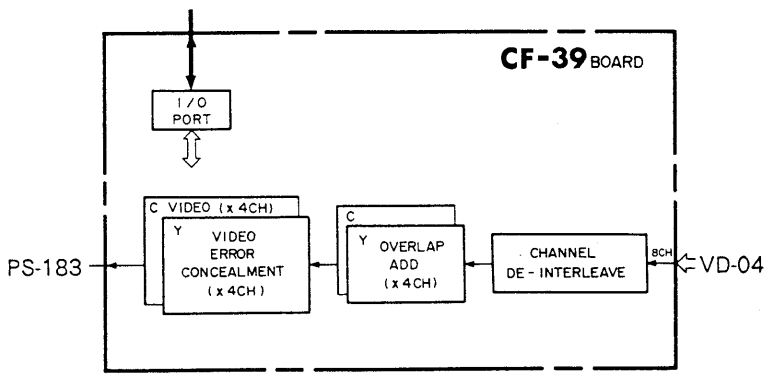


Fig. 4-1-32. CF-39 Board Block Diagram

2. Channel De-interleave/ Overlap Addition

The RDD bus consists of 8 channels×8=64 bus lines, which correspond to 8-channel data transmitted from the VD-04 board.
RD-FL1 to RD-FL8 are error flags which have 1 : 1 correspondence with data. Error data not corrected by the VD-04 board are supplied with flags. These data and flags are once latched for channel de-interleave. The 1 clock's or 3 clock's delay is changed by every line for separating the Y and chroma signals.
The following barrel shifter restores data by the reverse rotation of the data which has been distributed by the SP-06 board. 6 clocks' delay is for timing adjustment to the chroma processing.
Refer to Fig. 4-1-33. This is a function of chroma processing. The chroma signal become a signal formed a series of each four samples PBS and PRS after channel de-interleave processing. These signals are moved to arrange PBS and PRS alternately by every sample time base multiplexing. Then, resulting signals are overlapped to data in order to conceal data at the end.

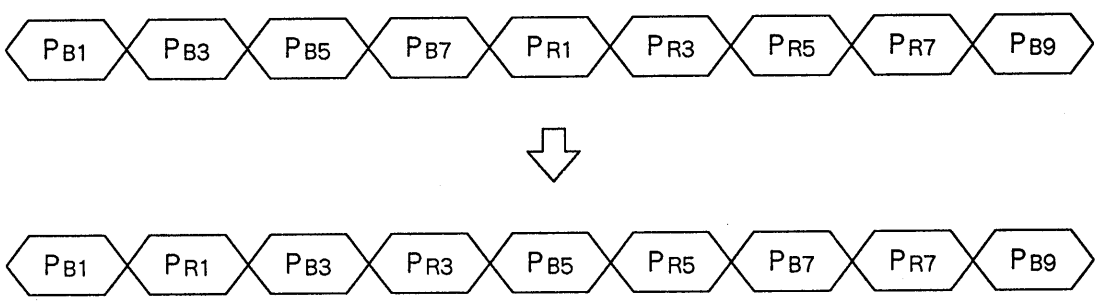


Fig. 4-1-33. Chroma Overlapping

3. Error Concealment

The following describes the error concealment processing of the HDD/HDDP-1000, provided data E on the n line is erroneous.
Provided data 1 sample before data E on the n line is D, data 1 sample after E is F, data in the same position as sample E on the n−1 line is B, data before and after it are A and C respectively, data in the same position as sample E on the n+1 line is H, and data before and after it is G and I respectively, concealment is performed in accordance with the algorithm in the flowchart 4-1-35. First, the erroneous data E is replaced with the average of conforming two data in the vertical, horizontal or diagonal direction.
If the average is impossible, E is replaced with any conforming one among the peripheral data B, H, D, F, A, C, G and I. If all of them are erroneous, data E is replaced with data B (already concealed).

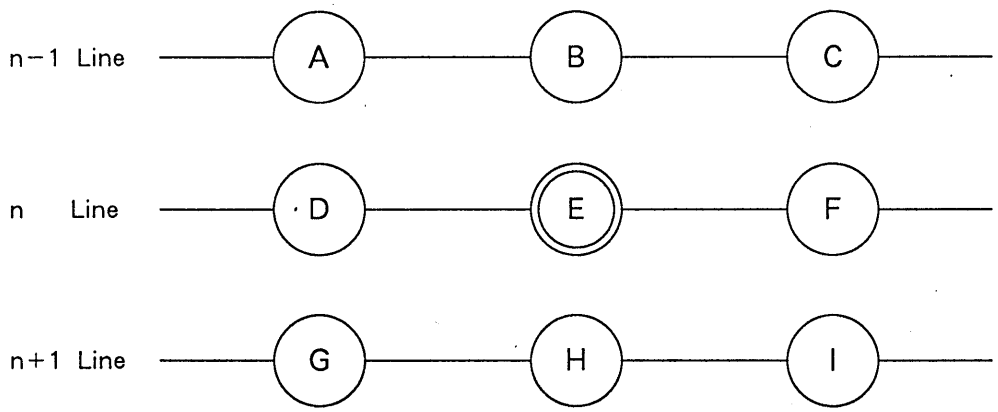


Fig. 4-1-34. Error Concealment

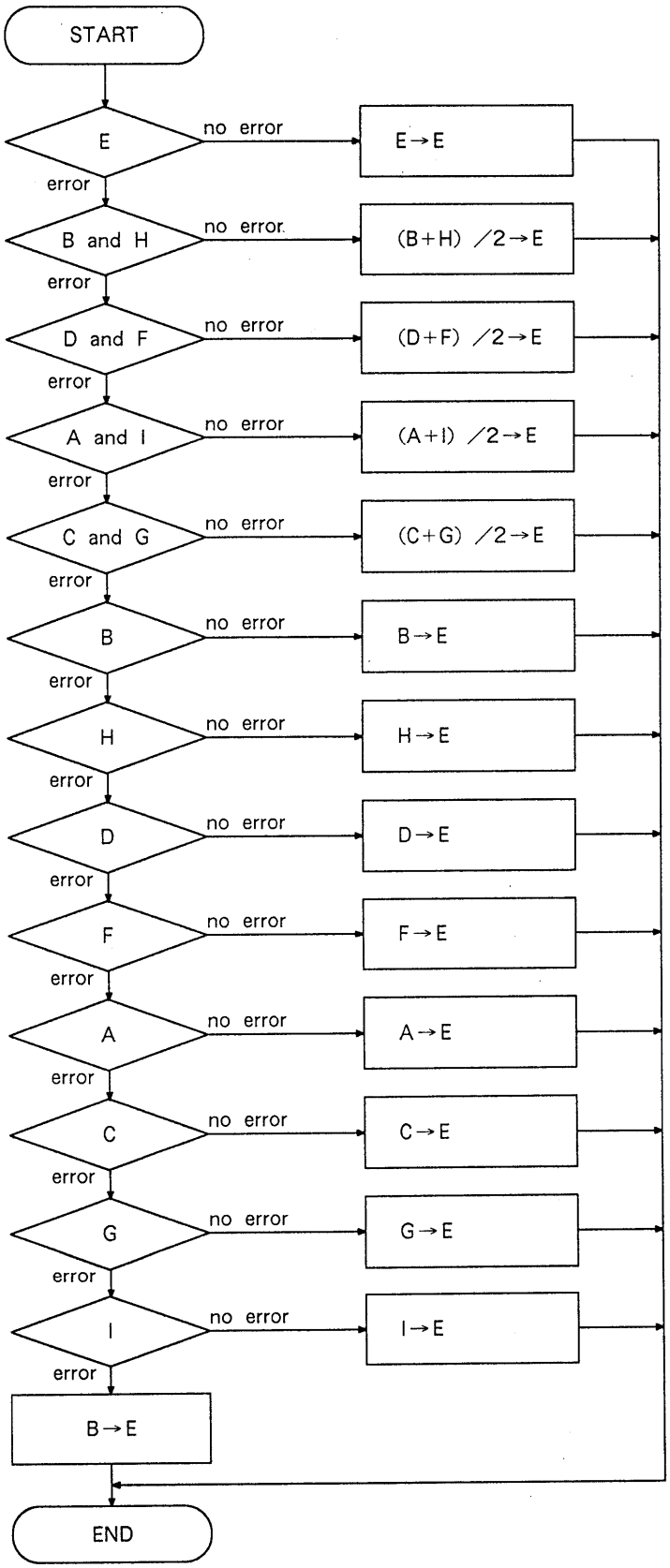


Fig. 4-1-35. Error Concealment Flowchart

First, overlapped data are input to ICD23. This is switching IC which selects normal operation or flag operation. The flag operation can be used for error observation mode.
If the LSB is erroneous, the error can hardly be checked by observing the picture ; the lowest level is inverted only. For easy observation, the error flag and image data can be replaced with each other. For that purpose, data and flag are changed.
The latch operation is performed when the normal/flag signal is normal mode. If it is flag mode, 8-bit video data is changed into data with a certain code using flag signal. If there is no error, data has a pedestal code, which is displayed black. If there is an error, data has a code displayed white.

A, B, C, ··· I of the strategy of error concealment are observed on the picture screen. I is the latest data on the time base. In the order of H, G, F, E, D, C, B and A, data become earlier. Then, A, B, C, D, E, F, G, H, and I data can be selected and sent to the data selector.
4-bit error flag from the overlap circuit is supplied to the data concealment control circuit. The ROM stores the correction modes in accordance with flag data in the order of priority. Information for deciding the correction modes in accordance with the error pattern is transmitted from ROM.
For averaging in the vertical, horizontal and diagonal directions, the corresponding data to the upper and lower 8 bits in the data selector are selected. Control is based on the error flag. If error prevent from averaging, simplified replacement is carried out. The data selector selects the same data. ICB21 to ICB23 form an adder. If different data are input, it averages them. If the same data are input, it adds them once and divide into half the added value, obtaining the original data.

Concealed data is sent the ICB20, i.e., 1 H delay circuit. This circuit outputs the n −1 line data. If all data around a data are erroneous in the worst case, the erroneous data can be corrected using the previous concealed data.

Another signal is supplied to the selector consisting of ICA20, 22 and 23. Just before the selector, the line is branched and the signal is input to the line adder circuit consisting of ICA19, 21 and ICB19. The field of the playback data may not correspond to the reference signal field during slow playback. The reference signal is always performed in the continuous fields 1, 2, 1, 2 and so forth. During slow playback, the same field may be read repeatedly. If the fields are different, the line may shift from the correct position. In such condition, an output picture shifts vertically by 0.5 H. To prevent such phenomenon when the fields are not correspondent, the upper and lower lines are added and half divided for averaging to produce an intermediate line, i.e., line addition. The line adder functions for this processing. The line addition is performed during slow playback only. The following selector selects which data to output, line-added data or non-added data. The line add Y signal is used for selection. Data is normally output straight and latched by the following latch circuit, then sent out to the next PS-183 board.
The chroma concealment circuit has the same functions as the Y concealment circuit basically. Since the chroma signal has P_B and P_R alternately, each 1 sample data is added between A, B and C data. Different data is also added between D, E and F. Likewise, data is existed between G, H and I. The delay amount changes because of concealment using every another data. The basic processing is the same.

4-1-13. PS-183 Board

1. Outline

Heretofore, the Y and chroma data are processed at 1/4 frequency respectively in 8 channels. The PS-183 board parallel/serial converts these data to restore them to the original signals. Then, sync code and ID data are added to the video data for digital output, and it is sent outside the processor via the DIF-1 board. The video data is also output to the ADA-12 board which converts the digital signals into analog output signals. The converted analog signals pass through interpolation filters. Interpolation filters which have different frequency characteristics are used for Y and chroma signals since they have different band width. There is a circuit for correcting delay difference in units of clock caused by the Y and chroma interpolation filters since these filters have different group delay characteristics.
In addition, the digital data of tri-level sync is added in the H blanking and V blanking periods of Y signal.

2. Parallel/Parallel Converter

The 32-bit data (RED 17-10, 27-20, 37-30, and 47-40) are input to this circuit as Y signals. The RED 17-10 is the data of the leftmost quartered parts of the picture screen, i.e., part A. The RED 27 through RED20, RED37 through RED30 and RED47 through RED40 correspond to the data in parts B, C and D respectively.
Input video data is latched and input to the parallel-parallel converter, which converts the data into 4-phase data using the line memory. Though input data are arranged in the order of vertically-quartered parts of the picture screen, they are converted, when they are output, into 4 phases where each line's data are assigned to every fourth sample Nos., i.e., 1, 5, 9, 13, ···, 2, 6, 10, 14, ···, and so forth.

3. Parallel/Serial Converter

Data are converted from TTL into ECL. The parallel/serial converter restores 4-phase data into 1-phase data at the clock rate of 74.25 MHz.

4. Y/C Delay Controller

The Y signal must be delayed against the chroma signal for delay difference generated by the interpolation filter on the ADA-12 board. This PS-183 board compensates the delay in units as clocks.

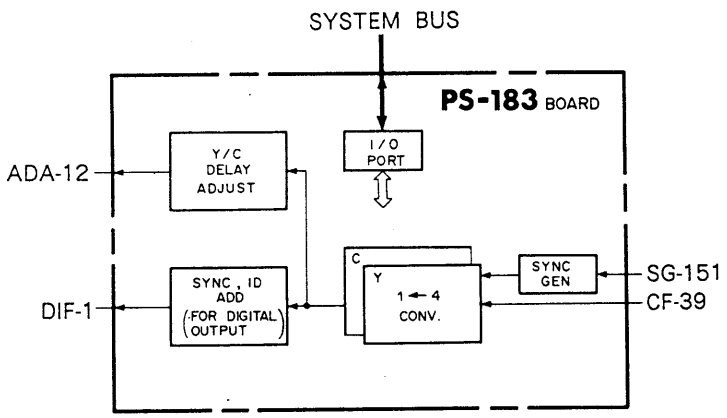


Fig. 4-1-36. PS-183 Board Block Diagram

5. Sync/ID Adder

Data branched before the Y/C delay control circuit is for the digital output. Sync code and ID are added to this data for the digital output interface. The data is output via the buffer to the DIF-1 board.
After the clock rate of the chroma signal is converted into 74.25 MHz, no sync and ID codes are added to the chroma signal. The chroma data is just latched and output via the buffer.

6. Sync Data Generator

The sync data generator generates the tri-level sync signal, and inserts the sync data in the H blanking and V blanking of the Y signals as digital data.
Pedestal level data is added in the blanking periods of the chroma signals.

7. User Data Memory

There is a buffer memory where the user data is written. The user data is located at the start position of the recording active lines : 3H, lines 38 to 40 in the first field, and 2H, lines 601 and 602 in the second field. Only data of lines 38 to 40 and 601 and 602 are written in the buffer memory.

8. Control System

To the RELNP of the connector No. A27D, the line pulse is sent from the CF-39 board. This pulse resets in units of line to activate the H counter.
The FIFO memory block write controller generates the write control signal for the line memory consisting of the FIFO memory used for the parallel-parallel converter, i.e., write enable and reset signals.
The RELNP of the connector Nos. A28A and A28B is the input for ECL level differential line pulse, which allows output timing control. This line pulse and the 18 MHz clock regenerated by the read clock generator are used to drive the H counter. This counter generates the memory read timing signal. It also generates the timing signal for inserting sync into the H blanking and V blanking by the sync add controller.
The ICK18 is V counter. This V counter is reset by the REV signal sent from the SG-151 board.
The TAPE RF2, input to connector No. A28C, is the field ID corresponding to the data read from the frame memory. In the normal playback, the first field and second field are input alternately. In the slow playback, the same field data may be input continuously. In such a case, this TAPE RF2 indicates the field type of input data. If it is set to Low, the first field data is input. If it is High, the second field data is input. The REF ID is the field ID of the reference system. It indicates the first and second fields alternately.
The V timing controller operates based on the V counter signal. The controller generates the V timing control signal for the write address generator of the user data RAM, memory controller, etc.
The PS-183 board reads out the user data, and the data of the lines written the user data is once written in the buffer memory. When the user data period has passed, the data are transferred from the buffer memory to the user's data RAM ICJ23. This operation is controlled by the user data RAM write address generator and user data buffer memory controller.
The data is checked with the user data error check before being transferred from the user data buffer memory. The same data is written twice to compose the user data. Contiguous two data are compared and, if they are the same, they are correct. If they are different, they are erroneous and are not written.
The digital output controller controls the position of adding the sync and ID.
The H counter ICG15 generates the memory read control signal for the parallel-parallel converter. The bit 10 signal of this counter is input to the FIFO memory block read controller, which generates the read enable and reset signals. This controller has independent H counters for writing and reading, so as to change the phase of video signals by shifting the reset timing of the read counter. Rotary switches SW1 and SW2 are used to set the shift of the video signal phase. They are usually set to zero position ; input signal is output as is. The phase can be shifted by changing setting of these switches.
There are system bus input/output ports for controlling the functions of this board from the PR-115 board. The bus is connected to this bus transceiver and address bus buffer. It consists of the address bus and data bus for 256-kbit user data RAM.
User data RAM controller generates the write enable, output enable, and other signals for the user data RAM.

4-1-14. DIF-1 Board

The DIF-1 board is digital interface circuit. D-sub 50-pin connector is used for digital input and output. If the S/N ratio of the input clock deteriorates due to transmitting through long cable, data includes jitters by using the clock as is. The PLL circuit reduces the jitters. The PLL circuits regenerates the clock, based on which data is latched and sent to the SP-06 board.

The DIF-1 board latches data output from the PS-183 board and outputs it from the D-sub 50-pin connector as the digital video output signal. The output clock is adjusted by the delay line so that its leading edge is at the center of data changeover points, then output at timing easy to be latched by the receiver.

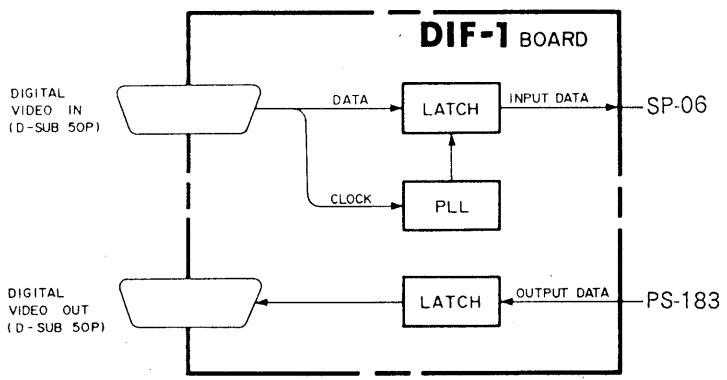


Fig. 4-1-37. DIF-1 Board Block Diagram

4-1-15. VM-08 Board

The VM-18 board works for monitoring the playback RF/CTL waveform and input/output picture. At the output of this board, BNC connectors are provided for the monitor output and waveform output. G, B, R, and sync signals are available at the both of monitor output and waveform output. RF or CTL signal is available only at the wave form output. The selection of waveform output is carried out by the menu of HDD-1000 via PR-115 and SG-115. RF waveform of CTL signal, and input or output video/sync signal are also selected by the menu.
The input/output video and sync signals are supplied from ADA-12 board, and then sent to the monitor output amplifier. There are RV1, RV2 and RV3 which adjust the input signal to 700mV±1%. Then amplified G, B, R, and sync signals are output from each monitor output BNC connector.
The input G, B, R, and sync signals are also supplied to waveform selection circuit. The RF/CTL signal is also sent to here as a WFM±signal from the SIF-4 board with differential line. These signals are switched in this circuit by MONI SEL21 signal sent from the SG-115 board. Then one of them is sent out to waveform output connectors through the waveform output amplifier.

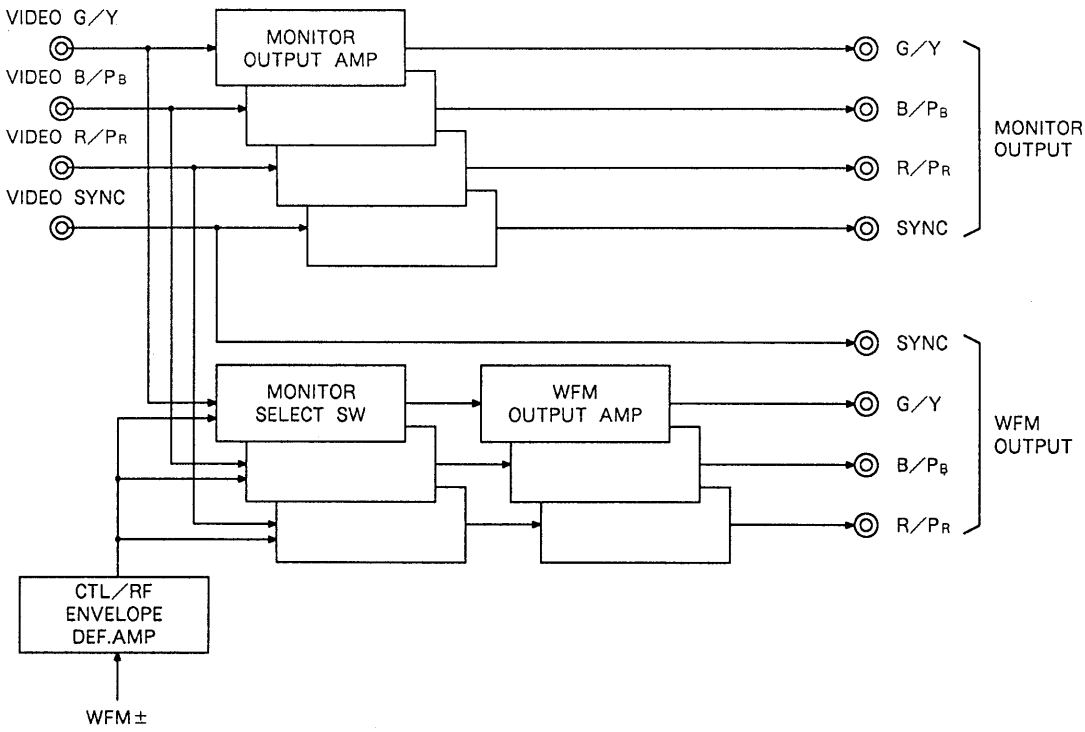


Fig. 4-1-38. VM-08 Board Block Diagram

4-1-16. DP-95 Board

As shown in Fig. 4-1-39, the DP-95 is directly connected to the system bus of the PR-115. The I/O expander in this board activates the LEDs.
Output signals from the I/O expander activate and flashes the INPUT VIDEO, SOURCE VIDEO, ANALOG OUT, VIDEO PRESET, REFERENCE SYNC, INPUT AUDIO , and PROCESSOR SWITCH ENABLE indicators.
These 14 LEDs are all green. 7 pairs of these LEDs represent 7 functions ; a pair of LEDs go on alternately, or go on or out simultaneously, indicating the internal conditions of the processor.
The Alarm indicators consist of the SYSTEM, TEST MODE, ERROR RATE VIDEO, ERROR RATE AUDIO, and AUDIO ASYNCH. Each consists of red and green LEDs. The green LED goes on in the normal state. The red SYSTEM LED goes on in case of system down, failure in communication between the VTR and HDDP-1000, etc.
The red TEST MODE goes on if the switch on the board is set to TEST MODE position or the like.
The red ERROR RATE VIDEO/AUDIO goes on if the video/audio error rate is deteriorated.
The red AUDIO ASYNCH goes on if the audio V is not locked synchronously with the video V.
Lighting of these LEDs depends on the program stored in the PR-115 board.
In terms of the circuit, these LEDs are merely driven by the I/O expanders and buffers.
If the connector CN1 is disconnected, the LED of the PE-18 does not go on since the power is supplied from here. Either of the two LEDs goes on depending on the Low/High level since they are driven by the inverter and buffer. So, only A of the input video control signals is input.

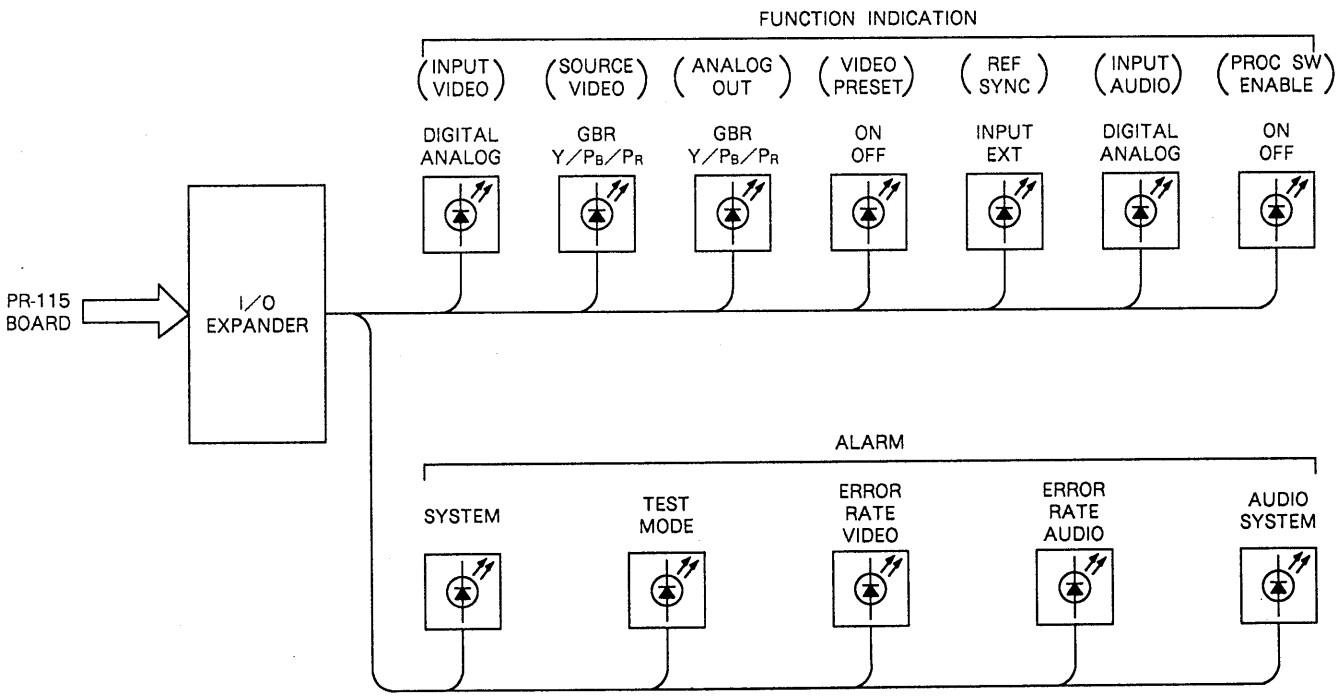


Fig. 4-1-39.

The SOURCE VIDEO signals B and C are input to GBR, Y/P_B/P_R. They indicate the analog video signal conditions. Signals are input independently since both LEDs may not go on due to digital signals. Only one type of signal is input to the inverter and buffer of the ANALOG OUT since its state is either ON or OFF.
This also applies to the VIDEO PRESET.
For Reference signal indicator, F and G are input to indicate independently. These signals are lit by following case,

1. Reference signal is input video
2. Reference signal is EXTERNAL input

These inputs are analog signals. For digital Reference input, both LED are lit.
Only the REFERENCE SYNC indicator flashed when no Sync is selected. It flashes in the case of internal.
The INPUT AUDIO carries only one type of signal, i.e., digital or analog.
The PROCESSOR SWITCH ENABLE also carries only one type signal since its state is ON or OFF only. To set the processor condition with the switch on the processor board without using the menu of the VTR, set the PROCESSOR SWITCH ENABLE switch to ON. The processor condition is usually set using the menu on the VTR.
The ERROR RATE VIDEO does not indicate the normal error rate. 1 frame includes 4000 to 5000 segments. If the number of segments with at least one error exceeds approximately 1000, the red ERROR RATE VIDEO LED goes on.

4-2. AUDIO SIGNAL SYSTEM

4-2-1. Outline

Audio signal system consists of following boards :
- AD-38 Board : A/D conversion
- DA-28 Board : D/A conversion
- DEC-41 Board : Encoder/decoder
- IFA-5 Board : VTR interface
- IO-33 Board : Analog XLR connector
- IO-34 Board : Digital I/O connector (XLR)
- IO-39 Board : Digital I/O connector (D-sub 15-pin)
- PR-115 Board : Processor control

Since 8-channel are processed with HDDP-1000, the following describes the flow of 1-channel signal.
Input signal is fed to the AD-38 board and passes through the input differential amplifier. A level control IC follows the differential amplifier. The VR-74 board in the VTR outputs data about the gain to be adjusted which is read and processed by the PR-115 once, then input to the AD board.
An emphasis amplifier follows the AD board. The AD board performs double over-sampling. Signal passes through the low-pass filter for double over-sampling and then the sampling hold circuit, and are A/D converted. A digital filter changes 96 kHz A/D signal into 48 kHz signal.
Since the signal is serial signal, it is converted into 16-bit parallel signal to be output to the audio parallel bus. Each channel has an A/D converter and a DC feedback circuit converges the signal to zero.
Emphasis ON/OFF is displayed on the LED via the I/O port of the CPU.
Digital data converted into parallel is once read by the PR-115 board. The PR-115 board performs selection of various signals, level control, digital high-pass filtration, error correction of the playback signal, etc.
Signal to be recorded is output from the PR-115 board to the DEC-41 board. The data input to the DEC-41 board is interleaved by the encoder. The Sync word and CRCC are added in front of and behind the 16 bits interleaved data and parity is added in the middle of the data and then they are HDM-1 modulated. The HDM-1 is a modulation method in accordance with the DASH format.
Data passes through the buffer and the IFA-5 board, and is output to the VTR via a 50-pin D-sub connector.

The playback signal from the IFA-5 board and EE signal from the encoder are selected and input to the decoder. Since playedback signal includes jitters, a PLL circuit is provided for extracting the clock. After extracting the clock, an LSI checks HDM-1 demodulation and CRCC and performs sync separation. If there is no Sync output signal, the CRCC error is occurred and the error indicator LED on the front of the board goes on. Demodulated signal is de-interleaved and is error corrected, then returns to the PR-115 board.
If the video tracking control is turned during playback mode, the audio signal is shifted with respect to the reference signal since it is written in the longitudinal direction. The tracking shifted data is fed via the PR-115 board for correcting the recording phase in editing. If the tracking phase is adjusted to the optimum position for the video signal with the tracking control, the playback phase of the audio signal is shifted and thus the phase is kept its sequential form at editing.
The 16-bit parallel data processed by the PR-115 board is input to the DA-28 board and is converted into serial data and then passes through the quadruple over-sampling digital filter, D/A converter and low-pass filter. Since the low-pass filter delays the phase of the high-frequency range, there is a circuit for correcting the delay. Signal passes through the de-emphasis circuit, line amplifier and muting circuit and is output.
The signal from the I/O port of the CPU activates the emphasis indicator LED.
The multiplexer selects each channel's analog output for cue channel recording, mixes 2-channel signals of 8 channels, and outputs them to the VTR via the D-sub 50-pin connector.
The PR-115 board has a clock generator for controlling the bus and reference block addresses. The main CPU on the PR-115 board selects which data of the playback signal, analog input data or digital input data, etc. to output to the DA-28 and DEC-41 boards.
Digital audio input data, i.e., serial data in the AES/EBU format, is converted into parallel data and output to the audio bus. When outputting, parallel data on the audio data bus is read and converted into the AES/EBU format. For the data of which error detection is impossible, error flags are transmitted from the DEC-41 board. In the case of 1-sample error, the average of two samples before and after the error is used to correct the error. In case of continuous errors, a value before the errors is held for correction. For errors which cannot recovered by pre-hold, the CPU makes them to the muting circuit.

4-2-2. IO-33 Board

The IO-33 board consists of a connector and jumper pin only.

4-2-3. AD-38 Board

The AD-38 board performes A/D conversion of 8-channel audio signals. The audio signals input from the canon connector on the IO-33 board is level controlled by the gain control circuit consisting of IC101 and IC102.
The analog multiplier IC103 receives 14-bit data transferred from the system bus and controls its output current in accordance with the setting of the REC volume control on the HDD-1000 control panel. IC104 performs I-V conversion. The deglitcher IC105 reduces glitch caused when the 14-bit data is switched by analog multiplier IC103 and prevent it from being heard as noise.
The filter FL101 is a low-pass filter for double over-sampling (since double over-sampling is performed by A/D conversion). Q101 and Q102 are the emphasis on/off switch. IC107 performs sampling hold at 96 kHz and output is A/D converted by IC108. RV102 is used for noise level control. RV103 is for distortion control.
IC14 is a digital filter restoring ×2 over-sampled 2-channel signals into ×1 sampled signals. IC11 carries out serial/parallel conversion and outputs 8-channel audio signals to the bus.

IC4 is a port receiving data from the system bus and condition of IC4 is controlled by IC3. Every time 16-bit data output to PA0 to 7 and PB0 to 7 (REC volume) are updated, IC2 outputs WR pulse for writing in the multiplier. PC0 to 7 drives the emphasis circuit and the emphasis indicator LEDs.
Sample hold signal of the deglitcher is also output with the data write pulse from IC2 being as a trigger. These audio signals are held within the period determined by the time constant of CR of monostable multivibrator. IC12 is a clock buffer, 384FS is the clock for the digital filter. It is half divided into 192 times by IC6.

IC11 converts 8-channel serial audio data into parallel data and outputs them to the bus.
Balanced signals X and Y are terminated by 600-ohm if the short pin J101 is inserted.
Each of these signals are received by the inverting amplifier in IC101. Each output of IC101 is input to IC102 to be converted from differential into single-phase signal. The level of the output from pin 1 of IC102 is slightly reduced by the reversing amplifier in the same IC102, then controlled by IC103 (analog multiplier), and output from pin 4 of IC13. This output is made after converted to voltage signal by IC104 and sample-held by IC105 (deglitcher).
IC104 is the emphasis amplifier. Emphasis on/off is set with the EMPH switch on the level control panel of the VTR.
The ×2 low-pass filter FL101 follows the emphasis. Its output is amplified by IC106. IC107 is a sampling hold circuit for A/D conversion. Signal sample-held by IC107 is A/D converted by IC108. RV103 (converter balance) is for MSB balance adjustment, i.e., for adjusting the MSB +/− ratio equal to reduce distortion.
IC111 is a variable voltage regulator to vary the +5V to be supplied to IC108 slightly for S/N ratio adjustment.
The following IC109 and IC110 are used to reduce DC components by means of feedback in order to equalize the ratio of MSB ("0" and "1") occurrence.
IC14 is a 2-channel digital filter. 2 channels of A/D converter outputs are input and then output to DOR and DOL. Outputs of ICs 17 and 18 for channels 5 to 8 are a little different and DOL only is output. Since the serial/parallel convertor IC11 has 6 input pins only, each sample of channels 5/6 and 7/8 carries 2-channel data format.

4-2-4. DEC-41 Board

1. Data Flow in Encoder

20-bit data to be recorded is read from the digital audio bus in 8-bit memory. The high-order 16 bits are divided into high-order 8 bits and low-order 8 bits. As for the low-order 4 bits, 2 samples of data, amounting to 8 bits, are processed together. These 8-channel data are once stored in small-capacity RAM, then transfer into the interleave memory.
Data is once read from the interleave memory for parity calculation. After calculating the parities P and Q, the data is re-stored in the interleave memory.
The ICF14 converts the data and parity read at the interleaved timing into serial signal. CRCC output of ICF14 and SYNC word output of ICF12/ICF13 are added before and after this signal. In the time sharing adopted here, 8 channels in 1 sub block repeat.
The modulation generator (ICD11 to ICD13) outputs not modulated waveform but invert signal (Invert=1, Non-invert=0) necessary for modulation. Inversion is performed by ICE8 exclusive-OR gate. Up to this exclusive-OR gate, data is transferred in the condition where inverting point is "1" and non-inverting point is "0". Though only one line of serial data is input to the modulation generator, it outputs two lines of data, data inverted at the edge of the input data bit cell and data inverted at the center of the input data bit cell.
The following shuffling memory consisting of ICD9 and ICD10 converts the form of 8-channel time sharing from sub block unit to bit unit and controls the amount of delay.
The channel switching circuit consisting of ICE9 and ICE10 converts independent inversion data at the edge and center of the bit cell into unified data by switching the inversion points alternately by every 4 channels. Then, the exclusive OR plus shift register consisting of ICE8 and ICE7 converts the inversion data into actual inversion data. The 4-bit shift register of ICE7 time-shares 4 channels. It is used as a memory to 4-channel time-share.

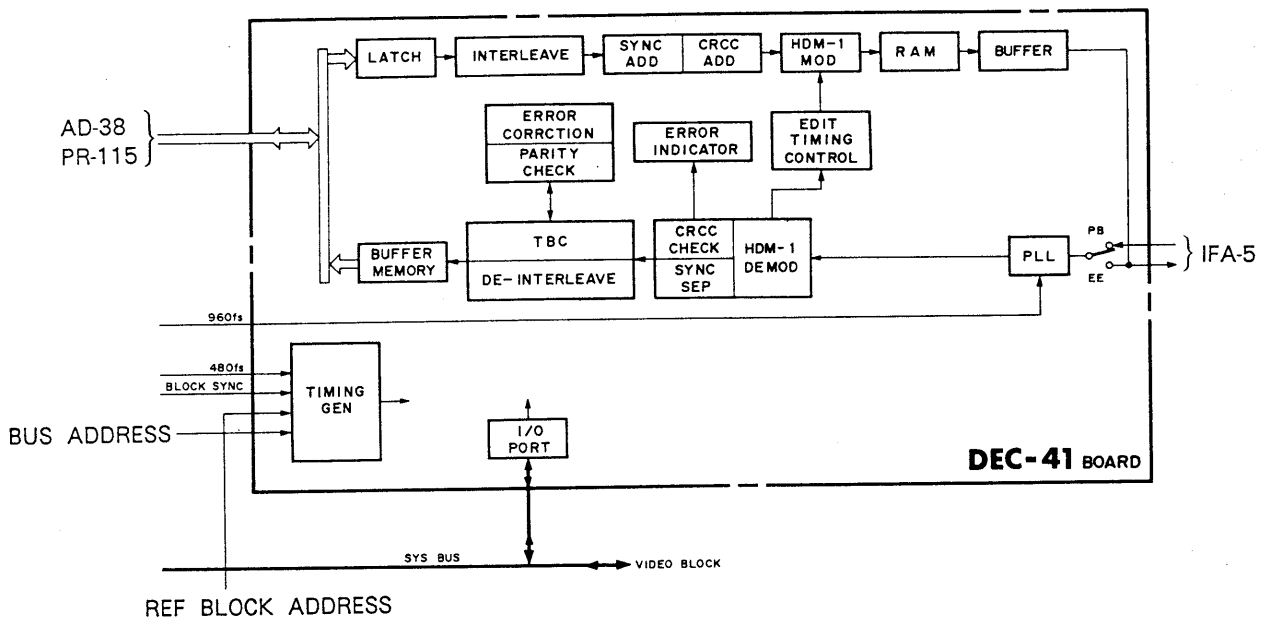


Fig. 4-2-1. DEC-41 Board Block Diagram

2. Encoder Peripheral Circuits

The block address multiplexer consisting of ICA2 and A3 outputs the high-order and low-order bits of the block address alternately since the Sync word can include 4 bits as sync address bit.
The encoder flag bit control circuit consisting of ICA4 and B3 reads flag data from the system bus connected to the PR-115 board and writes it in the RAM ICA4 as necessary, then outputs it at appropriate timing.
The flag supplied by the system bus consists of the emphasis flag and 4 ch/8 ch mode discriminating flag only so far. However, the insert flag indicating the editing point with the encoder is added by ICB2 independently. Addition of the insert flag reduces data aborted at the editing point.
The shuffling address generator generates address used for re-arranging data. Timing pulses needed for various parts are generated at ROM of ICC14, ICC16 and ICC18.

3. Data Flow in Decoder

The clock generator and data latch circuit generates clock synchronous with data from the playback data.
The HDM-1 demodulator circuit demodulates HDM-1 modulated data and outputs 16-bit parallel data. If the CRCC check results in success, pulses are generated every blocks. If these pulses discontinue, a CRCC error occurs; each channel's LED on the front of the board goes on in such a case.
Data output from the LSI passes through the buffer consisting of ICH11 and H12 and is output to the decoder data bus. Output data is de-interleaved by the main RAM of the decoder.
The parity checker circuit corrects errors. Error flags are added to non-corrected errors.
The multi level selector switch 1 can selects the number of samples of continuous errors for muting.
The high-order 16-bit and low-order 4-bit corrected data are stored independently in the decoder output buffer.
They are output to the PR-115 board via the audio data bus at the appropriate timing.

4. Decoder Peripheral Circuit

The block address checker checks whether the block address included in the Sync word accords with the flywheel counter. If not, digital audio data is not written in the memory but is aborted. The decoder flag memory is RAM similar to the memory in the encoder flag bit controller. It stores flags played back by the decoder. Therefore, the PR-115 board is read out via the port connected to the system bus.
Via the system bus I/O ports, the EE/PB, REC enable and other various data are input and output to/from the encoder and decoder. Data indicating the amount of delay of the encoder output varied when editing, is supplied via this system I/O ports.

4-2-5. IFA-5 Board

The D-sub 50-pin connector CN1 is a connector for transferring digital audio signals with the VTR.
IC2 and IC3 are the RS-422 drivers and IC4 and IC5 are the RS-422 receivers. The 25-pin D-sub connector (RS-232C) is for future extension, i.e., for monitoring the conditions of the CPU in the processor from an external personal computer.
IC1 is the RS-232C driver/receiver.
TXB232C indicates data from the CPU to a personal computer. RXB232C indicates data from the personal computer to the CPU.
RTSB indicates the request to send signal from the CPU to the personal computer. CTSB indicates the clear to send signal from the personal computer to the CPU.

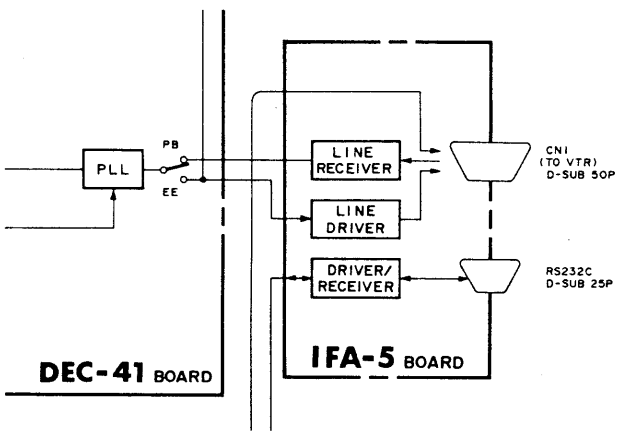


Fig. 4-2-2. IFA-5 Board Block Diagram

4-2-6. DA-28 Board

DA-28 board is the audio D/A converter board. 16-bit data sent from the PR-115 board are converted into serial signals in units of 2 channels by IC1, IC3 and IC5.

Data are sent at 48 kHz sampling rate heretofore. The digital filter IC121 over-samples data at quadruple frequency, increasing the frequency to 192 kHz. The data are output to IC101 of the D/A converter IC130. RV101 absorbs the deviation in the output of the D/A converter. FL101 is the low-pass filter for double over-sampling.

This filter uses the buffer IC101 for high-impedance output. IC102 corrects the delay characteristics of FL101. Since near 20 kHz is delayed comparing to the low-frequency range, the correction circuit delays the los-frequency range only.

The de-emphasis circuit Q101 is controlled via the I/O ports of the system bus of IC9 and IC11. The line amplifier consisting of IC103, IC104 and IC106 converts the signal into differential level, which are output via the muting circuit consisting of Q102 to Q105.

IC102 applies DC feedback to IC101 to remove DC components since signals of IC103, IC104 and IC106 must not includes DC components.

Signals passing through the buffer IC105 are input to the mix channel select switches IC18 and IC19, which can mix any 2 of 8 channels. Then, signals are converted into differential signal by IC12 and IC13, pass through the muting circuit Q3 to Q6, then output. These signals are used by the VTR as the Cue channel input signals.

Channel-1 to channel-8 signals are output from IO-33 board. The monitor and cue signals are output from the IFA-5 board to the VTR via the D-sub 50-pin connector.

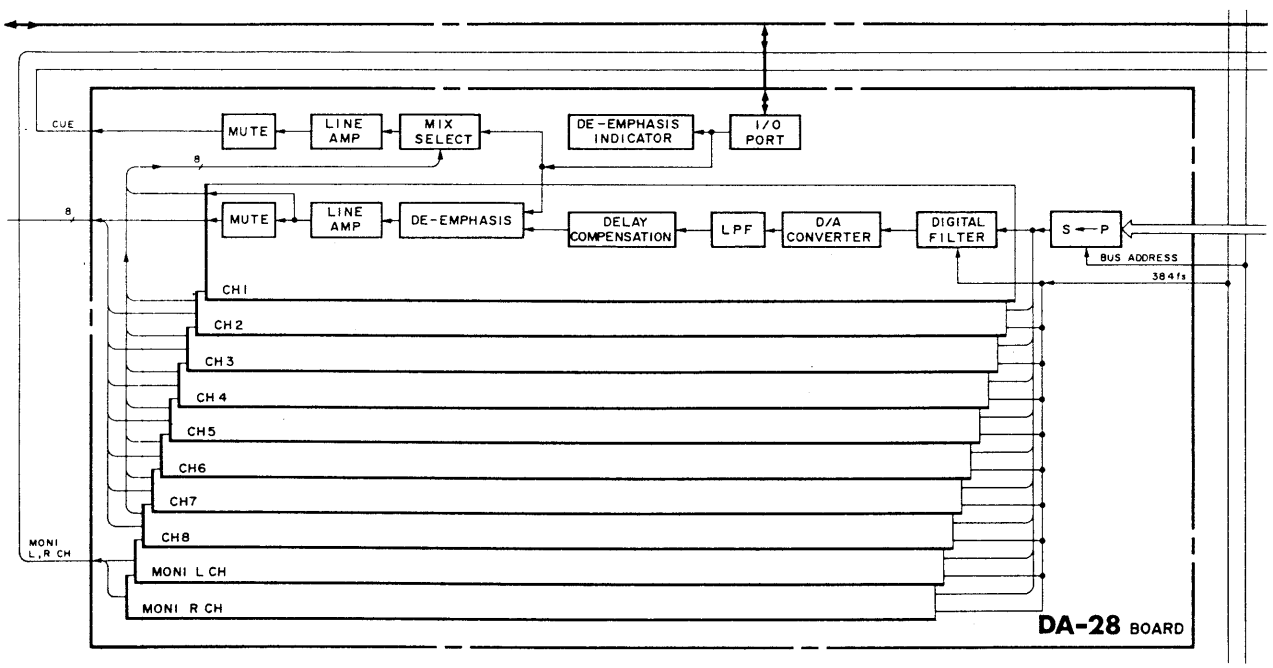


Fig. 4-2-3. DA-28 Board Block Diagram

Data from the digital data 16-bit bus are parallel-serial converted by ICand IC2. SO12 of IC2 outputs channel-1 and 2 serial data. SO34 outputs channel-3 and -4 serial data. SO12 of IC1 outputs channel-5 and channel-6 data. SO34 outputs channel-7 and channel-8 data. SO56 outputs L-channel and R-channel monitor data.

IC9 provides the system I/O ports. PA0 to PA7 are channel-1 to channel-8 de-emphasis bits. When the signal goes Low, de-emphasis turns on and the LED goes on. The signals are converted, by IC7 and IC8, into +5V/−18V "0" and "1", which drive the emphasis ON/OFF transistor.

PB0 and PB1 are the de-emphasis data for L-channel and R-channel monitor signals.

PC0 is the port for power on muting. Releasing of muting is delayed when power is turned on. When power is turned off, Q1 is immediately turned off by a circuit consisting of C34, Q7, R31, etc. since this port cannot offer in-time control.

Each 3-bit PD0 through PD6 are used to determine the channel of 8 channels selected by the mix channel select IC18 and IC19.

Current is added to the select output of these IC18 and IC19 by IC12. The output data is converted into differential signal by IC13, then output via the muting circuit consisting of Q3, Q4, Q5, and Q6.

IC121 is a quadruple digital filter. Data at the quadruple sampling rate, i.e., 192 kHz, through IC121 is input to the D/A converter IC130. Converted analog signal is output from AOL and AOR as current, it is inverted by IC101.

FL101 is a double over-sampling filter with high-impedance output, whose output is received by the following buffer IC101. The time constant of the delay correction circuit IC102 is set so that the preshoot and overshoot become equivalent. R110 and R111 to Q101 is the de-emphasis circuit and when Q101 turned on, de-emphasis is activated. Signal is converted into differential signals by IC103, IC104 and IC106. IC104 and IC106 are connected in parallel to secure current output.

Q102, Q103, Q104 and Q105 are for muting when power is turned on.

Differential output of IC104 and IC106 pass through IC102, which feed back only DC components to IC101. Thus, potential DC difference of the output of IC104 and IC106 is zero.

One of the differential output passes through the buffer IC105, and is input to the cue mix channel select circuit.

Each channel has a three-terminal regulator. IC122 and IC123 are the regulator for channel 1. IC128 and IC129 are that for channel 2.

The gain of the delay correction circuit in the monitor channels (IC952 and IC902) are reduced by 6 dB. Thus, when the level of the audio channels 1 to 8 is 4 dBm, the standard level, that of the monitor channel is 2-dBs lower that it. BCK is ×32FS. LRCK is ×1FS. XIN is ×384FS.

4-2-7. PR-115 Board

1. Outline

The PR-115 board covers the control of the digital audio system, switching of the processor video system, communication with the VTR, and supply of the clock signals to the audio boards. It includes the serial interface for digital audio, audio concealment (error correction), and audio edit functions.

2. Clock Generator

This board has 92.16 MHz and 92.06784 MHz VCXOs to handle two field frequencies, 59.94 and 60 Hz. For synchronization with the video clock, field frequencies AUDH (B27A) and AUDVP (B28A) are transmitted from the video SG board. VCXO is divided into 240-time FS (sampling frequency) and is input to the H Sync PLL for synchronization with AVDH.
The counter block (ICH29, H32, H33) supplies 960-time and 480-time FS to other boards at the ECL level. ICG30, ICG32 and ICG33 supply 384-time FS to D/A and A/D converters at the ECL level. This FS is divided and converted from ECL into TTL level, which is supplied to the host CPU, sub CPU, and digital I/O.
The 5-block Sync generator (ICF32 and ICF33) supplies 5-block Sync signal synchronous with V to the decoder board.
The bus address generator (ICC29, ICC31, ICC33, ICD29 and ICD30) generates addresses of the audio data bus. It divides the 48 kHz sampling area into the digital I/O select area, decoder output area, encoder input area, D/A output area, meter value reading area, and monitor output reading area, and gives 240 addresses to them.
The reference block address generated by the reference block address generator (ICA33, ICB28, ICB32, ICC27, etc.) is synchronous with V. One cycle of digital audio signal processing is complete for 250 blocks (3V). Each is expressed by 8 bits. The programmable timer counter controlled by the CPU interrupts the CPU synchronously with V and generates other clock signals. The clock system also includes the editor address generator. ICA28 to ICH27 generate the edit address.

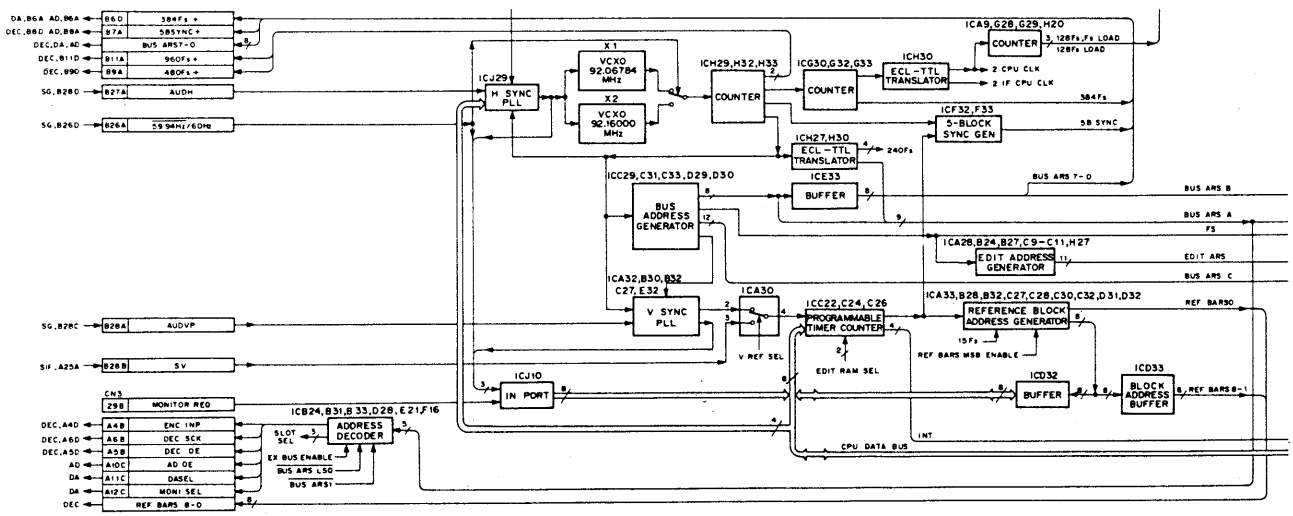


Fig. 4-2-4. Clock Generator

3. CPU Peripheral Circuit

ICA6 is the host CPU. ICA4 is the interrupt controller. It causes interruption synchronous with V ; it causes interruption once and eight times per V.
DECINT (A3B) is the muting interrupt of input terminal.
When the decoder board outputs a muting request, the CPU is interrupted and muting is activated.
ICA8 is the address bus buffer. ICA9 and B9 form the data bus buffer.
ICA2 is the ROM for the host CPU programs. ICA10, A11 and D14 form the address decoder. ICA12 and A13 form the working RAM, the RAM area of the CPU. The ROM capacity is 1 megabit. Two 256-kilobit RAMs are used.

CN3 is a connector for debugging and is connected with a external computer. CPU control signals such as read, write, etc. are output to this connector.
The clock generator receives the double CPU clock, then divides it by half and outputs to the host CPU. This generator controls CPU resetting and wait for the CPU. The clock frequency is 9.216 MHz (at the field frequency of 60 Hz). The CPU reads and writes in 4 cycles. Since this speed may result in failure in reading depending on devices type, reading is performed through waiting in such a case ; for example, 2 waits are given to an area or no wait is given to another area by dividing the memory map into several areas.
Each block has the CPU bus. The address decoder carries out selection such as transmitting CPU commands to each block or accessing data.

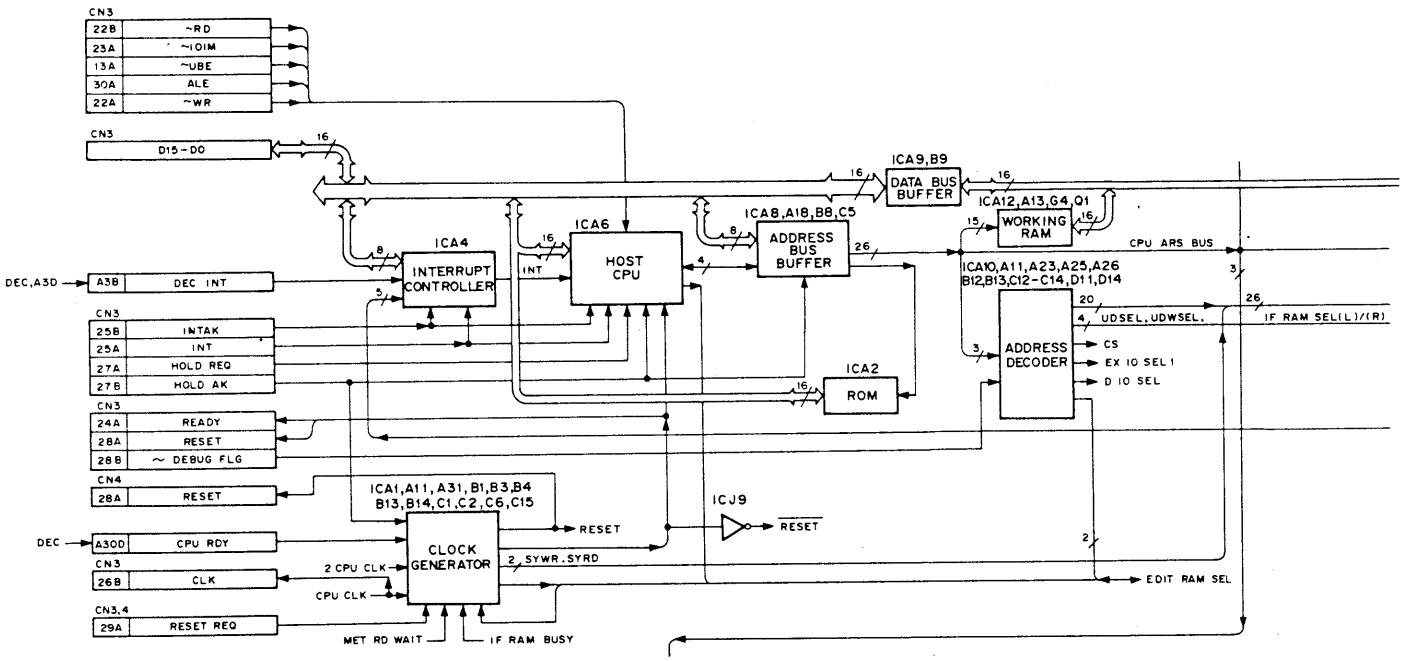


Fig. 4-2-5. CPU and Peripheral Circuits

4. Communication

Sub CPU ICH3 is V25 handling communication with the VTR. Its operation is based on V interruption. It receives the reset and interrupt signals from the host CPU. This host CPU has two communication lines and three 8-bit extension ports.

Every V causes the host CPU to interrupt. When a command is transmitted from the VTR, the sub CPU interrupts the host CPU. The sub CPU transfers data with the host CPU via the interface RAM consisting of ICJ4 and ICJ6.

Input terminal RXA422 of B15B receives data sent by the VTR to the processor. Output terminal TXA422 of B14B outputs data from the processor to the VTR. When the RS-422 data synchronous with V is read by the sub CPU (ICH3), the sub CPU writes the data into the interface RAM. The host CPU reads the data. Then, the host CPU resends a command corresponding to the next V.

This CPU uses the PAL as the address decoder (IGC1) like the host CPU. ICG2 is 256-kilobit ROM. The interface RAM is 8×2-kilobit RAM.

The sub CPU has the switches for the video and audio systems in front of the board. Signals for these switches are input via the expansion port.

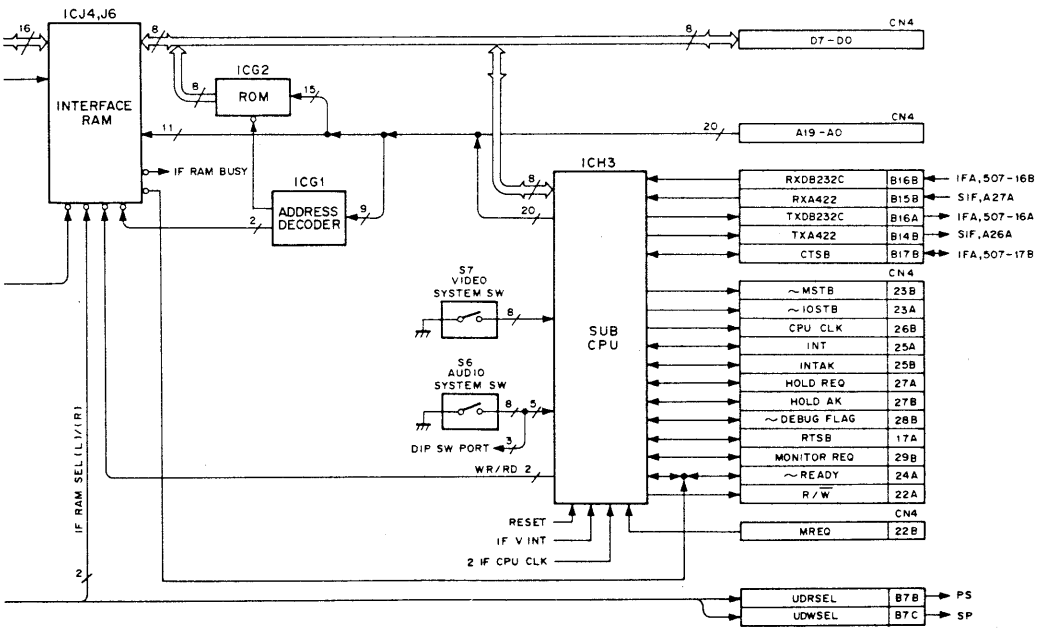


Fig. 4-2-6.

5. Digital I/O

The digital input select (ICJ27) has the diagnostic function which selects its own digital output and inputs it in the digital input to check whether it functions properly.
The digital I/O (ICG22, ICG26) is the AES/EBU interface circuit.
The digital I/O (ICG22, ICG26) converts input serial signals in the AEC/EBU format into parallel signals and outputs them to the audio data bus, and inverts the parallel data into AES/EBU signals. C0 to C11 of the ICG22 and ICG26 are the AES/EBU format channel status bits, which are supplied to the CPU bus for control.
The DIO clock counter (ICB25, ICE26, ICF18, ···) supplies the clock signals necessary for digital I/O. It generates these clock signals from the normal sampling frequency and 32-time FS.
The address decoder (ICH23) decodes the CPU address, outputs digital I/O select signals, and outputs the enable signals for reading and writing the channel status bits.
The I/O expander (ICE22) is controlled by the host CPU. The port is connected to DIGITAL INPUT INDICATOR (D3 to D6) and AUDIO REC INDICATOR (D2).
There are five TP terminals. TP1 outputs status pulses within the period of V interruption. TP2 is for V/8. Others are the status test terminals for other interruptions. It can be known by observing the signals at TP1 and TP2 whether the CPU operates properly.
Serial input signal to the digital I/O is input to the circuit from ICJ27 to ICG27. If digital input is coming in, D3 to D6 go on.

6. Meter Circuit

The meter ROM (ICE27) reads 14 bits of meter audio data and converts it into 8-bit data for meter display. The meter data selector (ICB29) writes the output of ICE27 into RAM ICE29, ICE30 and ICF29. It has In and Out ports and outputs data to ICE32. This data is fed back to the meter data selector. A comparator (ICF30) determines which data to select. A value to be indicated on the meter is read from the CPU once per V. Data peak holding is performed since data with great fluctuation may not be read.

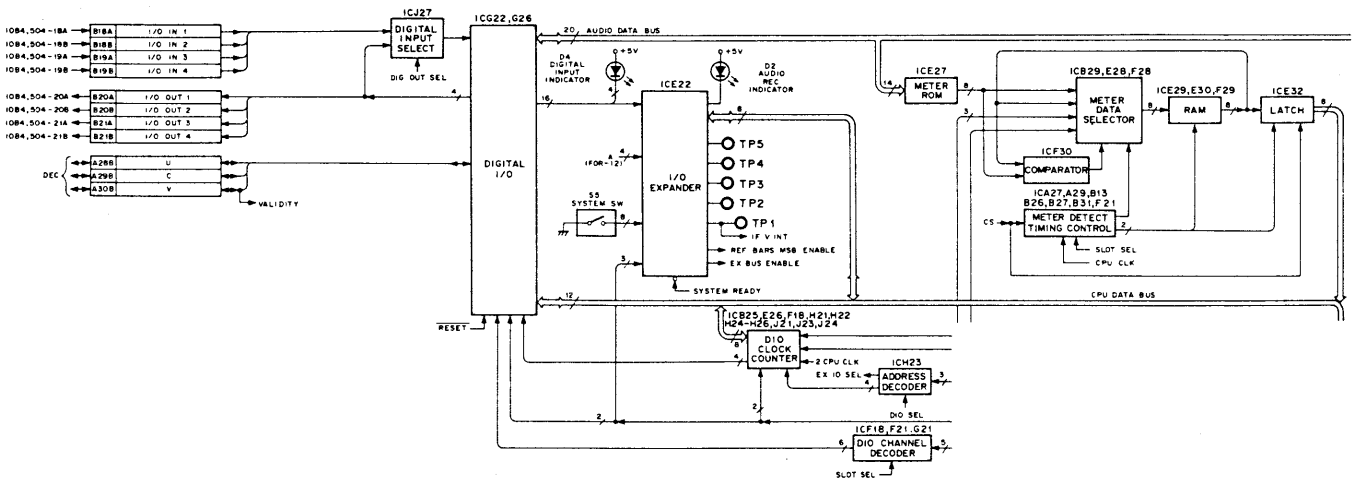


Fig. 4-2-7. Meter Circuit

7. Editing

ICB25, ICE16, ICE18 and ICE19 are bidirectional buffers. It transfers data with other bards via the audio data bus. The data memory (ICF11, F13, F15) is used to write audio data and read out the edited data.

Manual assembler commands are written in the coefficient RAM (ICF10, G10, H11, H13). The CPU can write the commands via the dual port RAM. Certain commands are written in from hardware when an error occurs. In accordance with written commands, signals to the D/A output or encoder input are selected, meter display signals are selected, monitor output signals are selected, recording level is determined according to the VTR REC volume controller, and playback level is determined in accordance with the VTR master playback volume controller.

The fade time latch (ICG16, J16) latches the fade time coefficient and, in accordance with the coefficient, processes input data using the data adder (ICG17, ICG18, ICH17, ICJ17), multiplier accumulate (ICH15), and data memory (ICF11, ICF13, ICF15), then outputs processed data to other boards.

ICF7 is the ROM for manual assembler commands. If the average request is input, one sample is omitted and two samples in front and behind the omitted one are used to reproduce the omitted data.

The two samples used for averaging have their own weights. The closer sample is multiplied by 7/16. The further sample is multiplied by 1/16. These two values are added.

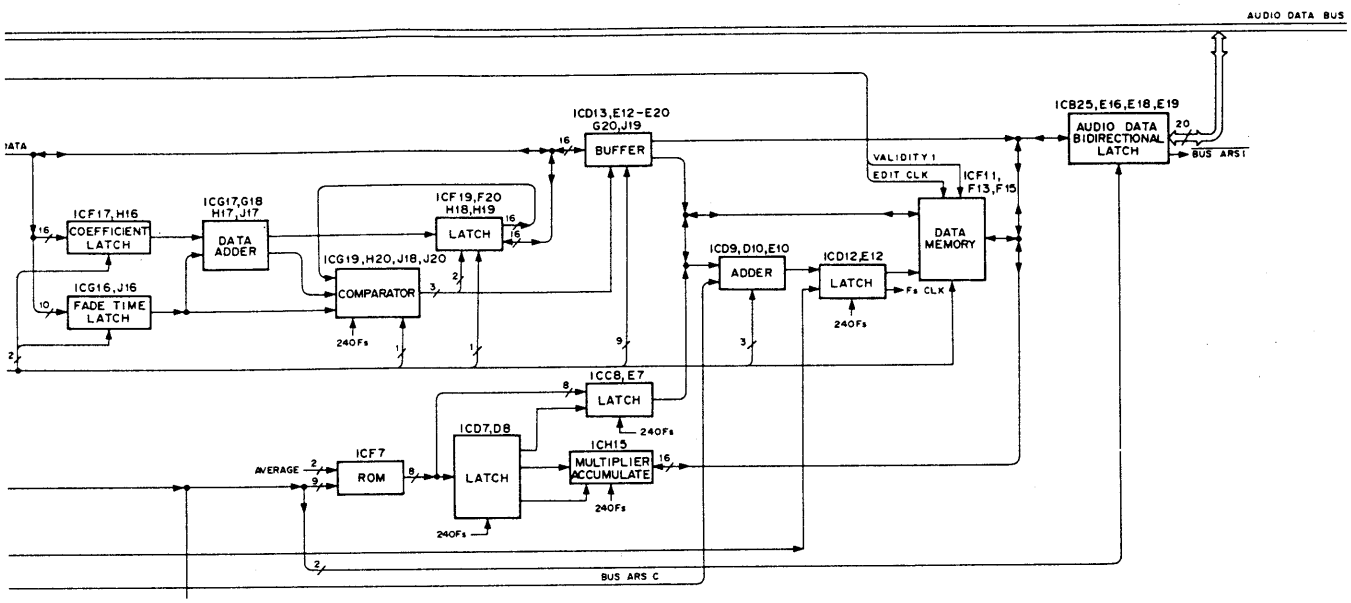


Fig. 4-2-8.

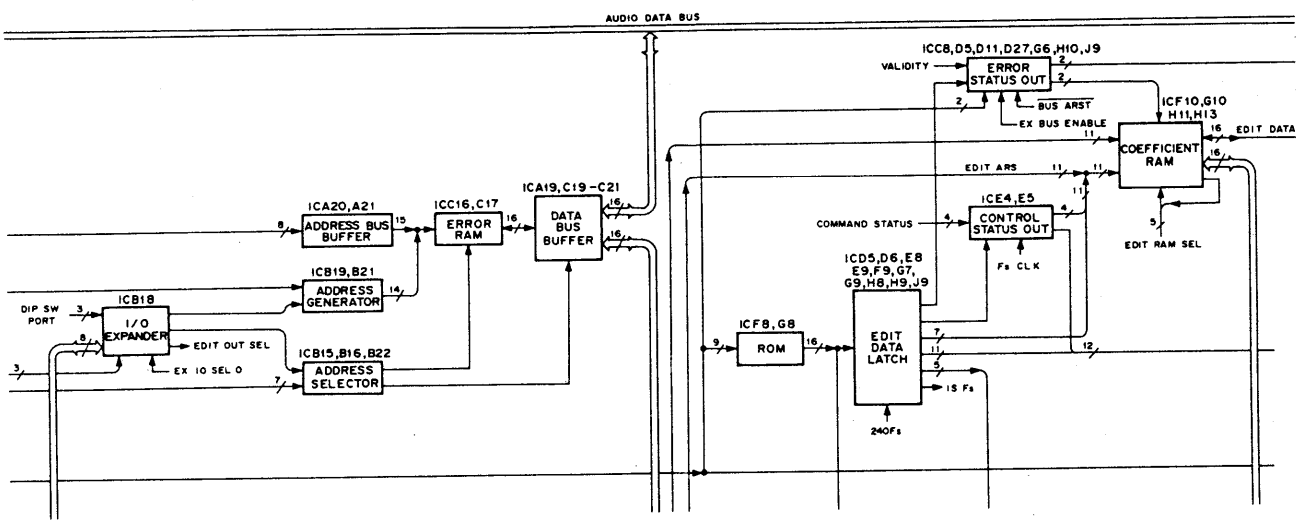


Fig. 4-2-9.

The error RAM (ICC16, ICC17) reads both the audio data and host CPU data. The data bus buffer (ICA19, ICC19 to ICC21) switches audio data and host CPU data in accordance with the control signal from the address selector (ICB15, ICB16, ICB22).

8. Average Channel Detector

The average channel detector (ICF3, ICF4, ICJ9) carries out average detection when an error occurs. 8-channel error data are transmitted in serial from the decoder. ICF4 converts these data into parallel data. The average indicator (ICF1, ICF2) displays the channel of average processing. The converted parallel data are converted again into serial data by ICF3 and output to the hold detector (ICE3, ICE5, ICE6, ICF6, ICJ6).

If more than two samples of error signals are input continuously, the hold indicator (ICE1, ICE2) indicates the channel of hold processing.

These average and hold indicators are connected to the I/O expander of the CPU. The CPU reads the output of the indicators and checks the channel which undergoes the average and hold processing.

The lock indicator (D7) goes on if the internal clock signal is synchronized with the reference signal (AUDH, AUDV).

The mute indicators (D8 to D15) display the muted channels.

DIP switch S2 is for controlling the CPU such as inhibiting host CPU interruption, etc. It is usually fixed.

ROM (ICF8, ICG8) is used for hold processing control.

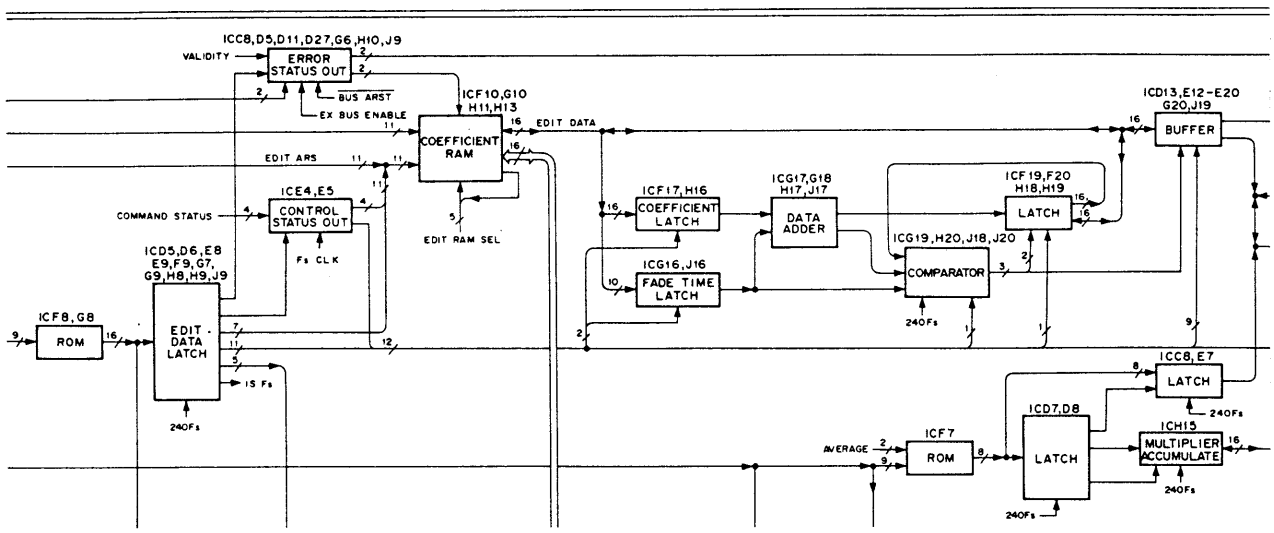


Fig. 4-2-10.

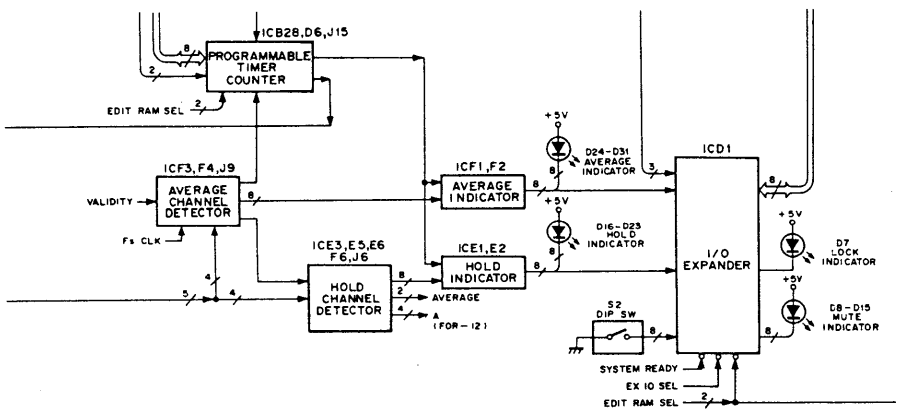


Fig. 4-2-11.

4-2-8. IO-39/IO-34 Boards

The IO-39 board has the driver and receiver circuits for the digital audio signals in the AES/EBU format and inputs and outputs signals via D-sub 15-pin connector.
IC1 is the receiver for the digital audio signals input from outside. IC2 is the driver for the digital audio signals output to outside. Each of them consists of 4 channels, amounting 8 channels.

The IO-34 board has the driver and receiver for the digital audio signals in the AES/EBU format and inputs and outputs data via XLR connectors CN651 to CN658. Each connector handles 2-channel I/O digital audio data. The driver and receiver are the same as used on the IO-39 board. IC1 is the receiver and IC6 is the driver.

If data are input to both the D-sub 15-pin and XLR connectors, IC2, IC3, IC4 and IC5 select the input to the XLR connectors. Four independent selector circuits are provided. If signals are input to the D-sub connector and only channel-1 and -2 signals are input to the XLR connectors, XLR connectors are selected for channels 1 and 2 and the D-sub connector is selected for 3 to 8 channels.

The IFA-5 board, IO-33 board, IO-34 board and IO-39 board output signals to the sub mother board SMB-2 for BOARD sensing. If any board is disconnected, the CPU on the PR-115 board senses the disconnected board thanks to short-circuit on each board. Error message "IO-33" is displayed on the VTR control panel when the IO-33 board is not inserted correctly.

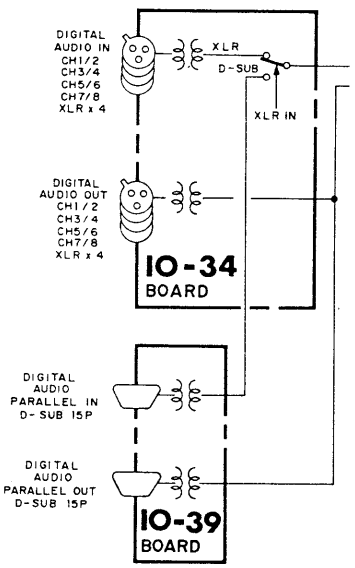


Fig. 4-2-12. IO-39/IO-34 Boards Block Diagram

SECTION 5
GENERAL INFORMATION FOR ALIGNMENT

5-1. INDEX OF ADJUSTMENT COMPONENTS

AD-38 BOARD — **Sec. No.**

ADA-12 BOARD — **Sec. No.**

DA-28 BOARD Sec. No.

SG-151 BOARD Sec. No.

VM-08 BOARD Sec. No.

AC-69 BOARD Sec. No.

SWITCHING REGULATOR Sec. No.

5-2. ADJUSTMENTS AFTER CIRCUIT BOARD REPLACEMENT

When a circuit board has been replaced, proceed with the adjustments described below.

SG-151 BOARD REPLACEMENT

8-1. WRITE ZERO ADJUSTMENT

VIO-10 BOARD REPLACEMENT

8-2. PB SYSTEM MATRIX INPUT LEVEL ADJUSTMENT
↓
8-3. PB SYSTEM VIDEO OUTPUT LEVEL ADJUSTMENT
↓
8-4. PB SYSTEM FREQUENCY RESPONSE ADJUSTMENT
↓
8-5. REC SYSTEM MATRIAL INPUT LEVEL ADJUSTMENT
↓
8-7. REC SYSTEM FREQUENCY RESPONSE ADJUSTMENT
↓
8-12. SYNC LEVEL ADJUSTMENT

VM-08 BOARD REPLACEMENT

8-8. WFM OUTPUT LEVEL ADJUSTMENT (1)
↓
8-9. WFM OUTPUT LEVEL ADJUSTMENT (2)
↓
8-10. PICTURE MONITOR OUTPUT LEVEL ADJUSTMENT
↓
8-11. PICTURE MONITOR FREQUENCY RESPONSE CHECK
↓
8-13. WFM SYNC LEVEL ADJUSTMENT

5-3. EQUIPMENT AND TOOLS

1. **Oscilloscope**
   Model 2465A mode by Tektronix or equivalent

2. **Audio signal generator**
   Model SG5010 mode by Taktronix or equivalent

3. **Audio level meter**
   Model AA5001 mode by Tektronix or equivalent

4. **Digital voltmeter**
   No. of significant digits : 5 or more
   Accuracy : 0.02% ± 1 count

5. **Frequency counter**
   Effective digits : more than 7 digits

6. **HD picture monitor**

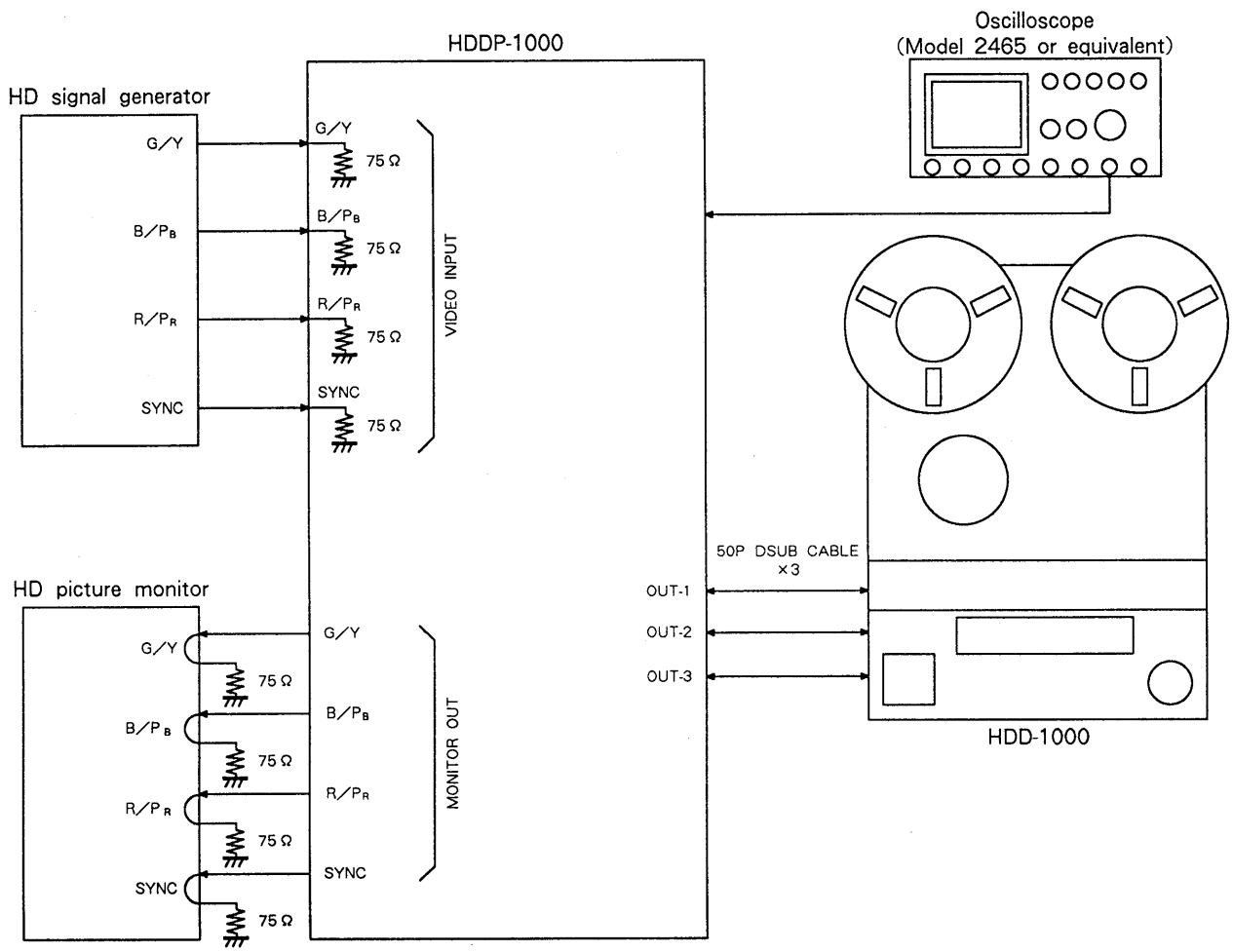
7. **HD digital VTR**
   Sony HDD-1000

8. **HD signal generator**
   Use internal signal generator generated by the other HDDP-1000 or use the HDTV digital test signal generator Model TP21S6 by SHIBASOKU.

9. **EX-186 extension board**
   Sony Part No. A-6001-018-A
   Used for the inspection and adjustment of the principal circuit boads. One extender comes with the HDDP-1000.

10. **IC test clips**
    TC-8 Sony Part No. J-6350-280-A
    TC-16 Sony Part No. J-6041-770-A
    TC-20 Sony Part No. J-6041-780-A
    There are useful for connecting the oscilloscope probe to the leads of the DIP ICs when conducting inspections and adjustments. TC-8 is used for 6-pin or 8-pin DIP ICs, TC-16 for 14-pin and 16-pin DIP ICs, and TC-20 for 18-pin and 20-pin DIP ICs.

5-4. EQUIPMENT CONNECTIONS



5-5. SWITCH SETTINGS

Unless otherwise specified, set the switches to the positions indicated below for adjustment.

AD-38 BOARD

J1 ····· FREE
J2 ····· FREE
J3 ····· FREE
J4 ····· FREE
J5 ····· FREE
J6 ····· FREE
J7 ····· FREE
J8 ····· FREE
J101 ····· SHORT
J102 ····· OPEN
J201 ····· SHORT
J202 ····· OPEN
J301 ····· SHORT
J302 ····· OPEN
J401 ····· SHORT
J402 ····· OPEN
J501 ····· SHORT
J502 ····· OPEN
J601 ····· SHORT
J602 ····· OPEN
J701 ····· SHORT
J702 ····· OPEN
J801 ····· SHORT
J802 ····· OPEN

ADA-12 BOARD

JP1 ····· SHORT
JP2 ····· OPEN
JP3 ····· SHORT
JP4 ····· OPEN
JP5 ····· SHORT
JP6 ····· OPEN
JP7 ····· SHORT
JP8 ····· OPEN
JP9 ····· SHORT
JP10 ····· OPEN
JP11 ····· SHORT
JP12 ····· OPEN
JP13 ····· SHORT
JP14 ····· OPEN
JP15 ····· SHORT
JP16 ····· OPEN
JP17 ····· SHORT
JP18 ····· OPEN
JP19 ····· SHORT
JP20 ····· OPEN
JP21 ····· SHORT
JP22 ····· OPEN
JP23 ····· SHORT
JP24 ····· OPEN
S1-1 Not used.
S1-2 G/Y IN ····· OFF
S1-3 DISP ····· OFF
S1-4 G/Y OUT ····· OFF
S1-5 BLK REQ ····· OFF
S1-6 GRAY REQ ····· OFF
S1-7 INPUT CHARA ····· OFF
S1-8 LOCAL/RMT ····· OFF
S2-1 P_R ····· ON
S2-2 P_B ····· ON
S2-3 Y ····· ON
S2-4 R/P_R ····· ON
S2-5 B/P_B ····· ON
S2-6 G/Y ····· ON
S2-7 Not used.
S2-8 Not used.

CF-39 BOARD

S1-1 CHANNEL DE-INTERLEVE ····· ON
S1-2 Not used.
S1-3 Not used.
S1-4 Not used.
S2 CHANNEL SHIFT ····· 0
S3 FLAG M-SEL ····· 0
S4 ERROR CORRECTION ····· ECC2
S5 CONCEAL. ····· ON
S6 FLAG ····· OFF

CI-05 BOARD

S1-1 Always set to OFF.
S1-2 Always set to OFF.
S1-3 Always set to OFF.
S1-4 NOR/STUNT ····· OFF (NOR)
S1-5 NOR/FAST ····· OFF (NOR)
S1-6 MODE C ····· OFF (FOW)
S1-7 MODE B ····· OFF (REC)
S1-8 MODE A ····· OFF (NOR)
S2-1 NOR/FREEZE A ····· OFF
S2-2 NOR/FREEZE B ····· OFF
S2-3 EE/TAPE ····· OFF (EE)
S2-4 BYPASS A ····· OFF
S2-5 BYPASS B ····· OFF
S2-6 Not used.
S2-7 Not used.
S2-8 NOR/TEST ····· OFF

DEC-41 BOARD

SW1	MUTE SENS ····· 3 OR B
SW2	TEST ····· 0

PR-115 BOARD

S1	Not used.
S2-1	Always set to OFF.
S2-2	Always set to OFF.
S2-3	Always set to OFF.
S2-4	Always set to OFF.
S2-5	CPU SQUEEZE ····· ON
S2-6	Always set to ON.
S2-7	Always set to ON.
S2-8	Always set to ON.
S3	SYSTEM RESET ····· OFF
S4-1	Always set to OFF.
S4-2	Always set to OFF.
S4-3	Always set to OFF.
S4-4	Always set to OFF.
S5-1	Always set to OFF.
S5-2	Always set to OFF.
S5-3	Always set to OFF.
S5-4	Always set to OFF.
S5-5	Always set to OFF.
S5-6	Always sst to OFF.
S5-7	Always set to OFF.
S5-8	Always set to OFF.
S6-1	AUDIO SYSTEM ····· OFF
S6-2	REC INHIBIT ····· OFF
S6-3	Always set to OFF.
S6-4	Always set to OFF.
S6-5	Always set to OFF.
S6-6	Always set to OFF.
S6-7	ANALOG REFERRENCE ····· OFF
S6-8	ANALOG/DIGITAL INPUT SELECT ·· OFF
S7-1	Always set to OFF.
S7-2	Always set to OFF.
S7-3	Always set to OFF.
S7-4	COMMUNICATION DOWN SELECT ···· OFF
S7-5	ANALOG VIDEO INPUT SELECT ····· OFF
S7-6	ANALOG VIDEO OUTPUT SELECT ··· OFF
S7-7	VIDEO SYSTEM BOARD MODE SELECT ····· OFF
S7-8	CI-05 BOARD MODE SETTING ····· OFF

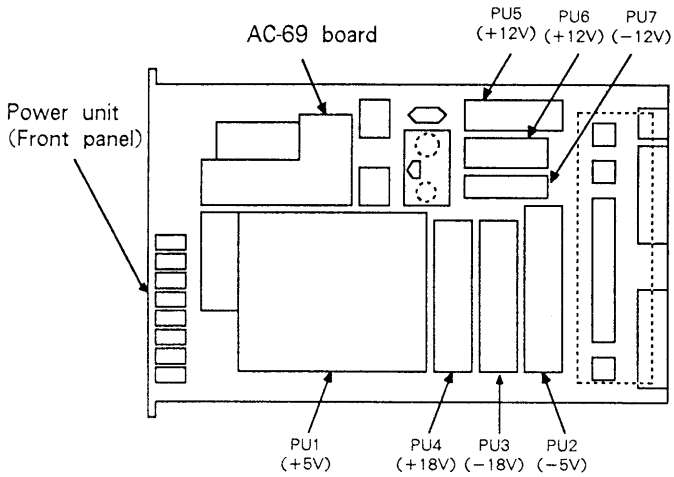
PS-183 BOARD

SW1	VIDEO PHASE ····· 0
SW2	VIDEO PHASE ····· 0
SW3-1	USER DATA DIGITAL OUT ····· OFF
SW3-2	Not used.
SW3-3	Not used.
SW3-4	Not used.
SW4	Y-C DELAY ADJ ·····

SG-151 BOARD

S1	SYNC PHASE ····· 5
S2	Y/C DELAY ····· 3
S3-1	AREF/DREF ····· OFF
S3-2	ACREF/DCREF ····· OFF
S3-3	GEN LOOK/INT ····· OFF
S3-4	INPUT/EXT ····· OFF
S3-5	M SEL0 ····· OFF
S3-6	M SEL1 ····· OFF
S3-7	AIN/DIN ····· OFF
S3-8	NOR/TEST ····· OFF
S4	SYNC PHASE FINE ····· FREE
S5	SYNC PHASE COARESE ····· PRESET
S6	59.96Hz/60Hz ····· 60Hz
S1/SW-334	G/Y INPUT LEVEL ····· FIX
S2/SW-334	B/P_B INPUT LEVEL ····· FIX
S3/SW-334	R/P_R INPUT LEVEL ····· FIX
S4/SW-334	MASTER INPUT LEVEL ····· FIX
S5/SW-334	Y OUTPUT LEVEL ····· FIX
S6/SW-334	P_B OUTPUT LEVEL ····· FIX
S7/SW-334	P_R OUTPUT LEVEL ····· FIX
S8/SW-334	MASTER OUTPUT LEVEL ····· FIX

SECTION 6
POWER SUPPLY ALIGNMENT



Note : Avoid adjusting any of the voltage unless absolutely necessary.

6-1. VOLTAGE ADJUSTMENTS (±5V, ±12V)

Equipment : Digital voltmeter

(1) Extract the ADA-12 board from the HDDP-1000 and insert the extension board EX-186.

(2) Check that the breaker on the front panel of the power supply unit is ON.

(3) Set the power switch on the front door to ON and check that the AC input voltage is within ±10% of the rating.

(4) When ●RV1/AC-69 has been replaced, set ●RV1 to its center position.

(5) **±5V, ±12V adjustments**
Check the following voltages on the extension board EX-186. Use test point for GND terminal as reference voltage.
+5V adjustment
CN2-1a/EX-186 = +5.00±0.25VDC
●PU1 (switching regulator) front panel potentiometer
−5V adjustment
CN2-2a/EX-186 = −5.20±0.25VDC
●PU2 (switching regulator) front panel potentiometer
+12V adjustment
CNA-2a/EX-186 = +12.00±0.24VDC
●PU5 (switching regulator) front panel potentiometer
+12V (FAN) adjustment
CN748/MB-225 = +12.00±0.48VDC
●PU6 (switching regulator) front panel potentionmeter
−12V adjustment
CNA-3a/EX-186 = +12.00±0.24VDC
●PU7 (switching regulator) front panel potentiometer

6-2. VOLTAGE ADJUSTMENTS (±18V)

Equipment : Digital voltmeter

(1) Extract the SG-151 board (slot #12) from the HDDP-1000 and insert the extension board EX-186.

(2) Check that the breaker on the front panel of the power supply unit is ON.

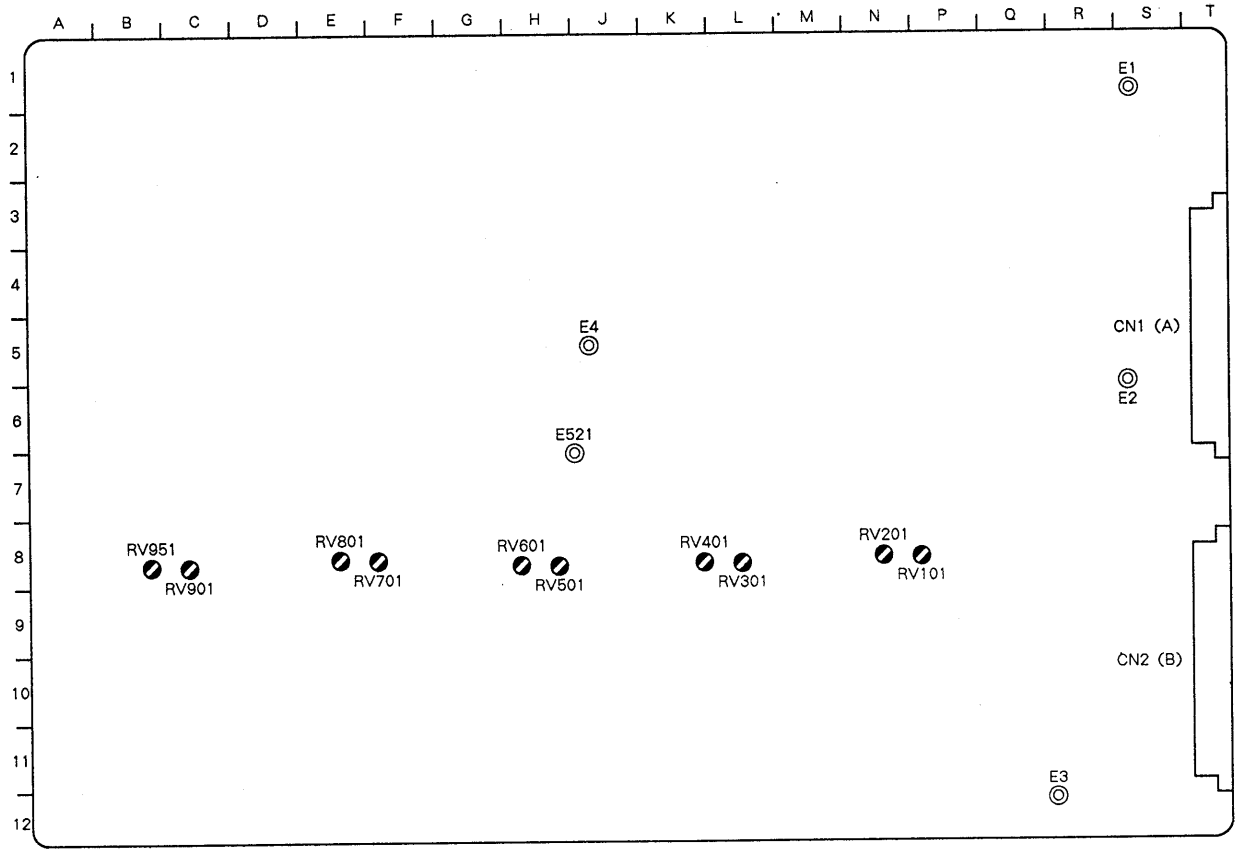
(3) Set the power switch on the front door to ON and check that the AC input voltage is within ±10% of the rating.

(4) When ●RV1/AC-69 has been replaced, set ●RV1 to its center position.

(5) **±18V adjustments**
Check the following voltages on the extension board EX-186. Use test point for GND terminal as reference voltage.
+18V adjustment
CN2-29d/EX-186 = +18.00±0.36VDC
●PU4 (switching regulator) front panel potentiometer
−18V adjustment
CN2-29a/EX-186 = −18.00±0.36VDC
●PU3 (switching regulator) front panel potentiometer

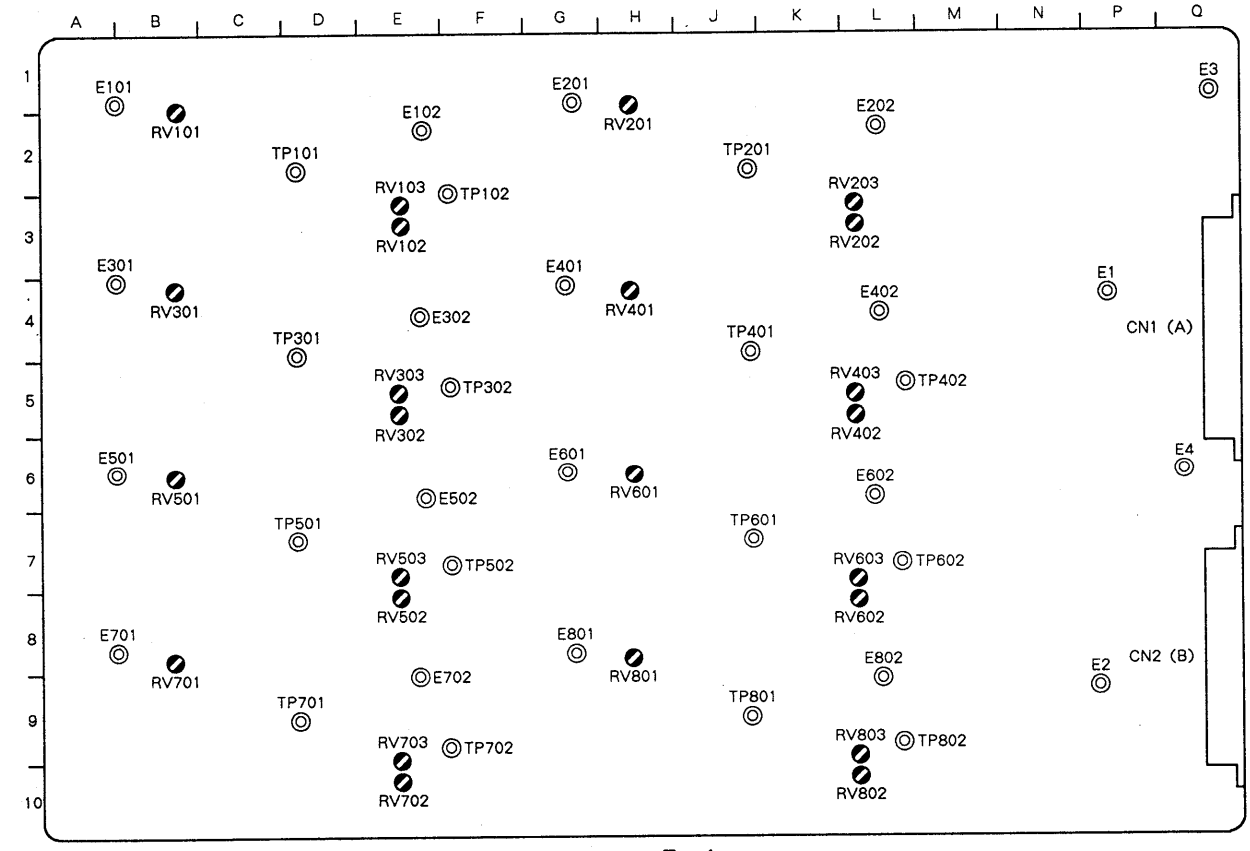
SECTION 7
ANALOG AUDIO SYSTEM ALIGNMENT

DA-28 Board (Component Side)



RV101	P8
RV201	N8
RV301	L8
RV401	L8
RV501	H8
RV601	H8
RV701	E8
RV801	E8
RV901	C8
RV951	B8

AD-38 Board (Component Side)



RV101	B2
RV102	E3
RV103	E3
RV201	H2
RV202	L3
RV203	L3
RV301	B4
RV302	E5
RV303	E5
RV401	H4
RV402	L5
RV403	L5
RV501	B6
RV502	E7
RV503	E7
RV601	H6
RV602	L7
RV603	L7
RV701	B8
RV702	E10
RV703	E10
RV801	H8
RV802	L10
RV803	L10

7-1. AUDIO OUTPUT LEVEL ADJUSTMENT

Equipment ; Audio level meter
Connection ; See Section 5-4
Menu/Switch Settings ; See Section 5-5 and text

Step 1. Menu Setting
Select the menu "T22. AUDIO TEST SG : 1 kHz" of the HDD-1000.

Step 2. Adjustment
Adjust the output level of each channel for +4 dBm ±0.1 dB.

AUDIO CHANNEL	ADJUSTMENT (DA-28 BOARD)
CH-1	⊘RV101 (P8)
CH-2	⊘RV201 (N8)
CH-3	⊘RV301 (L8)
CH-4	⊘RV401 (L8)
CH-5	⊘RV501 (H8)
CH-6	⊘RV601 (H8)
CH-7	⊘RV701 (E8)
CH-8	⊘RV801 (E8)

Step 3.
After adjustment, select the following menu from the HDD-1000.
T22. AUDIO TSET SG : OFF

7-2. MONITOR OUTPUT LEVEL ADJUSTMENT

Equipment ; Audio level meter
Connection ; See Section 5-4
Menu/Switch Settings ; See Section 5-5 and text

Step 1. Menu Setting
Select the menu "T22. AUDIO TEST SG : 1 kHz" of the HDD-1000.

Step 2.
Select both L-CH and R-CH MONITOR SELECT of the VTR to CH-1 and turn the MONITOR PHONES control to fully clockwise (MAX.).

Step 3. Adjustment
Adjustment the output level of both L-CH and R-CH for +4 dBm±0.1 dB

MONITOR CHANNEL	ADJUSTMENT (DA-28 BOARD)
L-CH	⊘RV901 (C8)
R-CH	⊘RV951 (B8)

Step 4.
After adjustment, select the following menu from the HDD-1000.
T22. AUDIO TEST SG : OFF

7-3. AUDIO INPUT LEVEL ADJUSTMENT

Equipment ; Audio signal generator
Audio level meter
Connection ; See Section 5-4
Menu/Switch Settings ; See Section 5-5 and text
Input Signal ; 1 kHz/+4 dBm

Step 1.
Input 1 kHz/+4 dBm signal to each channel.

Step 2. Adjustment
Adjust the output level of each channel for +4 dBm ±0.1 dB

AUDIO CHANNEL	ADJUSTMENT (AD-38 BOARD)
CH-1	⊘RV101 (B2)
CH-2	⊘RV201 (H2)
CH-3	⊘RV301 (B4)
CH-4	⊘RV401 (H4)
CH-5	⊘RV501 (B6)
CH-6	⊘RV601 (H6)
CH-7	⊘RV701 (B8)
CH-8	⊘RV801 (H8)

7-4. DISTORTION ADJUSTMENT

Equipment ; Audio signal generator
Audio level meter
Connection ; See Section 5-4
Menu/Switch Settings ; See Section 5-5 and text
Input Signal ; 1 kHz/+4 dBm

Step 1.
Input 1 kHz/+4 dBm signal to each channel.

Step 2. Adjustment
Adjust the distortion of each channel's output signal for minimum (0.05% or less).

Spec. : Distortion=0.05% or less

AUDIO CHANNEL	ADJUSTMENT (AD-38 BOARD)
CH-1	⊘RV103 (E3)
CH-2	⊘RV203 (L3)
CH-3	⊘RV303 (E5)
CH-4	⊘RV403 (L5)
CH-5	⊘RV503 (E7)
CH-6	⊘RV603 (L7)
CH-7	⊘RV703 (E10)
CH-8	⊘RV803 (L10)

7-5. SIGNAL-TO-NOISE RATIO ADJUSTMENT

Equipment : Audio level meter
Connection : See Section 5-4
Menu/Switch Settings : See Section 5-5 and text
Input Signal : No. signal

Step 1. Adjustment
Adjust the output level of each channel for minimum (−66 dBm or less).

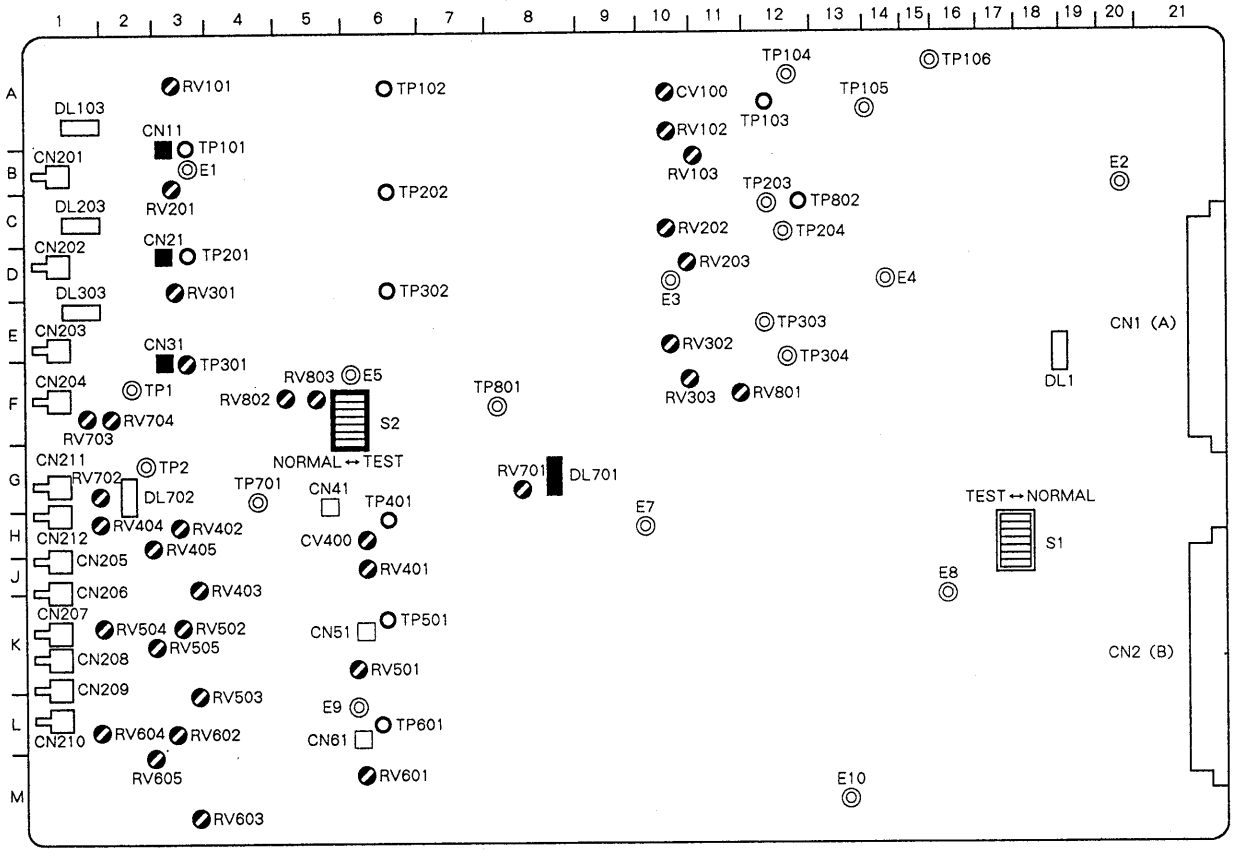
Spec. : S/N = −66 dBm or less

AUDIO CHANNEL	ADJUSTMENT (AD-38 BOARD)
CH-1	⊘RV102 (E3)
CH-2	⊘RV202 (L3)
CH-3	⊘RV302 (E5)
CH-4	⊘RV402 (L5)
CH-5	⊘RV502 (E7)
CH-6	⊘RV602 (L7)
CH-7	⊘RV702 (E10)
CH-8	⊘RV802 (L10)

SECTION 8
ANALOG VIDEO SYSTEM ALIGNMENT

Serial No : Up to 10199

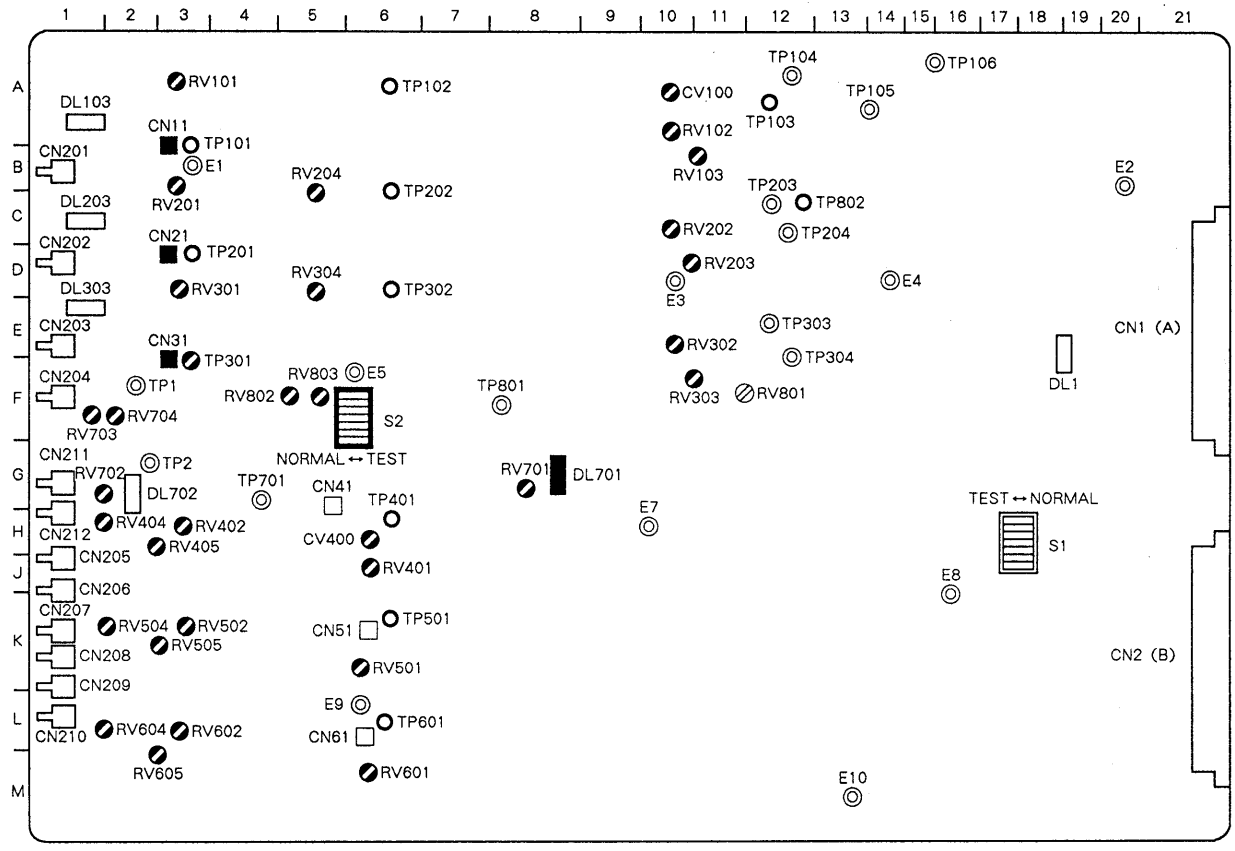
ADA-12 Board (Component Side)



CN11	B3	RV101	A3	RV401	J6	RV505	K2	RV704	F2	TP103	A12
CN21	D3	RV102	A10	RV402	H3	RV601	M6	RV801	F11	TP201	D3
CN31	F3	RV103	B11	RV403	K3	RV602	L3	RV802	F5	TP202	B6
		RV201	B3	RV404	H1	RV603	M3	RV803	F5	TP301	E3
CV100	A10	RV202	C10	RV405	H2	RV604	L1			TP302	D6
CV400	H6	RV203	D11	RV501	K6	RV605	M2	S2	F6	TP401	H6
		RV301	D3	RV502	K3	RV701	H8			TP501	K6
DL701	H8	RV302	E10	RV503	L4	RV702	H1	TP101	A3	TP601	L6
		RV303	F11	RV504	K1	RV703	F1	TP102	A6	TP802	C12

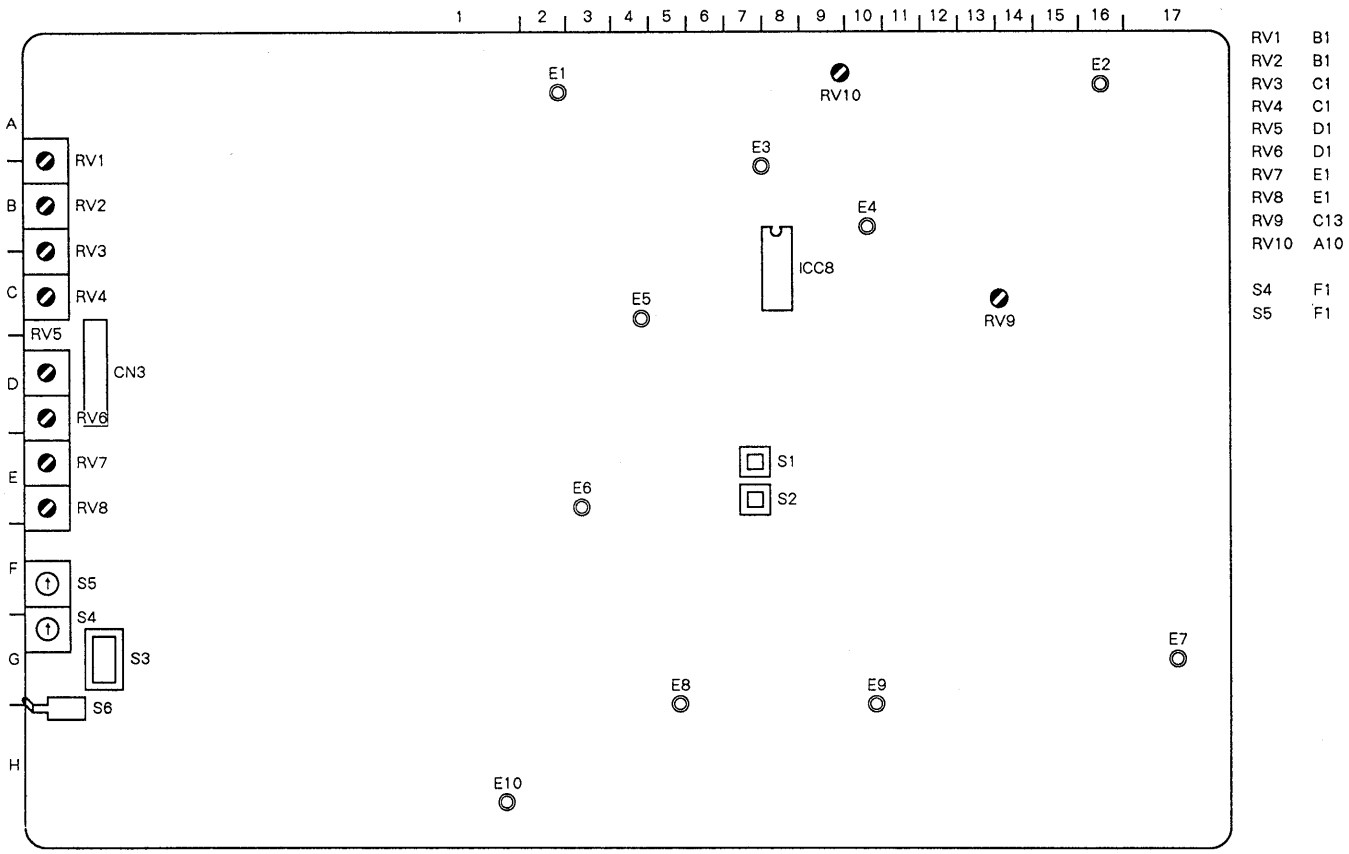
Serial No : 10201 and higher

ADA-12 Board (Component Side)

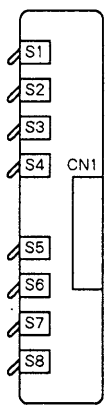


CN11	B3	RV101	A3	RV303	F11	RV505	K2	RV801	F11	TP201	D3
CN21	D3	RV102	A10	RV304	D5	RV601	M6	RV802	F5	TP202	B6
CN31	F3	RV103	B11	RV401	J6	RV602	L3	RV803	F5	TP301	E3
		RV201	B3	RV402	H3	RV604	L1			TP302	D6
CV100	A10	RV202	C10	RV404	H1	RV605	M2	S2	F6	TP401	H6
CV400	H6	RV203	D11	RV405	H2	RV701	H8			TP501	K6
		RV204	B5	RV501	K6	RV702	H1	TP101	A3	TP601	L6
DL701	H8	RV301	D3	RV502	K3	RV703	F1	TP102	A6	TP802	C12
		RV302	E10	RV504	K1	RV704	F2	TP103	A12		

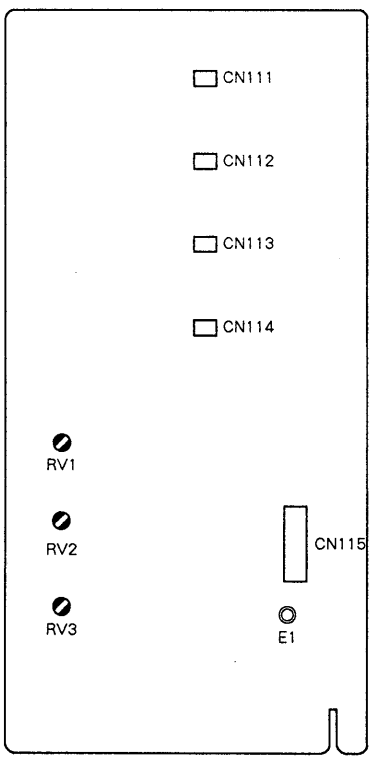
SG-151 Board (Component Side)



SW-334 Board (Component Side)



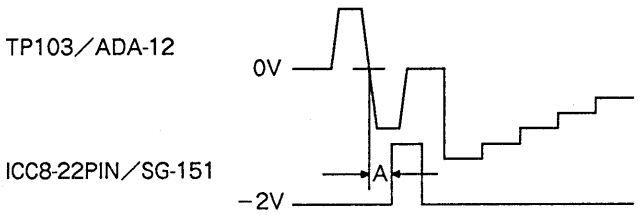
VM-08 Board (Component Side)



8-1. WRITE ZERO ADJUSTMENT

Equipment ; Oscilloscope
Connection ; See Section 5-4
Menu Setting ; See text.
Switch Setting ; OUTPUT LEVEL CONT. ···FIX
Input Signal ; Color bar (Y, PB, PR, or G, B, R)

Step 1. Adjustment



A=3±2 nsec
◐RV10/SG-151/A10

Step 2. Confirmation
Select the menu of the HDD-1000 to "S12. EXTREF" and check to see that the phase fluctuation is 5 nsec or less.

Step 3.
After adjustment, select the menu of the HDD-1000 to "S12. INPUT".

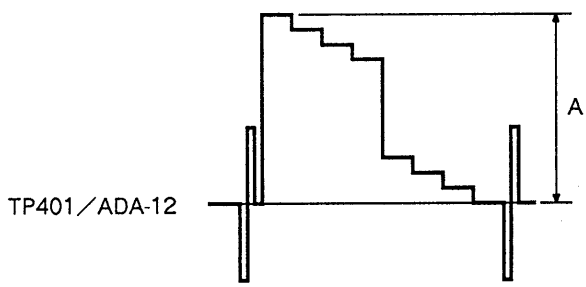
8-2. PB SYSTEM MATRIX INPUT LEVEL ADJUSTMENT

Equipment ; Oscilloscope
Connection ; See Section 5-4
Mode of HDD-1000 ; EE
Menu Setting ; See text.
Switch Setting ; OUTPUT LEVEL CONT. ···FIX
Input Signal ; Color bar (Y, PB, PR)

Step 1.
Select the menu of the HDD-1000 to "T20. CB" and "I83. Y, PB, PR".

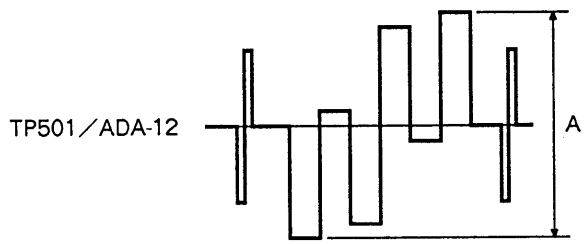
Step 2. Y/C Delay Confirmation
Observe the VIDEO OUT-1 (G/Y, B/PB, R/PR) connector and confirm the Y/C delay between Y, PB, PR and Y−PB, Y−PR, PB−PR.
Spec ; 0±3 nsec

Step 3. Y Matrix Input Level Adjustment



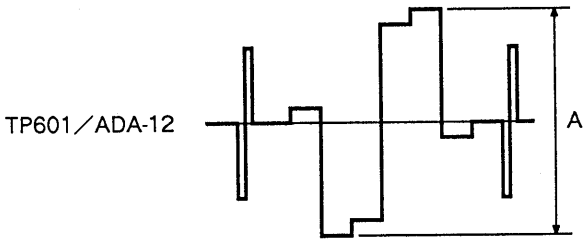
A=1.00±0.01V
◐RV401/ADA-12/J6

Step 4. PB Matrix Input Level Adjustment



A=1.00±0.01 Vp-p
◐RV501/ADA-12/K6

Step 5. P_R Matrix Input Level Adjustment



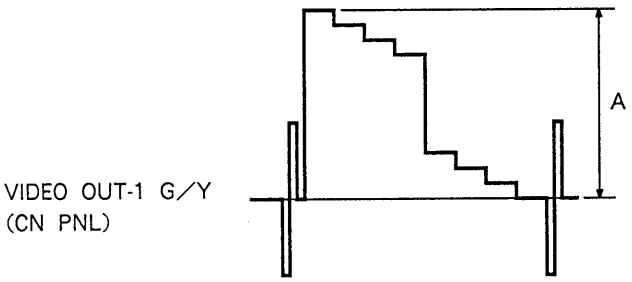
A=1.00±0.01 Vp-p
● RV601/ADA-12/M6

8-3. PB SYSTEM VIDEO OUTPUT LEVEL ADJUSTMENT

Equipment ; Oscilloscope
Connection ; See Section 5-4
Mode of HDD-1000 ; EE
Menu Setting ; See text.
Switch Setting ; OUTPUT LEVEL CONT. ···FIX
Input Signal ; Color bar (Y, P_B, P_R)

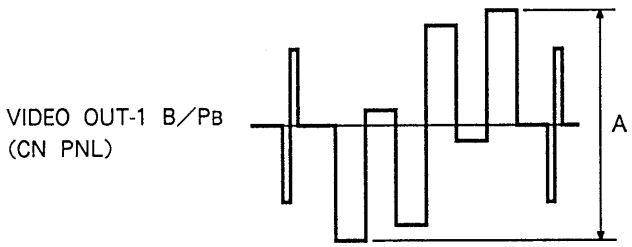
Step 1.
Select the menu of the HDD-1000 to "T20. CB" and "I83. Y, P_B, P_R".

Step 2. Y Level Adjustment



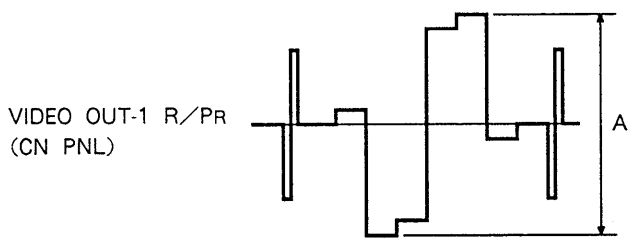
A=700±4 mV (terminating with 75Ω)
● RV402/ADA-12/H3

Step 3. P_B Level Adjustment



A=700±4 mVp-p
(terminating with 75Ω)
● RV502/ADA-12/K3

Step 4. P_R Level Adjustment



A=700±4 mVp-p
(terminating with 75Ω)
● RV602/ADA-12/L3

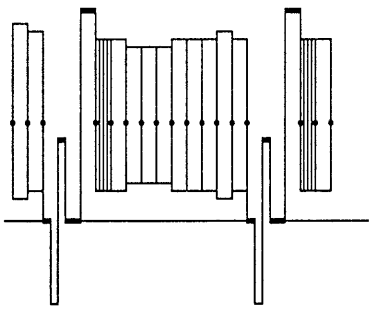
8-4. PB SYSTEM FREQUENCY RESPONSE ADJUSTMENT

Equipment ; Oscilloscope
Connection ; See Section 5-4
Mode of HDD-1000 ; EE
Menu Setting ; See text.
Switch Setting ; OUTPUT LEVEL CONT. ···FIX
Input Signal ; Multiburst (Y, P_B, P_R)

Step 1.
Select the menu of the HDD-1000 to "I83. Y, P_B, P_R" and "T20. MB"

Step 2.
Adjust the frequency response of the output signal from CN41 on the ADA-12 board.

CN41
(ADA-12 board)



3 to 27 MHz : 0±3%
(terminating with 75 Ω)
● CV400/ADA-12/H6

Step 3.
Select the menu of the HDD-1000 to "I83. R, G, B".

Step 4.
Adjust G/B/R outputs of VIDEO OUT−1 connectors (G/Y, B/P_B, R/P_R) with CV401, CV501 and CV601, respectively. Observe VIDEO OUT−2 connectors (G/Y, B/P_B, R/P_R) and confirm frequency response of G/B/R outputs.
Spec. ; 0 to 27 MHz : 0±5% (terminating with 75 Ω)
30 MHz : 0±$^{5}_{10}$% (terminating with 75 Ω)

Step 5.
Select the menu of the HDD−1000 to "T20. OFF", "I81. R, G, B" and "I83. R, G, B".

Step 6.
Adjust G/B/R outputs of WFM OUT connectors (G/Y, B/P_B, R/P_R) with CV402, CV502 and CV602, respectively. Observe MONITOR OUT connectors (G/Y, B/P_B, R/P_R) and confirm frequency response of G/B/R outputs.
Spec. ; 0 to 27 MHz : 0±5% (terminating with 75 Ω)
30 MHz : 0±5% (terminating with 75 Ω)

8-5. REC SYSTEM MATRIX INPUT LEVEL ADJUSTMENT

Equipment ; Oscilloscope
Connection ; See Section 5-4
Mode of HDD-1000 ; EE
Menu Setting ; See text.
Switch Setting ; INPUT/OUTPUT LEVEL CONT. ···FIX
Input Signal ; Color bar (G, B, R)

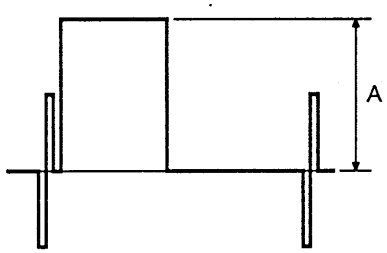
Step 1.
Set external HD signal generator to color bar (G, B, R).

Step 2.
Select the menu of the HDD-1000 to "T20. OFF" and "I81. G, B, R".

Step 3. Y/C Delay Confirmation
Observe the VIDEO OUT-1 connectors (G/Y, B/P_B, R/P_R) and confirm the Y/C delay between Y, P_B, P_R and Y−P_B, Y−P_R, P_B−P_R.
Spec. ; 0±3 nsec

Step 4. Y Matrix Input Level Adjustment

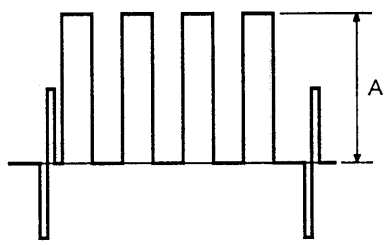
TP101/ADA-12



A=1.000±0.005V
● RV101/ADA-12/A3

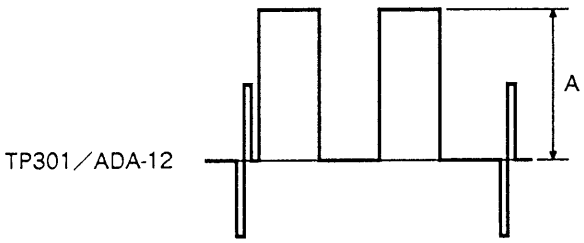
Step 5. P_B Matrix Input Level Adjustment

TP201/ADA-12



A=1.000±0.005V
● RV201/ADA-12/B3

Step 6. P_R Matrix Input Level Adjustment



A=1.000±0.005V
● RV301/ADA-12/D3

Step 7. Matrix Error Confirmation

(1) Set external HD signal generator to multiburst (G, B, R).
(2) Observe TP202 and TP302 on the ADA-12 board and check the matrix errors. (between 100% white level and pedestal level)
Spec. ; 0±4 mVp-p
(3) If not, readjust RV101, RV201 and RV301 on the ADA-12 board.

8-6. REC SYSTEM VIDEO OUTPUT LEVEL ADJUSTMENT

Equipment : Oscilloscope
Connection : See Section 5-4
Menu Setting : See text.
Switch Setting : INPUT/OUTPUT LEVEL CONT. ···FIX
Input Signal : Color bar (G, B, R)

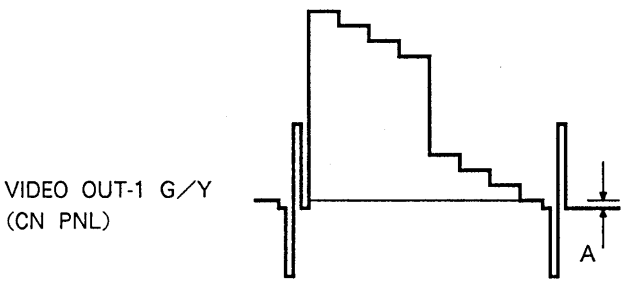
Step 1.
Select the menu of the HDD-1000 to "I83. Y, P_B, P_R".

Step 2.
Set external HD signal generator to color bar (G, B, R).

Step 3.
Terminate the VIDEO OUT-1 connectors (G/Y, B/P_B, R/P_R) with 75 Ω terminator.

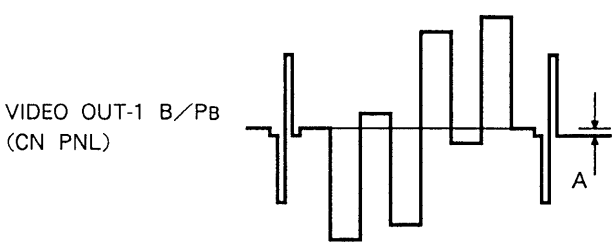
Step 4. Pedestal Clamp Level Adjustment
Observe the VIDEO OUT-1 connectors (G/Y, B/P_B, R/P_R) and adjust the pedestal clamp level of Y, P_B and P_R outputs as follows.

(1) G/Y Pedestal Clamp Level Adjustment



A=0±3 mV
● RV103/ADA-12/B11

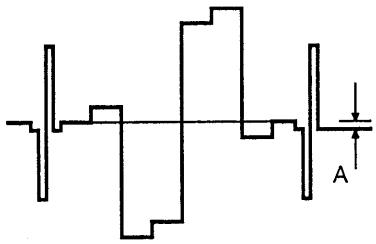
(2) B/P_B Pedestal Clamp Level Adjustment



A=0±3 mV
● RV203/ADA-12/D11

(3) R/P_R Pedestal Clamp Level Adjustment

VIDEO OUT-1 R/P_R
(CN PNL)



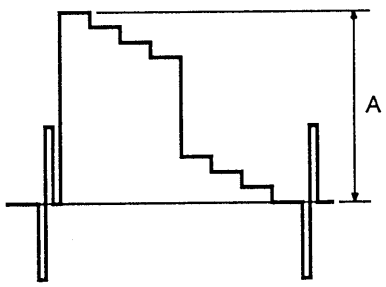
A=0±3 mV
●RV303/ADA-12/F11

Step 5. A/D Reference Voltage Adjustment
Adjust the voltage at TP802/ADA-12 with ●RV801/ADA-12/F11.
Spec. ; −2V±10 mV

Step 6. Video Output Level Adjustment
Select the menu of the HDD-1000 to "T20. CB" and "T20. OFF" alternately, and adjust so that both output equal level.

(1) G/Y Output Level Adjustment

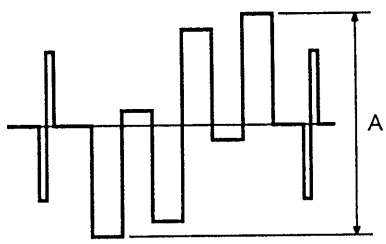
VIDEO OUT-1 G/Y
(CN PNL)



A=700±4 mV
(Deviation should be within ±3 mV.)
●RV102/ADA-12/A10

(2) B/P_B Output Level Adjustment

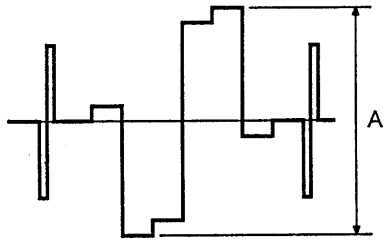
VIDEO OUT-1 B/P_B
(CN PNL)



A=700±4 mVp-p
(Deviation should be within ±3 mV.)
●RV202/ADA-12/C10

(3) R/P_R Output Level Adjustment

VIDEO OUT-1 R/P_R
(CN PNL)



A=700±4 mVp-p
(Deviation should be within ±3 mV.)
●RV302/ADA-12/E10

Step 7.
Select the menu of the HDD-1000 to "T20. OFF".

8-7. REC SYSTEM FREQUENCY RESPONSE ADJUSTMENT

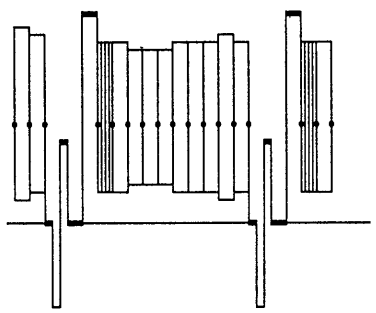
Equipment ; Oscilloscope
Connection ; See Section 5-4
Mode of HDD-1000 ; EE
Menu Setting ; See text.
Switch Setting ; INPUT/OUTPUT LEVEL CONT. ···FIX
Input Signal ; Multiburst (Y, P_B, P_R)

Step 1.
Set external HD signal generator to multiburst (Y, P_B, P_R).

Step 2.
Select the menu of the HDD-1000 to "I81. Y, P_B, P_R".

Step 3. Adjustment
Observe the VIDEO OUT-1 G/Y connector on the connector panel and adjust the frequency response of the output signal.

VIDEO OUT-1 G/Y
(CN PNL)



3 to 27 MHz : 0±5%
(terminating with 75 Ω)
● CV100/ADA-12/A10

Step 4.
Select the menu of the HDD-1000 to "I81. R, G, B" and "I83. R, G, B".

Step 5.
Observe the VIDEO OUT-1 connectors (G/Y, B/P_B, R/P_R) and VIDEO OUT-2 connectors (G/Y, B/P_B, R/P_R), and confirm frequency response of both G/B/R outputs.
Spec. ; 0 to 27 MHz : 0±5% (terminating with 75 Ω)
30 MHz : $0\pm^{5}_{10}$% (terminating with 75 Ω)

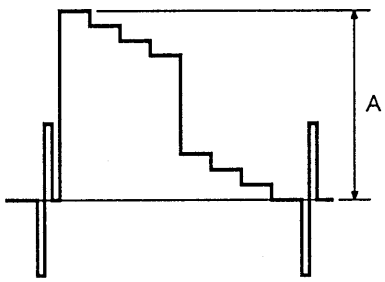
8-8. WFM OUTPUT LEVEL ADJUSTMENT (1)

Equipment ; Oscilloscope
Connection ; See Section 5-4
Mode of HDD-1000 ; EE
Menu Setting ; See text.
Switch Setting ; OUTPUT LEVEL CONT. ···FIX
Input Signal ; Color bar (Y, P_B, P_R)

Step 1.
Select the menu of the HDD-1000 to "T20. CB" and "S03. SELECT".

Step 2. Y Output Level Adjustment

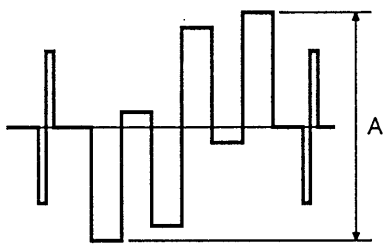
WFM OUT G/Y
(CN PNL)



A=700±4 mV (terminating with 75 Ω)
● RV404/ADA-12/H1

Step 3. P_B Output Level Adjustment

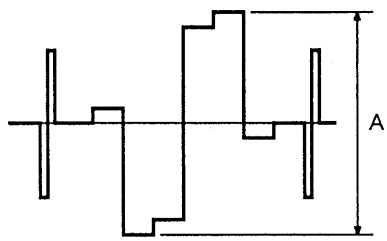
WFM OUT B/P_B
(CN PNL)



A=700±4 mVp-p (terminating with 75 Ω)
● RV504/ADA-12/K1

Step 4. P_R Output Level Adjustment

WFM OUT R/P_R
(CN PNL)



A=700±4 mVp-p (terminating with 75 Ω)
● RV604/ADA-12/L1

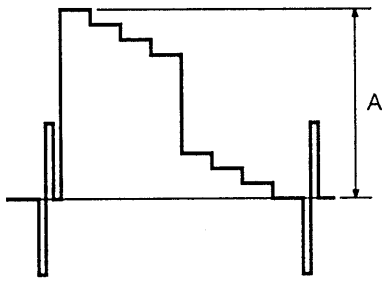
8-9. WFM OUTPUT LEVEL ADJUSTMENT (2)

Equipment ; Oscilloscope
Connection ; See Section 5-4
Mode of HDD-1000 ; EE
Menu Setting ; See text.
Switch Setting ; INPUT/OUTPUT LEVEL CONT. ···FIX
Input Signal ; Color bar (G, B, R)

Step 1.
Set external HD signal generator to color bar (G, B, R).

Step 2.
Select the menu of the HDD-1000 to "T20. OFF" and "S02. INPUT".

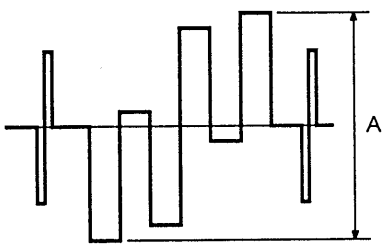
Step 3. Y Output Level Adjustment



WFM OUT G/Y
(CN PNL)

A=700±4 mV (terminating with 75 Ω)
● RV405/ADA-12/H2

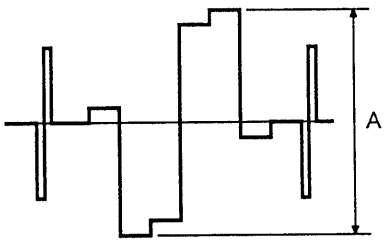
Step 4. P_B Output Level Adjustment



WFM OUT B/P_B
(CN PNL)

A=700±4 mVp-p (terminating with 75 Ω)
● RV505/ADA-12/K2

Step 5. P_R Output Level Adjustment



WFM OUT R/P_R
(CN PNL)

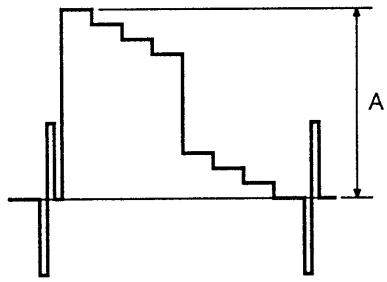
A=700±4 mVp-p (terminating with 75 Ω)
● RV605/ADA-12/M2

8-10. PICTURE MONITOR OUTPUT LEVEL ADJUSTMENT

Equipment ; Oscilloscope
Connection ; See Section 5-4
Mode of HDD-1000 ; EE
Menu Setting ; See text.
Switch Setting ; OUTPUT LEVEL CONT. ···FIX
Input Signal ; Color bar (Y, P_B, P_R)

Step 1.
Select the menu of the HDD-1000 to "T02. CB" and "S02. PROC".

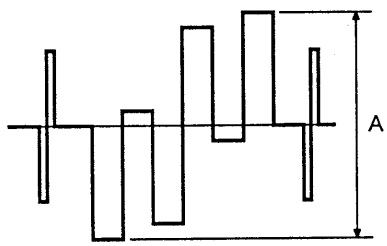
Step 2. Y Output Level Adjustment



MONITOR OUT G/Y
(CN PNL)

A=700±4 mV
(terminating with 75 Ω)
● RV1/VM-08/D1

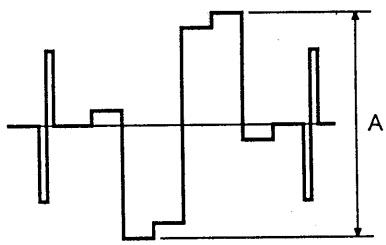
Step 3. P_B Output Level Adjustment



MONITOR OUT B/P_B
(CN PNL)

A=700±4 mVp-p
(terminating with 75 Ω)
● RV2/VM-08/C1

Step 4. P_R Output Level Adjustment



MONITOR OUT R/P_R
(CN PNL)

A=700±4 mVp-p
(terminating with 75 Ω)
● RV3/VM-08/B1

8-11. PICTURE MONITOR FREQUENCY RESPONSE CHECK

Equipment ; Oscilloscope
Connection ; See Section 5-4
Mode of HDD-1000 ; EE
Menu Setting ; See text.
Switch Setting ; INPUT/OUTPUT LEVEL CONT. ···FIX
Input Signal ; Multiburst (G, B, R)

Step 1.
Set external HD signal generator to multiburst (G, B, R).

Step 2.
Select the menu of the HDD-1000 to "T20. OFF" and "I81. G, B, R".

Step 3.
Observe the WFM OUT connectors (G/Y, B/P_B, R/P_R) and MONITOR OUT connectors (G/Y, B/P_B, R/P_R), and confirm frequency response of both G/B/R outputs.
Spec. ; 0 to 27 MHz : 0±5% (terminating with 75 Ω)
30 MHz : 0$\pm^{5}_{10}$% (terminating with 75 Ω)

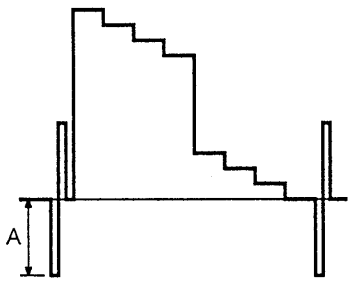
8-12. SYNC LEVEL ADJUSTMENT

Equipment ; Oscilloscope
Connection ; See Section 5-4
Mode of HDD-1000 ; EE
Menu Setting ; See text.
Switch Setting ; INPUT/OUTPUT LEVEL CONT. ···FIX
Input Signal ; Color bar (Y, P_B, P_R)

Step 1.
Select the menu of the HDD-1000 to "I81. Y, P_B, P_R" and "I83. Y, P_B, P_R".

Step 2. Y SYNC Level Adjustment

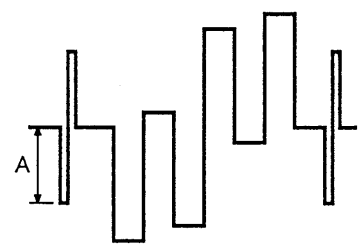
VIDEO OUT-1 G/Y
(CN PNL)



A=300±3 mV
(terminating with 75 Ω)
● RV701/ADA-12/H8

Step 3. P_B SYNC Level Check

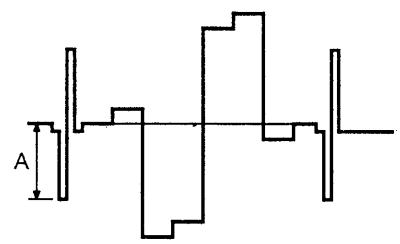
VIDEO OUT-1 B/P_B
(CN PNL)



A=300±6 mV
(terminating with 75 Ω)

Step 4. P_R SYNC Level Check

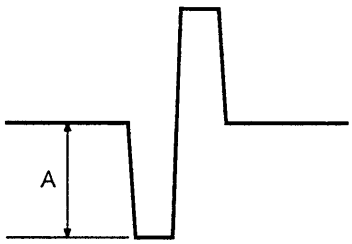
VIDEO OUT-1 R/P_R
(CN PNL)



A=300±6 mV
(terminating with 75 Ω)

Step 5. SYNC Level Adjustment

VIDEO OUT-1 SYNC
(CN PNL)



A=300±6 mV
(terminating with 75 Ω)
● RV702/ADA-12/H1

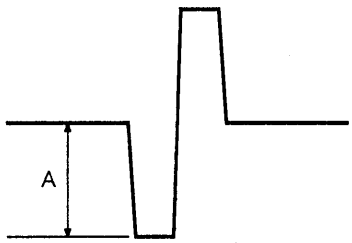
8-13. WFM SYNC LEVEL ADJUSTMENT

Equipment ; Oscilloscope
Connection ; See Section 5-4
Mode of HDD-1000 ; EE
Menu Setting ; See text.
Switch Setting ; INPUT/OUTPUT LEVEL CONT. ···FIX
Input Signal ; Color bar (Y, P_B, P_R)

Step 1.
Select the menu of the HDD-1000 to "S02. INPUT".

Step 2. SYNC Level Adjustment

WFM OUT SYNC
(CN PNL)

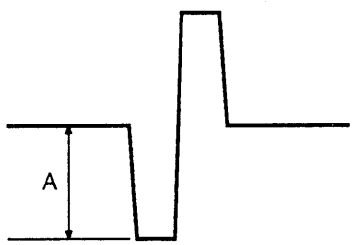


A=300±3 mV (terminating with 75 Ω)
● RV704/ADA-12/F2

Step 3.
Select the menu of the HDD-1000 to "S02. PROC".

Step 4. SYNC Level Adjustment

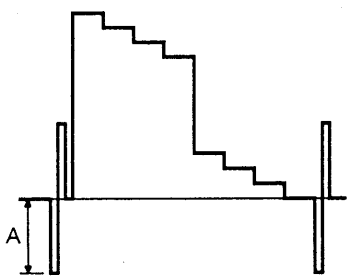
WFM OUT SYNC
(CN PNL)



A=300±3 mV (terminating with 75 Ω)
● RV703/ADA-12/F1

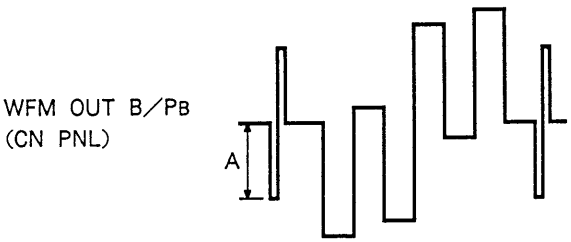
Step 5. G/Y SYNC Level Check

WFM OUT G/Y
(CN PNL)



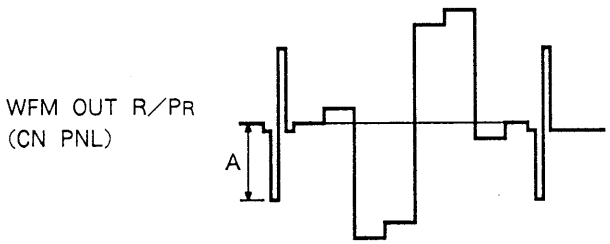
A=300±6 mV (terminating with 75 Ω)

Step 6. B/PB SYNC Level Check



A=300±6 mV (terminating with 75 Ω)

Step 7. R/PR SYNC Level Check

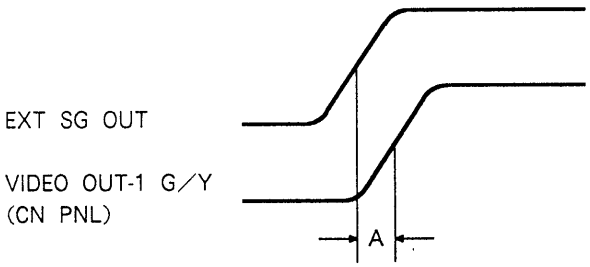


A=300±6 mV (terminating with 75 Ω)

8-14. SYNC OUTPUT PHASE ADJUSTMENT

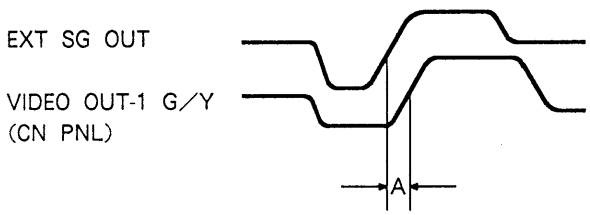
Equipment : Oscilloscope
Connection : See Section 5-4
Mode of HDD-1000 : EE
Menu Setting : See text.
Switch Setting : INPUT/OUTPUT LEVEL CONT. ···FIX
Input Signal : Pulse & bar (Y, PB, PR)

Step 1. Adjustment
Observe the Y signal that is output from the external HD signal generator and the Y signal that is output from the VIDEO OUT-1 G/Y connector. Adjust phase difference at 2T pulse portions of both outputs for minimum (6.7 nsec or less).



A=6.7 nsec or less
(terminating with 75 Ω)
● S4/SG-151/F1
● S5/SG-151/F1

Step 2.
Adjust the sync phase of above signals.



A=2 nsec or less
(terminating with 75 Ω)
● DL701/ADA-12/H8

Step 3. Check
Check the phase difference between VIDEO OUT-1 Y output and PB/PR/SYNC outputs.
Spec. ; 0±2 nsec

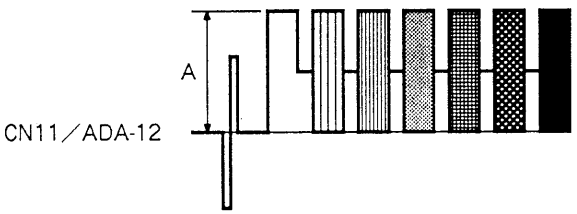
8-15. INPUT LEVEL CONTROL CHECK (1)

Equipment ; Oscilloscope
Connection ; See Section 5-4
Mode of HDD-1000 ; EE
Menu Setting ; See text.
Switch Setting ; INPUT/OUTPUT LEVEL CONT. ···FIX.
Input Signal ; Multiburst (G, B, R)

Step 1.
Select the menu of the HDD-1000 to "I81. G, B, R".

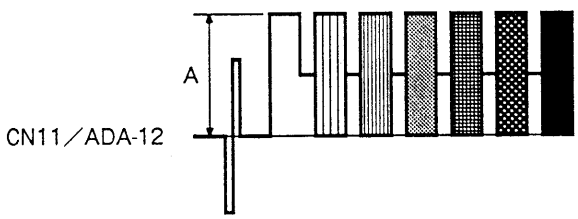
Step 2.
Set S1/SW-334 on the SG-151 board to MANUAL.

Step 3. Check
Turn ⊘RV1/SG-151/B1 fully counterclockwise and check the 100% white level and the frequency response of the CN11 / ADA - 12 / B3 output (terminating with 75 Ω).



Spec. ; 100% white level : A=365 mV or less
Frequency response : 0 to 27 MHz=0±5%
30 MHz=0±$^{5}_{10}$%

Step 4. Check
Turn ⊘RV1/SG-151/B1 fully clockwise and check the 100% white level and the frequency response of the CN11/ADA-12/B3 output (terminating with 75Ω).



Spec. ; 100% white level : A=630 mV or more
Frequency response : 0 to 27 MHz=0±5%
30 MHz=0±$^{5}_{10}$%

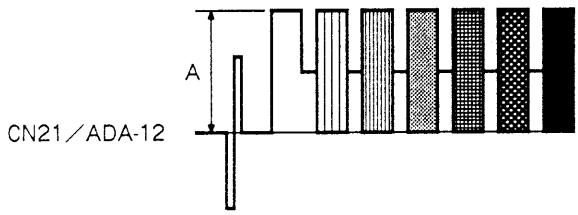
Step 5.
Set ⊘RV1/SG-151/B1 to mid-rotation and S1/SW-334 to FIX position.

8-16. INPUT LEVEL CONTROL CHECK (2)

Equipment ; Oscilloscope
Connection ; See Section 5-4
Mode of HDD-1000 ; EE
Menu Setting ; See text.
Switch Setting ; INPUT/OUTPUT LEVEL CONT. ···FIX.
Input Signal ; Multiburst (G, B, R)

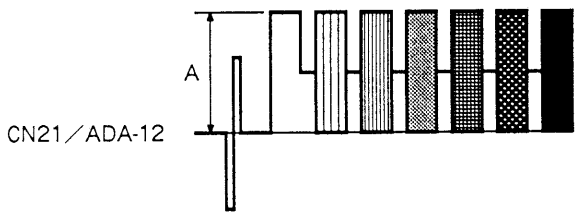
Step 1.
Set S2/SW-334 on the SG-151 board to MANUAL.

Step 2. Check
Turn ⊘RV2/SG-151/B1 fully counterclockwise and check the 100% white level and the frequency response of the CN21 / ADA - 12 / D3 output (terminating with 75 Ω).



Spec. ; 100% white level : A=365 mV or less
Frequency response : 0 to 27 MHz=0±5%
30 MHz=0±$^{5}_{10}$%

Step 3. Check
Turn ⊘RV2/SG-151/B1 fully clockwise and check the 100% white level and the frequency response of the CN21/ADA-12/B3 output (terminating with 75Ω).



Spec. ; 100% white level : A=630 mV or more
Frequency response : 0 to 27 MHz=0±5%
30 MHz=0±$^{5}_{10}$%

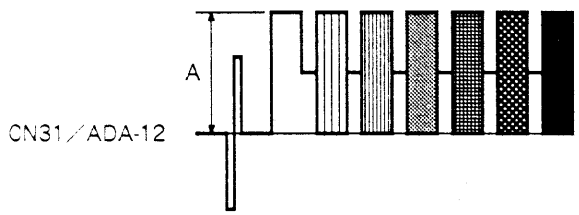
Step 4.
Set ⊘RV2/SG-151/B1 to mid-rotation and S2/SW-334 to FIX position.

8-17. INPUT LEVEL CONTROL CHECK (3)

Equipment : Oscilloscope
Connection : See Section 5-4
Mode of HDD-1000 : EE
Menu Setting : See text.
Switch Setting : INPUT/OUTPUT LEVEL CONT. ···FIX.
Input Signal : Multiburst (G, B, R)

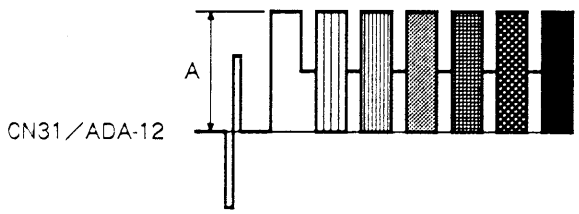
Step 1.
Set S3/SW-334 on the SG-151 board to MANUAL.

Step 2. Check
Turn ⊘RV3/SG-151/C1 fully counterclockwise and check the 100% white level and the frequency response of the CN31 / ADA - 12 / D3 output (terminating with 75 Ω).



Spec. ; 100% white level : A=365 mV or less
Frequency response : 0 to 27 MHz=0±5%
30 MHz=0±$^{5}_{10}$%

Step 3. Check
Turn ⊘RV3/SG-151/C1 fully clockwise and check the 100% white level and the frequency response of the CN31/ADA-12/B3 output (terminating with 75 Ω).



Spec. ; 100% white level : A=630 mV or more
Frequency response : 0 to 27 MHz=0±5%
30 MHz=0±$^{5}_{10}$%

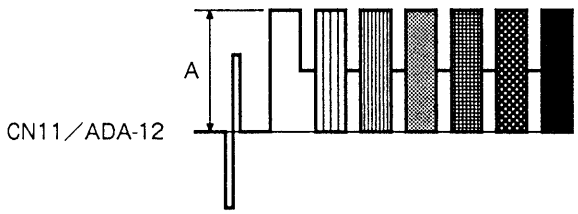
Step 4.
Set ⊘RV3/SG-151/C1 to mid-rotation and S3/SW-334 to FIX position.

8-18. INPUT LEVEL CONTROL CHECK (4)

Equipment : Oscilloscope
Connection : See Section 5-4
Mode of HDD-1000 : EE
Menu Setting : See text.
Switch Setting : INPUT/OUTPUT LEVEL CONT. ···FIX.
Input Signal : Multiburst (G, B, R)

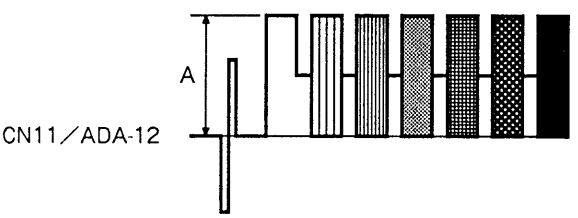
Step 1.
Set S4/SW-334 on the SG-151 board to MANUAL.

Step 2. Check
Turn ⊘RV4/SG-151/C1 fully counterclockwise and check the 100% white level and the frequency response of the CN11 / ADA - 12 / D3 output (terminating with 75 Ω).



Spec. ; 100% white level : A=365 mV or less
Frequency response : 0 to 27 MHz=0±5%
30 MHz=0±$^{5}_{10}$%

Step 3. Check
Turn ⊘RV4/SG-151/C1 fully clockwise and check the 100% white level and the frequency response of the CN11/ADA-12/B3 output (terminating with 75 Ω).



Spec. ; 100% white level : A=640 mV±15 mV
Frequency response : 0 to 27 MHz=0±5%
30 MHz=0±$^{5}_{10}$%

Step 4.
Set ⊘RV4/SG-151/C1 to mid-rotation and S4/SW-334 to FIX position.

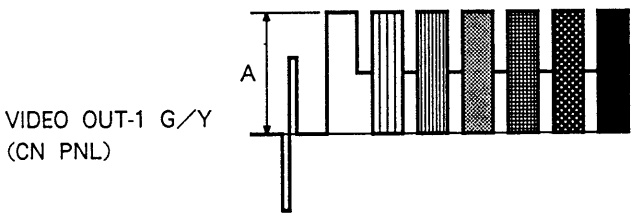
8-19. OUTPUT LEVEL CONTROL CHECK (1)

Equipment ; Oscilloscope
Connection ; See Section 5-4
Mode of HDD-1000 ; EE
Menu Setting ; See text.
Switch Setting ; INPUT/OUTPUT LEVEL CONT. ···FIX.
Input Signal ; Multiburst (Y, P_B, P_R)

Step 1.
Select the menu of the HDD-1000 to "I81. Y, P_B, P_R" and "I83. Y, P_B, P_R".

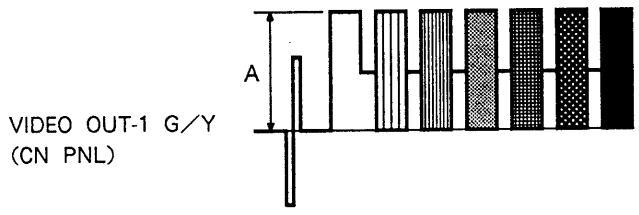
Step 2.
Set S5/SW-334 on the SG-151 board to MANUAL.

Step 3. Check
Turn ⊘RV5/SG-151/D1 fully counterclockwise and check the 100% white level and the frequency response of the VIDEO OUT-1 G/Y output (terminating with 75 Ω).



Spec. ; 100% white level : A=520 mV or less
Frequency response : 0 to 27 MHz=0±5%
30 MHz=0±$^{5}_{10}$%

Step 4. Check
Turn ⊘RV5/SG-151/D1 fully clockwise and check the 100% white level and the frequency response of the VIDEO OUT-1 G/Y output (terminating with 75 Ω).



Spec. ; 100% white level : A=890 mV or more
Frequency response : 0 to 27 MHz=0±5%
30 MHz=0±$^{5}_{10}$%

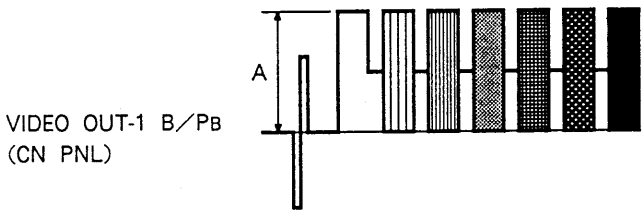
Step 5.
Set ⊘RV5/SG-151/D1 to mid-rotation and S5/SW-334 to FIX position.

8-20. OUTPUT LEVEL CONTROL CHECK (2)

Equipment ; Oscilloscope
Connection ; See Section 5-4
Mode of HDD-1000 ; EE
Menu Setting ; See text.
Switch Setting ; INPUT/OUTPUT LEVEL CONT. ···FIX.
Input Signal ; Multiburst (Y, P_B, P_R)

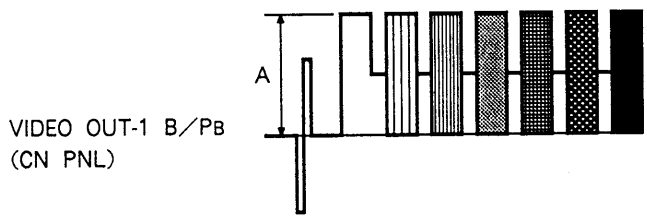
Step 1.
Set S6/SW-334 on the SG-151 board to MANUAL.

Step 2. Check
Turn ⊘RV6/SG-151/D1 fully counterclockwise and check the 100% white level of the VIDEO OUT-1 B/P_B output (terminating with 75 Ω).



Spec. ; 100% white level : A=520 mV or less

Step 3. Check
Turn ⊘RV6/SG-151/D1 fully clockwise and check the 100% white level of the VIDEO OUT-1 B/P_B output (terminating with 75 Ω).



Spec. ; 100% white level : A=890 mV or more

Step 4.
Set ⊘RV6/SG-151/D1 to mid-rotation and S6/SW-334 to FIX position.

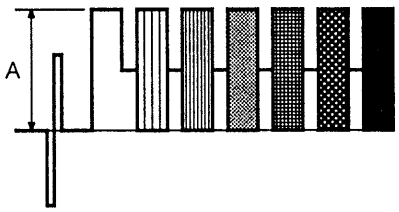
8-21. OUTPUT LEVEL CONTROL CHECK (3)

Equipment ; Oscilloscope
Connection ; See Section 5-4
Mode of HDD-1000 ; EE
Menu Setting ; See text.
Switch Setting ; INPUT/OUTPUT LEVEL CONT. ···FIX.
Input Signal ; Multiburst (Y, P_B, P_R)

Step 1.
Set S7/SW-334 on the SG-151 board to MANUAL.

Step 2. Check
Turn ◐RV7/SG-151/E1 fully counterclockwise and check the 100% white level of the VIDEO OUT-1 R/P_R output (terminating with 75 Ω).

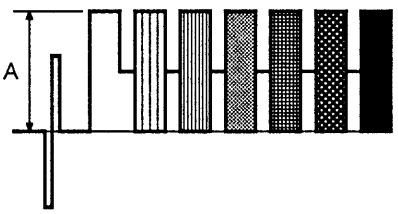
VIDEO OUT-1 R/P_R
(CN PNL)



Spec. ; 100% white level : A=520 mV or less

Step 3. Check
Turn ◐RV7/SG-151/E1 fully clockwise and check the 100% white level of the VIDEO OUT-1 R/P_R output (terminating with 75 Ω).

VIDEO OUT-1 R/P_R
(CN PNL)



Spec. ; 100% white level : A=890 mV or more

Step 4.
Set ◐RV7/SG-151/E1 to mid-rotation and S7/SW-334 to FIX position.

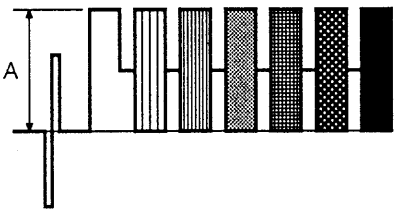
8-22. OUTPUT LEVEL CONTROL CHECK (4)

Equipment ; Oscilloscope
Connection ; See Section 5-4
Mode of HDD-1000 ; EE
Menu Setting ; See text.
Switch Setting ; INPUT/OUTPUT LEVEL CONT. ···FIX.
Input Signal ; Multiburst (Y, P_B, P_R)

Step 1.
Set S8/SW-334 on the SG-151 board to MANUAL.

Step 2. Check
Turn ◐RV8/SG-151/E1 fully counterclockwise and check the 100% white level of the VIDEO OUT-1 G/Y output (terminating with 75 Ω).

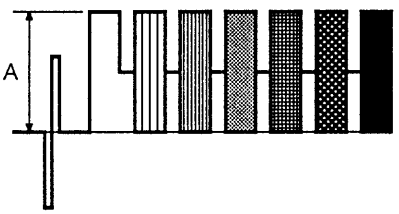
VIDEO OUT-1 G/Y
(CN PNL)



Spec. ; 100% white level : A=520 mV or less

Step 3. Check
Turn ◐RV8/SG-151/E1 fully clockwise and check the 100% white level of the VIDEO OUT-1 G/Y output (terminating with 75 Ω).

VIDEO OUT-1 G/Y
(CN PNL)



Spec. ; 100% white level : A=890 mV or more

Step 4.
Set ◐RV8/SG-151/E1 to mid-rotation and S8/SW-334 to FIX position.

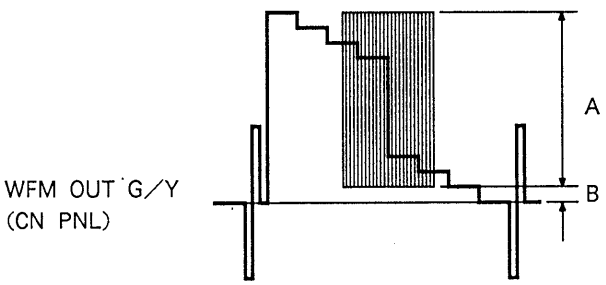
8-23. CHARACTER LEVEL ADJUSTMENT

Equipment ; Oscilloscope
Connection ; See Section 5-4
Mode of HDD-1000 ; EE
Menu Setting ; See text.
Switch Setting ; INPUT/OUTPUT LEVEL CONT. ···FIX.
Input Signal ; Color bar (Y, P_B, P_R)

Step 1.
Select the menu of the HDD-1000 to "S59. MONITOR" and "I66. ENABLE".

Step 2. Pedestal Level Adjustment
Serial No : Up to 10199
Observe the VIDEO OUT-1 G/Y connector. Adjust so that the pedestal level becomes ground level.
Spec. ; 0±25 mV (terminating with 75 Ω)
● RV403/ADA-12/K3

Step 3. Character Level Adjustment
Observe the WFM OUT G/Y connector and adjust the white level (A) and the black level (B) of the superimposed character.



Spec. ; Character white level A=700±10 mV
(terminating with 75 Ω)
● RV803/ADA-12/F5
Character black level B=70±10 mV
(terminating with 75 Ω)
● RV802/ADA-12/F5

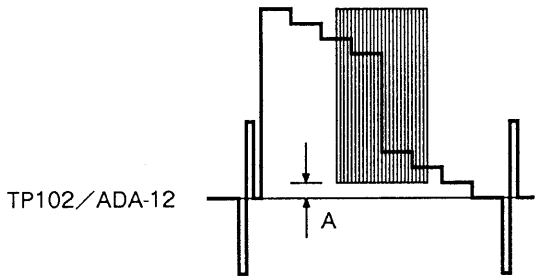
Serial No : 10201 and higher

8-24. CHARACTER OFFSET LEVEL ADJUSTMENT

Equipment ; Oscilloscope
Connection ; See Section 5-4
Mode of HDD-1000 ; REC CONFI
Menu Setting ; See text.
Switch Setting ; See Section 5-5
Input Signal ; Color bar (Y, P_B, P_R)

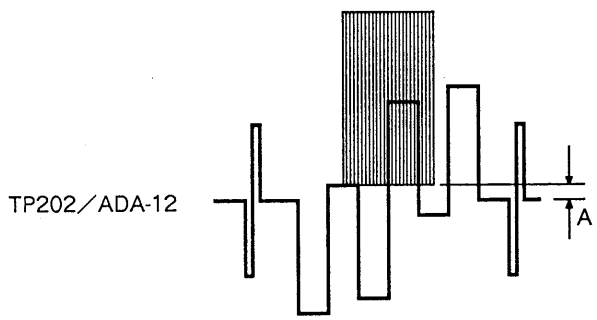
Step 1.
Selet the menu of the HDD-1000 to "S59. MONITOR" and "I60. ENABLE".

Step 2. Y REC Character Offset Level Adjustment



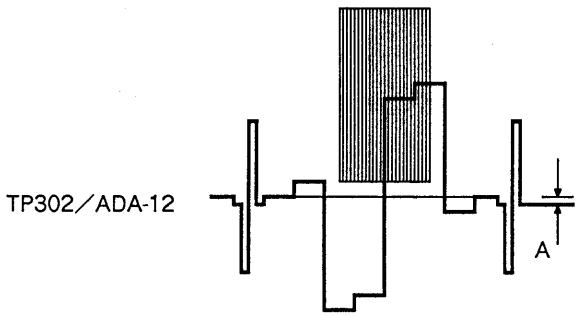
A=0±100 mV

Step 3. P_B REC Character Offset Level Adjustment



A=0±100 mV
● RV204/ADA-12/B5

Step 4. P_R REC Character Offset Level Adjustment



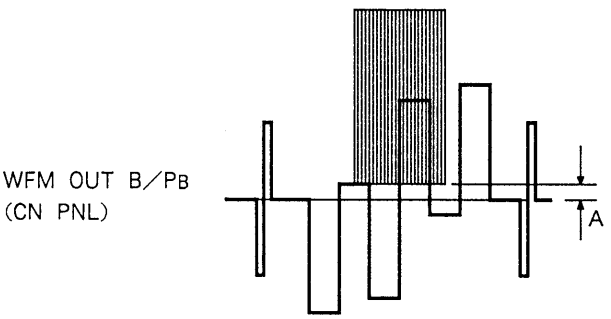
A=0±100 mV
● RV304/ADA-12/D5

Serial No : Up to 10199

8-25. OUTPUT OFFSET ADJUSTMENT

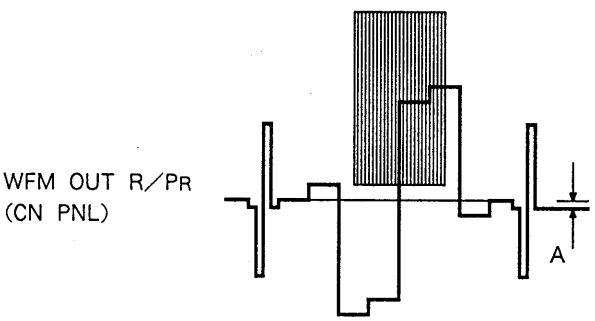
Equipment : Oscilloscope
Connection : See Section 5-4
Menu Setting : See text.
Switch Setting : INPUT/OUTPUT LEVEL CONT. ···FIX
Input Signal : Color bar (Y, P_B, P_R)

Step 1. P_B Offset Level Adjustment
Observe the WFM OUT B/P_B connector. Adjust so that the character black level of the P_B signal becomes pedestal level.



Spec. ; A=0±10 mV (terminating with 75 Ω)
● RV503/ADA-12/L4

Step 2. P_R Offset Level Adjustment
Observe the WFM OUT R/P_R connector. Adjust so that the character black level of the P_R signal becomes pedestal level.



Spec. ; A=0±10 mV (terminating with 75 Ω)
● RV603/ADA-12/M3

Step 3. G/B/R Offset Level Check
Observe the VIDEO OUT-1 G/Y, B/P_B and R/P_R connector on the connector panel and check the pedestal level of respective G/B/R signals.

Y : 0±50 mV (terminating with 75 Ω)
P_B : 0±50 mV (terminating with 75 Ω)
P_R : 0±50 mV (terminating with 75 Ω)

8-26. INTERNAL MODE ADJUSTMENT

Equipment ; Frequency counter
Switch Setting ; See Section 5-5 and text.
Input Signal ; No signal

Step 1.
Set S3/SG-151 BIT3 to INT and BIT8 to TEST.

Step 2.
Turn ON the power and warm-up for 10 minutes.

Step 3.
Connect frequency counter to pin1 of ICG15 and adjust ◐ RV9.
Spec. ; 74.25 MHz±50 Hz
◐RV9/SG-151/C13

Step 4.
After adjustment, restore S3/SG-151 BIT3 to GEN and BIT8 to NOR.

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