SONY®

Training Manual

High Definition Television

Circuit Description and Troubleshooting

Course: DTV-01

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Standard Definition/High Definition

Picture resolution is commonly measured in pixels or lines. The number of pixels is the number of black to white brightness changes possible on the screen first in a horizontal, then in a vertical row (e.g. 960x480). CRT manufacturing tolerances limits the number of pixels possible. This is a common resolution specification in a computer monitor CRT.

In a TV broadcast, the studio camera is the limitation to higher resolution. The picture scanned by the camera is segmented by pixels similar to the viewer's CRT. The greater the number of pixels in the horizontal and vertical row, the greater the resolution. This will be the current resolution limitation as the USA makes the transition toward high definition digital TV.

In a TV transmission, the ability of a signal voltage to quickly change from low to high and to produce a dark to white transition is comparable to a pixel. This is not a limitation in the transmission format, but the number of lines transmitted is and is used as a resolution measurement in transmissions. The number of lines transmitted in the current USA NTSC format is 525. This is considered a standard definition (SD) transmission.

A standard definition (SD) transmission of 525 lines can be transmitted in the analog or digital mode. A higher definition (HD) transmission can be transmitted only in the digital (DTV) mode.

- SDTV or SD – Standard definition is the current 525 lines of resolution transmitted, but only 480 of those lines are viewable. SD can be sent as an NTSC analog or digital (DTV) transmission.
- HDTV or HD – A high-definition transmission contains 720 or more horizontal lines. HD is transmitted only in a digital format.
- DTV – A digital TV transmission refers only to the digital encoding of the picture signal that may contain either a high (HD) or low (SD) resolution picture. The digital picture is not viewable on an analog TV without a "decoder box".

Digital Transmission Formats

There are 18 approved digital transmission formats. The first six offer HD signals in a 16x9 aspect ratio. The remaining 12 formats are SD signals in progressive (p) or interlaced (i) scan. Although not high resolution, they offer significant improvements over the NTSC analog signal.

18 Digital Transmission Formats					
Resolution	Aspect Ratio	Frames	Resolution	Aspect Ratio	Frames
1. 1920x1080	16:9	30 i	10. 704x 480	16:9	24 p
2. "	16:9	30 p	11. "	4:3	60 p
3. "	16:9	24 p	12. "	4:3	30 i
4. 1280x 720	16:9	60 p	13. "	4:3	30 p
5. "	16:9	30 p	14. "	4:3	24 p
6. "	16:9	24 p	15. 640x 480	4:3	60 p
7. 704x 480	16:9	60 p	16. "	4:3	30 i
8. "	16:9	30 i	17. "	4:3	30 p
9. "	16:9	30 p	18. "	4:3	24 p

A standard definition transmission permits space for another digital video stream to coexist on the same frequency (channel). Consequently a station can have more than one program stream on a digital channel. The maximum number is not known at this time.

How to use this book for servicing

When encountering this TV set for servicing there are several things you need to know. Below is a list of the necessary servicing items and where to locate them:

Servicing Needs	
Information	Location
1. Hookup / Operation / Normal Operation	First document in this training manual (Normal Operation)
2. External HDTV set-back box indicator lights	Appendix
3. Location of power handling parts and fuses	Service manual / visual inspection of heat sinks
4. Standby light indication message & board determination	Service manual and Protection Block document
5. Shutdown troubleshooting plan	Protect Circuitry 3 & 4
6. Power Supply, Deflection, Video Selection and Signal Flow Circuitry	Circuitry in this training book. See table of contents.
7. Focus Circuitry	Circuitry in this training book
8. Dynamic Convergence adjustments	Service manual page 27 (same as in training manual supplement)
9. Adjustments after tube replacement	Notes on using the service mode follow this chart. A list of register names are in the service manual. Training manual supplement

Service Mode Adjustment Notes

Because of this TV's complexity, the following precautions should be noted while making service adjustments for convergence, video level, size, and white balance or positioning:

1. The numerous service mode registers are usually grouped by ICs for easy access. Use the remote's #2 and #5 button to change IC groups. Then you can move from register to register with the #1 and #4 buttons.
2. Each register that controls the picture's size, deflection and position (on pages 45-47 of the service manual) has seven sets of adjustment data, one for each of the seven picture size modes. These settings do not interact. Enter the service mode, adjust the TV during that picture size, and store it.

Seven Picture Size Modes		
NTSC or SD DTV		HDTV
1. Normal 4:3 aspect ratio	4. Wide Zoom	6. HDTV Full
2. Full 16:9 aspect ratio	5. Caption (Top & bottom pix compressed)	7. HDTV Twin View
3. Zoom		

1. Some registers are duplicated under different groups for ease of adjustments. These duplicated registers have the same name. Changing the register data at one location causes the data to change at the other location as well.
2. Save adjustments often. Changing registers will hold the new data, but changing picture sizes (zoom, full, caption, etc) will instantly lose any unsaved data that was just held.
3. There are separate contrast, color level, and hue adjustments for:
   - The main picture
   - The HDTV picture
   - Each twin view picture

   They are adjusted for equal levels as you switch modes. This is so the picture is not brighter in one mode than another.

Introduction to MPEG-2 Compression

MPEG stands for Motion Picture Experts Group, named after the committee that developed the standard.

Why Compress?

MPEG defines a compression scheme for Video which evolved from the need to transmit digital video on existing communication channels with limited bandwidth. In addition to the bandwidth issue there is an obvious storage one as well.

Fastest Communication Channels	**Typical Bandwidth**
ISDN Line	144Kbps
T1 Line	1.5 Mbps
T3 Line	45 Mbps

With a whopping 4.7 gigabytes of data capacity, DVD-Video would seem to have more than enough room for motion pictures. Unfortunately, digital video has an incredibly voracious appetite for storage.

Raw or uncompressed Digital Video requires an enormous 252 Megabits/sec of bandwidth and approx 31 Mbytes per second of storage.

720x480 (Res.) X 8bits/sample X 30frames/sec X 3 Components

To understand this figure, we need to understand video in its purest form.

Component Video

In its purest form, Video is made up of 4 components.
- Luminance or Y which defines the brightness level and
- Color which is made up of 3 components called R-Y, B-Y and G-Y.

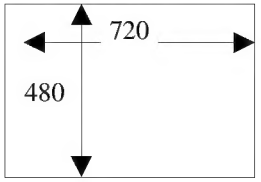
As it works out, we can mathematically calculate the 4th component (G-Y) from the others. Therefore, we only require 3 components for Video (Y, R-Y and B-Y).

$$Y = (R-Y) + (B-Y) + (G-Y)$$

Each sample we take of the video is represented by an 8 bit digital word which translates to 2^8 or 256 different levels of each component. Therefore, each pixel is made up of 3 components which can represent up to 2^8 (Y) X 2^8 (R-Y) X 2^8 (B-Y) = 2^{24} (commonly known as 24 bit color)or 16 million colors.

One PIXEL

The resolution or picture detail we require also plays an important role in our bandwidth and storage requirement. DVD uses a 720 Horizontal by 480 Vertical resolution or 720 pixels across times 480 rows or lines.



In summary we need to:
- sample 3 components (Y, R-Y and B-Y) each of which is composed of 720 x 480 (350,000) pixels.
- Represent each one by an 8 bit word (3 X 350,000 X 8 = 8,400,000bits). Therefore, each frame is made up of 8,400,000 bits.
- Finally, we would need to display at 30 frames per second (30 X 8,400,000 =252,000,000 bits/sec or 252 Mbits/sec Bandwidth.

To calculate the storage we simply divide the Bandwidth in bits by 8 bits per byte and we get 31.5Mbytes/sec Storage requirement.

As illustrated, the requirement is enormous which paves the way for compression and MPEG.

Compression Process

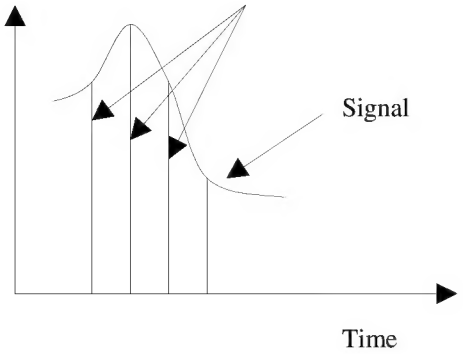
Compression of Video is accomplished via the following process.

1. Selective Sampling
2. Discrete Cosine Transform (DCT)
3. Predictive & Motion Encoding
4. Hoffman Encoding

Selective Sampling

The number of times per second that you sample a signal is called its sampling frequency. In Audio, the sampling frequency is 44,000 samples/sec which is approx 2 times the highest frequency in Audio (20,000 Hz). In contrast, Video is sampled at 4 times the highest frequency (13.5Mhz). Hence the term 4 in the sampling structure 4:4:4 representing the sampling ratio of Y, R-Y and B-Y respectively.

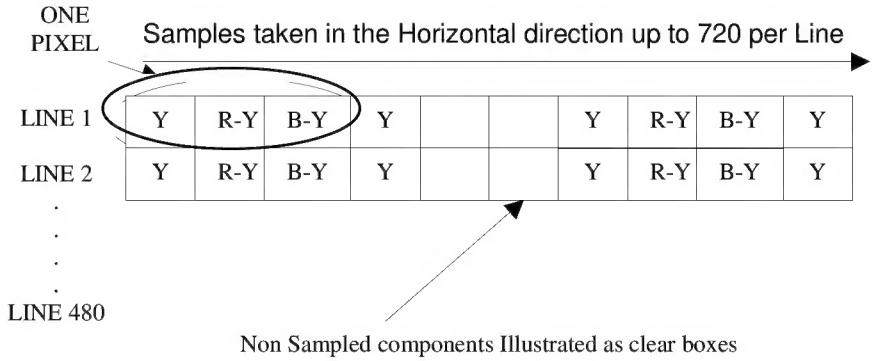
Therefore, the same number of samples are taken of Y as they are of R-Y and B-Y.



4:2:2

Since the eye is less perceptive to color changes than to Luminance, significant reduction of data can be accomplished in the Sampling process if we sample the color components (R-Y and B-Y) half as much as the Luminance component (Y). The result is a 1/3 reduction or a bandwidth of 166Mbits/sec.

Video sampled using this technique is represented by a 4:2:2 sampling structure. Y is sampled normally with R-Y and B-Y sampled half as much.

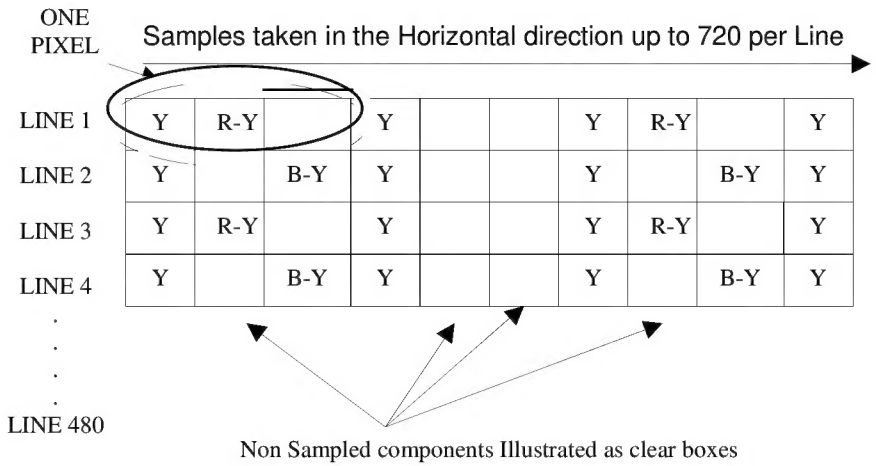


4:1:1

Consequently techniques such as the 4:1:1 further reduce color sampling to 1/4th of the Y component and compress by ½ or reduce bandwidth to 125Mbits/sec.

4:2:0

DVD takes it to another level by using a modified 4:2:2 sampling structure called 4:2:0. 4:2:0 samples R-Y half as much as Y and skips B-Y on the 1st line. However, on the next horizontal line, B-Y is sampled half as much as Y and R-Y is skipped. This routine is repeated effectively reducing the color components by another half achieving ½ compression or a 125Mbit/sec bandwidth.
Through interpolation, the 4:2:0 is reconstructed into 4:2:2 without the extra bandwidth requirement.



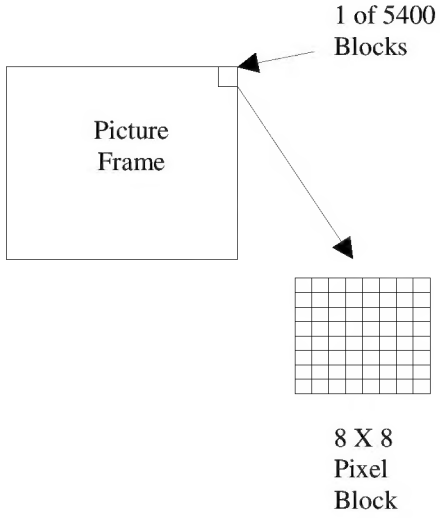
Discrete Cosine Transform

After the Selective Sampling process is complete, the next step in the MPEG process is to remove very fine picture detail imperceptible to the human eye. It is imperceptible because it is typically masked by other picture content.

In a Video Frame, the very fine picture details consist of high frequency information which are basically fast changing Luminance and Color content. In contrast, low frequency information are slow changing Luminance and Color content.

The high frequency information consumes the most data real estate and is where we focus to compress in this next stage.

The process of eliminating the imperceptible information is called Discrete Cosine Transform or DCT. The sampling process converts the information into digital data as described previously. Each digital picture frame is then sectioned off into 5400 blocks each consisting of 8 pixels wide X 8 pixels high.



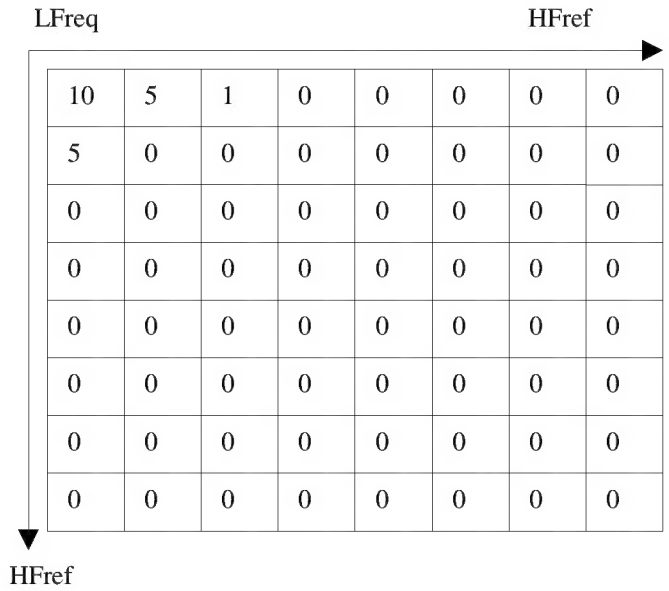
DCT transforms the 8X8 group of pixel values into frequency components.

Although pixel values vary randomly in the 8X8 block, DCT re-positions low frequency components on the upper left corner and high frequency components on the lower right of the block.
Through an additional numerical conversion process called “Quantization”, frequency component values are assigned.

High freq components are identified by the zero values (lower right) and low freq components by the larger values (upper left).

Data compression is accomplished by elimination of the high frequency components designated by the zeros.

8 X 8 Pixel Block



10	5	1	0	0	0	0	0
5	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0

Spacial Redundancy

Within a Frame, there are many redundant pixels. An example would be a blue sky. This type of redundancy within the Horizotal and Vertical plane of a frame is called “Spacial Redundancy”.

One pixel could be stored with information to repeat for the remaining pixels. This would eliminate the need to store every pixel in the frame.

Frames making use of this technique are called “Intra-Frames”.

Temporal Redundancy

Within Video scenes, there are many redundant frames. An example would be an anchor person reporting the news. With the exception of lip movement, the other portions of the frame remain unchanged over time. This type of redundancy over time is called “Temporal Redundancy”.

The first frame could be stored as the reference or non changing portions while remaining frames carry the lip motion information. This would eliminate the need to store several full frames.

Frames using Temporal redundancy which predict information based on preceding frames are called “Inter-Frames” or Motion predicted Images.

Predictive & Motion Encoding

The next step in the MPEG process is termed “Predictive & Motion Encoding” and it takes advantage of both Spacial and Temporal redundancy to achieve compression.

I-Pictures

To begin the process of using Spacial and Temporal redundancy techniques in compression, we need a reference or a start frame which does not depend on previous or preceding frames.

This start frame would make use of Spacial redundancy within itself and is termed an I picture.

I pictures are Intra-Frames and have zero dependency on previous or preceding frames. They do however provide information to preceding frames.

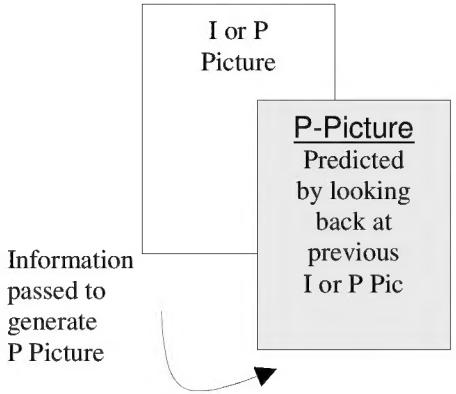
The other pictures types used by MPEG are called P-Pictures (Predictive) and B-Pictures (Bi-Directional).

I Pictures carry the most amount of data content. They are 3 times the size of a P-Picture and 5 to 6 times the size of a B-Picture.

P-Pictures

The P-Pictures are Predictive Encoded Images also known as Inter-Frames.

As the name indicates, a P-Picture is a predicted Image based on previous I or P-Picture. The P-Picture is dependent on past Images to exist.

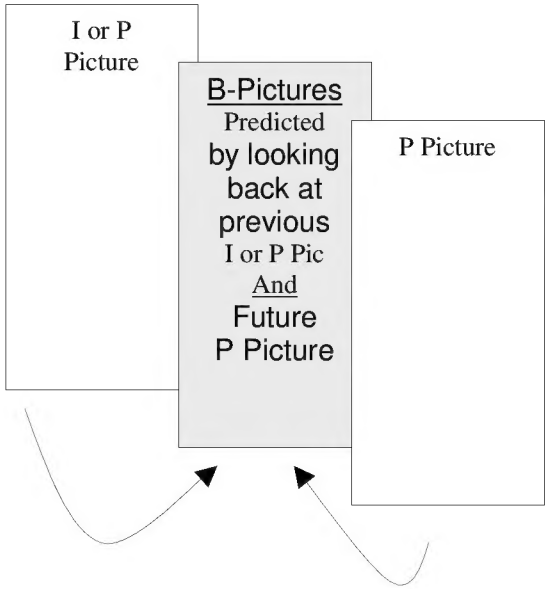


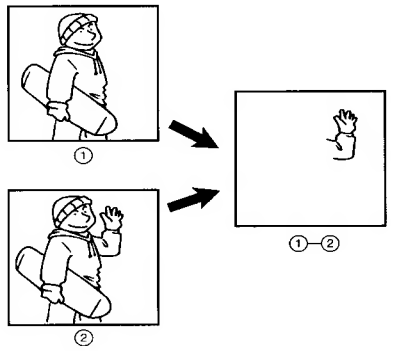
B-Pictures

The B-Pictures have Bi-directional dependency and are called Bi-Directional Predicted Images.

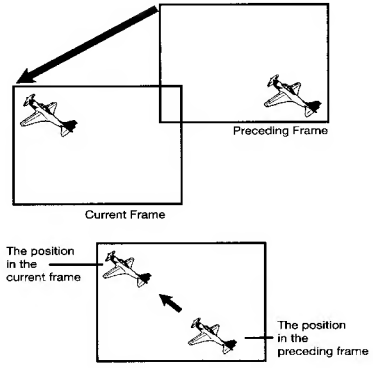
The B-Picture is also a predicted Image but it is based on prior I or P Pictures and preceding P-Pictures.

B-Pictures are typically made up of motion information and carry the least amount of data.





1. Pictures (1) and (2) to be reproduced as time elapses have many elements common to each other. Differential or (1) minus (2) is extracted and (2) is reproduced by synthesizing the differential with (1).



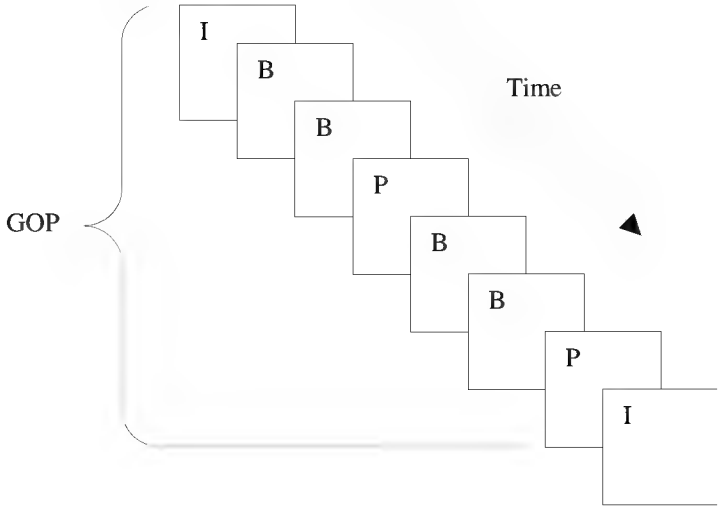
2. In the motion compensation process, pictures are divided into blocks and the motion vector which indicates the amount of movement is extracted and coded for the part whose position is changed, without changing its shape. By combining this motion compensation with predictive coding, data is more efficiently compressed.

I, P and B picture generation process

To clearly understand the relationship between the I, P and B pictures we need to understand how they are generated.

1. The start of an entirely new scene would require an I-Picture or a reference for other pictures to follow until the next I-Picture.
- The information between the I-Picture and the next reference I-Picture is called a GOP (Group of Pictures) which consist of one I and many P and B Pictures.
- I-Pictures typically re-occur at 15 picture intervals.

1. Next, the first P-Pictures in the GOP is generated based on the I-Picture.
2. In between the I and first P-picture, several B-Pictures are generated as necessary to convey motion information from the I to the first P-Picture. For this reason B-Pictures are dependent on past and future pictures.
3. Then the process repeats with the generation of second P-Picture which is now based on the first P-picture. And so on…



Hoffman Encoding

The last step in the MPEG process uses a statistical approach to compress the data further.
The last process is called Hoffman Encoding. Basically, this process takes a look at the string of MPEG data and replaces it with information which allows regeneration.
The best example is a string of eight “1’s” {11111111} replaced by {1x8} which represents; repeat the 1 eight times.

MPEG II –vs- MPEG I

The MPEG process described is common to both MPEG II and MPEG I thus, explaining the backward compatibility between the two.

The main differences between MPEG II and I are:

- MPEG II used in DVD uses a 720 x 480 resolution while MPEG I used in VIDEO CDs carries a resolution of 350 x 240. This difference alone accounts for a 75% reduction in data using MPEG I over MPEG II.
- MPEG II compresses data to about 1/40 on average while MPEG I compresses data to about 1/140 on average. Therefore 250Mbit/s are reduced to 6.25Mbits/s on average using MPEG II.
- MPEG II uses a variable rate compression while MPEG I uses a fixed rate.

350 x 240 = 84,000 pixels
720 x 480 = 350,000 pixels
MPEG I represents
84,000/350,000 = 25% of MPEG II.

MPEG II additional information

MPEG II is a broad standard which encompasses many resolutions including HDTV. These variations in MPEG II are defined by Levels and Profiles.

DVD is just one of the many profiles and levels defined by MPEG II called Main Profile at Main Level (MP@ML).

Video and Sound Specifications for DVD-Video

		DVD-Video		Video CD
video	video compression system	MPEG2 (MP@ML)		MPEG1
	resolution (pixels)	720 dots x 480 lines (Note1)		352 dots x 240 lines (Note1)
	horizontal resolution	approx. 500 TV lines		approx. 240 TV lines (same as VHS)
	compression ratio	approx. 1/40		approx. 1/140
	video bit rate	9.8 Mbps, max. (variable)		1.15 Mbps (fixed)
	field/frame	field/frame		frame
	aspect ratio	4:3 / 16:9(pan scan/letter box)		4:3
audio	audio	8 streams, max. (Note 2)		2 channel (stereo)
	audio system	Dolby Digital AC-3	Linear PCM	MPEG1 layer 2
	audio bit rate	448 kbps, max (per stream)	6.144 Mbps, max (per stream)	224kbps(fixed)
	number of channels	5.1 ch, max. (per stream)	8 ch, max. (per stream)	2 ch only
	quantization bit sampling frequency	48 kHz	16-bit, 20-bit, 24-bit 48 kHz, 96 kHz	16-bit 44.1kHz
others	subtitles	2 bits, run length bit map system, 32 streams, max.		open caption only

Note 1: If compatible with NTSC. Note 2: Either Dolby Digital AC-3 or Linear PCM can be selected for each audio stream.

Level \ Profile	Simple	Main	SNR Scalable Note 2	Spatial Scalable	High
High 1920 x 1080 x 30 or 1920 x 1152 x 25 Note 1		MP@HL US digital HDTV			HP@HL
High - 1440 1440 x 1080 x 30 or 1440 x 1152 x 25 Note 1		MP@H1440		SSP@H1440 European digital HDTV	HP@H1440
Main 720 x 480 x 29.97 or 720 x 576 x 25 Note 1	SP@ML Digital transmission cable TV	MP@ML Note 3 DVD-Video Digital satellite broadcasting (DirecTV and others)	SNP@ML		HP@ML
Low 352 x 288 x 29.97 Note 1		MP@LL	SNP@LL		

Note 1: Shows the standard number of horizontal pixels x vertical pixels x frame frequency
Note 2: SNR = Signal Noise Ratio
Note 3: MP@ML = Main Profile at Main Level

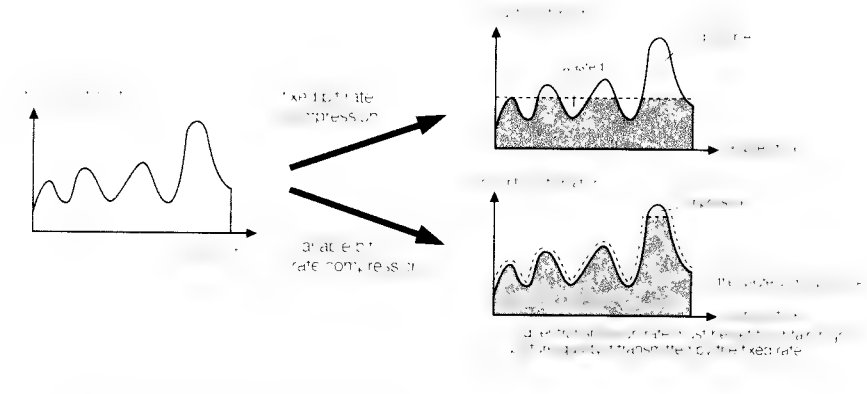
The Bit Rate Fluctuates

For DVD, variable bit rate is a tremendous advantage. If the bit rate were fixed, it could not accommodate the changing needs of video scenes. Consider the fast-paced action of a football player, running for a touchdown as the camera pans past the crowd. Full of motion, this is an extremely demanding scene, one that requires the bit rate to be very high. Now picture the same football player after the game, sitting in a restaurant, talking to his girlfriend. Almost nothing in the scene moves, so the bit rate can be quite low.

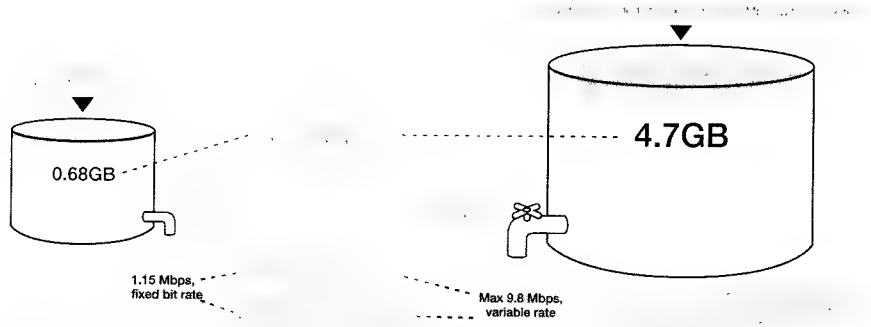
If DVD used a fixed bit rate, the system might fall short on the football scene. And it would definitely be wasting bits on the restaurant scene. DVD-Video accommodates both scenes by varying the bit rate. In fact, the maximum bit rate is 9.8 megabits per second which is nearly three times as high as the "average" rate.

If DVD used a fixed rate, it would have to be at least 7 Mbps to maintain picture quality! At that rate, total recording time would be cut in half. So the goal of capturing a full-length movie on a 3-3/4-inch disc could not be realized. Variable bit rate is one of the key technologies that makes DVD possible.

By the way, Video CD uses MPEG-1 to yield a fixed bit rate of 1.15 Mbps. The fixed rate and low number translate into the vast quality difference between DVD-Video and Video CD.



Transmission Rates Of Video CD And DVD-Video



DVD-Video

video data input

data is compressed to about 1/40 on average by MPEG2

- motion compensation (compressed by correlation between pictures) about 1/2
- Discrete Cosine Transform (compressed by correlation within pictures), about 1/10
- Huffman Coding (compressed by correlation of code rows), about 1/2

variable rate compression

data is distributed efficiently according to difference in video data volume

picture quality nearly equivalent to studio-use master tape (D1)

Video CD

video data input

data is compressed about 1/140 on average by MPEG1

- motion compensation (compressed by correlation between pictures), about 1/5
- Discrete Cosine Transform (compressed by correlation within pictures), about 1/14
- Huffman Coding (compressed by correlation of code rows), about 1/2

fixed rate compression

data is distributed evenly regardless of differences in video data volume

picture quality equivalent to home use VHS video

24 Frames-per-Second Storage

In video, what appears to be a continuously moving image is actually a series of discrete still pictures, called frames. Every video frame consists of two interlaced “fields”, each of which contains half the frame’s scanning lines. A U.S.-standard video picture runs at roughly 30 frames per second. In contrast, movie file operates at 24 frames per second. So the movies you see on television, cable or videocassette have all had their frame rates converted by a special machine called a “telecine”.

The telecine converts the 24 film frames into video fields. However, video requires 30 frames or 60 fields and Film is 24. Telecine performs this process by converting 12 film frames to 24 fields (2 Fields/Film Frame) and another 12 film frames to 36 fields (3 Fields/Film Frame). It is kept seamless by converting one Film Frame to 2 Fields and the next one to 3. This cycle is repeated 2, 3, 2, 3 until the 60 fields have been completed. This Telecine process is called 2-3 Pull Down.

To achieve maximum recording time, the DVD-Video disc is actually mastered in the original 24 film frame format. This reduces the video bit rate by 20%, even before MPEG-2 encoding. During playback, the DVD-Video player performs the 2-3 pull down function to generate a standard 30 frames per second video output.

NOTES

Model KW-34HD1 - Normal Operation

These are normal operating conditions for Sony's first high Definition TV during power on/off and input selection conditions.

Power ON

Operation	Initial Step	Sounds	Visual	Conditions
Plug in	AC connection	Nothing	Nothing	Front panel Master power button off
Power ON A	Master power ON button pressed	1. 2 Relays click immediately 2. Degaussing coil energized (humming sound) 3. TV audio 1 sec after relays click	1. Front panel Standby light: 2. Blinking after relay click 3. Stops blinking in about 7 seconds when the picture appears. 4. OSD: Yellow characters "Please check DTV receiver connections"	AC connected. Set formerly OFF (by remote). 1.3 Amps @120Vac
Power ON B	Power ON in remote pressed	1. 2 Relays click immediately 2. Degaussing coil energized (humming sound) 3. TV audio 1 sec after relays click	1. Front panel Standby light: 2. Standby light starts blinking after relay click 3. Stops blinking in 7 seconds when the picture appears. 4. OSD reads in Yellow characters "Please check DTV receiver connections".	AC connected. Master power button ON Standby light ON TV OFF 1.3 Amps @120Vac
TV OFF A	Master Power OFF pressed	2 relays clicks TV sound mutes	Picture goes dark All lights out	
TV OFF B	Remote power OFF pressed	2 relays clicks TV sound mutes	Picture goes dark Standby light comes ON	

When this TV is ON there is no static electricity felt at the CRT screen.
It is normal to have black left & right borders on both sides of the picture when viewing a 4:3 aspect ratio picture on a 16x9 aspect ratio TV picture tube.

TV Operation with NO Inputs connected

Selection	Access Step	Sounds	Visual	Conditions
Video input	Press TV/Video button until video 1, 2, or 3 appear on the screen	No sound when there is no video input.	Video 1, 2, or 3 appears in green letters at the upper left corner of the screen. Screen is dark with no video input.	Power ON No inputs
DVD, HD, input or High Definition TV input from external box	Press TV/Video button until DVD or HD input is selected.	No sound when there is no input.	DVD or HD appears in green letters at the upper left corner of the screen. Screen is dark with no input.	Power ON No inputs
VHF / UHF input	Press the TV button on the remote	Off the air white noise from the unconnected VHF/UHF input.	OSD station number appears in green at the upper right corner of the screen with snow. TV channels can be entered by remote or the up/down buttons will work if stations were programmed during set up.	Power ON No inputs
Cable Input	Press the TV button on the remote	Off the air white noise from the unconnected cable input.	OSD "C _" appears in green at the upper right corner of the screen with snow. Cable channels can be entered by remote or the up/down buttons will work if cable stations were programmed during set up.	Power ON No inputs

Input Selection

Input	Connections	Programming Steps	Results
VHF / UHF	VHF / UHF antenna to rear panel "VHF / UHF" F type connector.	1. Power **ON.** 2. Use the remote **TV**/Video button to select TV. 3. The remote ANT button toggles between VHF / UHF and cable. Select **VHF / UHF** (channel number without a C prefix). 4. From the 4rd Menu icon, select & enter "**Auto Program: VHF / UHF**". 5. Use Channel Up/Dwn to change stations for normal operation.	1. See previous Power ON chart. 2. Snow or a TV station with a channel number will appear if you are correctly in the TV mode. 3. Correct VHF / UHF channels will be numbered 2-69. Cable channels are preceded with a letter C like C78. 4. It takes almost 1 min. to scan through all the VHF / UHF stations. At the end it will select the lowest active VHF station.
Cable	Connect cable feed to rear panel "Cable" F type connector.	1. Power **ON.** 2. Use the remote **TV**/Video button to select TV. 3. The remote ANT button toggles between VHF / UHF and **cable**. Cable station numbers are preceded with a letter "C". Select a C prefix station like C4. 4. From the 4rd Menu icon, select & enter **"Auto Program: Cable".** 5. Use Channel Up/Dwn to change stations for normal operation.	1. See previous Power ON chart. 2. Snow or a TV station with a channel number will appear if you are correctly in the TV mode. 3. Correct Cable channels will be displayed as C1 to C125. 4. It takes about 1 min. to scan through all the cable stations. At the end it will select the lowest number active cable station.
High Definition TV	Connect an UHF antenna to the DTV Receiver (external set-back box) and the receiver to the rear of the TV using the supplied multi-pin I/O cable.	1. Power **ON.** 2. Use the remote TV/Video button to select **TV.** 3. The remote ANT button toggles between VHF / UHF and cable. Select **VHF / UHF** (without a C prefix). 4. From the 4rd Menu icon, select & enter "**Auto Program: VHF / UHF**". This tells the set-back box to auto program DTV stations too. ("DTV Auto Add" is only used to add DTV stations after one was found.). 5. Use Channel Up/Dwn to change stations for HDTV reception.	1. See previous Power ON chart. 2. Snow or a TV station with a channel number will appear if you are correctly in the TV mode. 3. Correct VHF / UHF channels will be numbered 2-69. Cable channels are preceded with a letter C like C78. 4. It takes about 1 min. to scan through all the VHF/UHF stations. At the end it will select the lowest number active station.
DVD, Video 1-3, or HD	Connect the video and audio cables of the DVD, VCR, game, or camcorder to the rear panel phono jacks. The video 2 input is located on the front panel. The HD box has component video (Y, R-Y, B-Y) outputs. They plug into the HD input (phono jacks).	1. Power **ON.** 2. Use the remote TV/Video button to select the desired input.	1. See previous Power ON chart. 2. The OSD will show the input selected as you press the TV/Video button. The input sequence is: Video 1-3, DVD, HD, TV and it repeats.

Inputs

RF Inputs

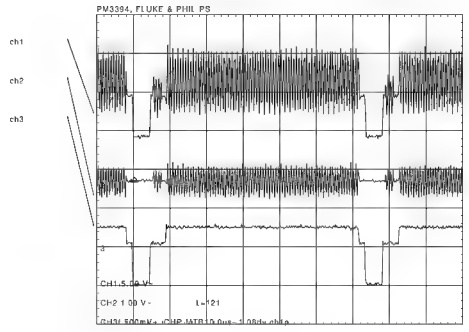
There are three independent RF inputs which allow the user to have cable, an outdoor antenna aimed for VHF and UHF stations and another antenna oriented for digital TV stations. Each RF input has a channel numbers assigned to it:

RF Channel Number Assignment	
Input	Channel Numbers
Cable	1-125
VHF / UHF	2-13 / 14-69
DTV	1-99

They are selected from the ANT remote control button.

Composite Video

This is a single video 1, 2, or 3 input cable that carries the combined Y and C signal. The TV/Video remote control button selects it. This composite signal requires the receiver to first separate the two components, usually using a comb filter. The chroma is demodulated into individual color components, such as RGB, before the color information can be used. These additional processing steps reduce resolution and could add noise, but composite video is a convenient method of transporting a video signal.



This scope shot is taken of a video signal that produces a blue screen. The top waveform is composite video and contains a combined signal. The middle waveform is the chroma signal from the S video output. It contains the burst after the retrace blanking area. The bottom waveform is the luminance signal containing the H sync pulse below the base line.

S Video Input

The S input refers to Separate Video inputs consisting of independent luminance (Y) and chroma (C) signals and a shield wire for each. They are input using a 5 pin standard connector. The fifth pin serves to close a switch in the jack that identifies the presence of the S video plug. The S Video signal is selected instead of the composite video 1-3 when the S video plug is detected.

The S video's luminance signal is the picture's brightness level signal. This Y input signal also carries both of the horizontal and vertical sync pulses. The chroma signal contains the color information phase referenced to the burst frequency of 3.58MHz. This C input contains 8 cycles of reference burst signal in the open retrace interval. The chroma signal requires demodulation into individual color components such as RGB before the color information can be used.

Component Video

Conversion

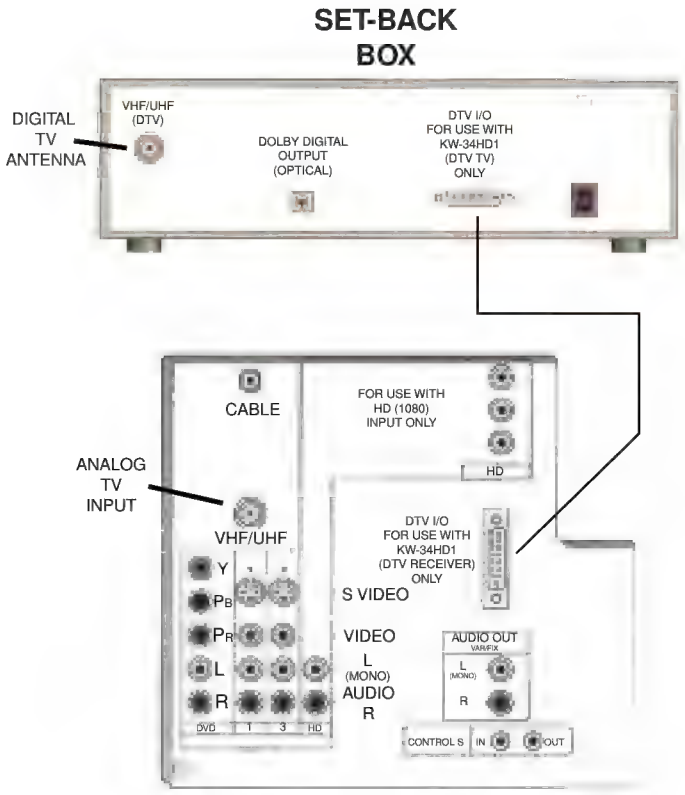
Video can be made of four components:

- Luminance or Y which defines the brightness level and
- Color, which is made of three components, called R-Y, B-Y and G-Y.

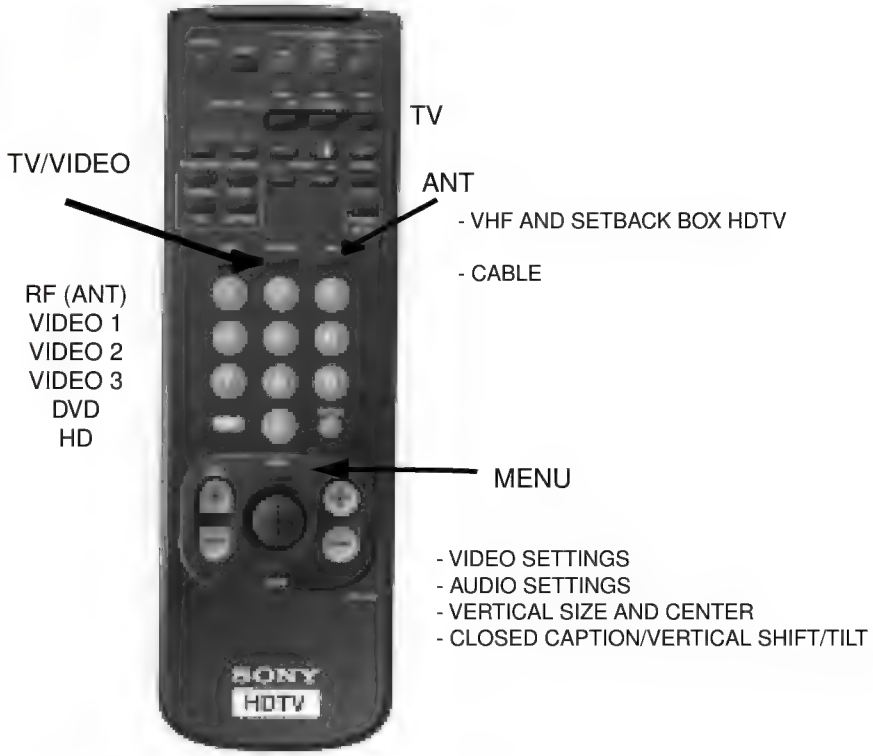
We can mathematically calculate the fourth component (G-Y) from the others so only three components are required for video:

Assuming R+B+G = Y, and (R-Y)+Y = R, then (G-Y) = -R-B.

The manufacture of the G-Y signal can be performed in an electric matrix consisting of summing op amps for adding (+) and subtractive op amps for the difference of the two signals (-). By adding the (inverted) signals, the last G-Y component can be derived.



REAR PANEL

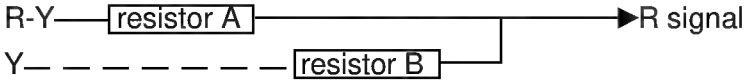


KW34HD1 REMOTE CONTROL

INPUTS

HDTV44

These simple matrixes are found in ICs frequently labeled as decoders or are part of a processor. A video processor IC can contain an additional simple electric matrix to convert the R-Y signals to their base Red signal voltages by just adding the Y signal as (R-Y) + Y = R. The RGB signals output can be used to drive the CRT.



Identification

Component video is usually carried on three lines: Y, R-Y, & B-Y. They can also abbreviated differently, but are the same:

- Y, U, V
- Y, Cr, Cb
- Y, Pr, Pb
- Y, R-Y, & B-Y.

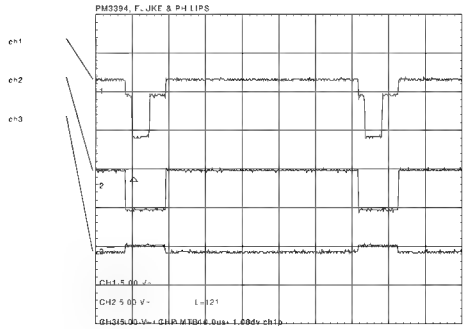
The Y, Pr, Pb version designates the progressive instead of interlaced picture scan format. This TV selects the DVD or HD component video input from the TV/Video remote button. However, the HD signal must have a horizontal frequency of 31 to 34kHz or the screen will remain dark with just an "HD" OSD.

Waveforms

The following is a scope shot of component video signals that makes up a blue screen picture. In the top waveform is the Y signal. It houses the horizontal sync pulses (the vertical is not seen at this time base, but it is present in the Y signal). The line between the sync pulses represents the brightness level. The higher the line, the brighter the picture. Therefore, a voltage at the sync pulse level is black.

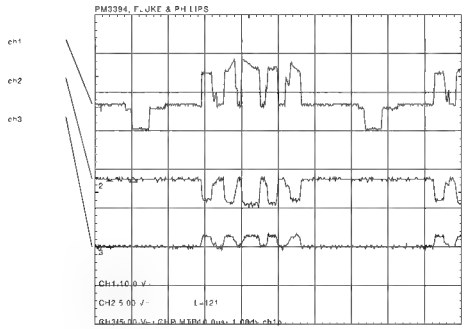
The middle waveform is the B-Y signal. The area corresponding to the horizontal sync pulse in the Y signal is at 0Vdc. The remainder of the voltage minus the Y level is the Blue color level. Since this is a picture of a blue screen, the voltage is high.

The bottom waveform is the R-Y signal. The area corresponding to the horizontal sync pulse in the Y signal is also at 0Vdc. The red - Y level during a blue screen is below 0Vdc. It will be equal to 0Vdc if the Y signal is subtracted.

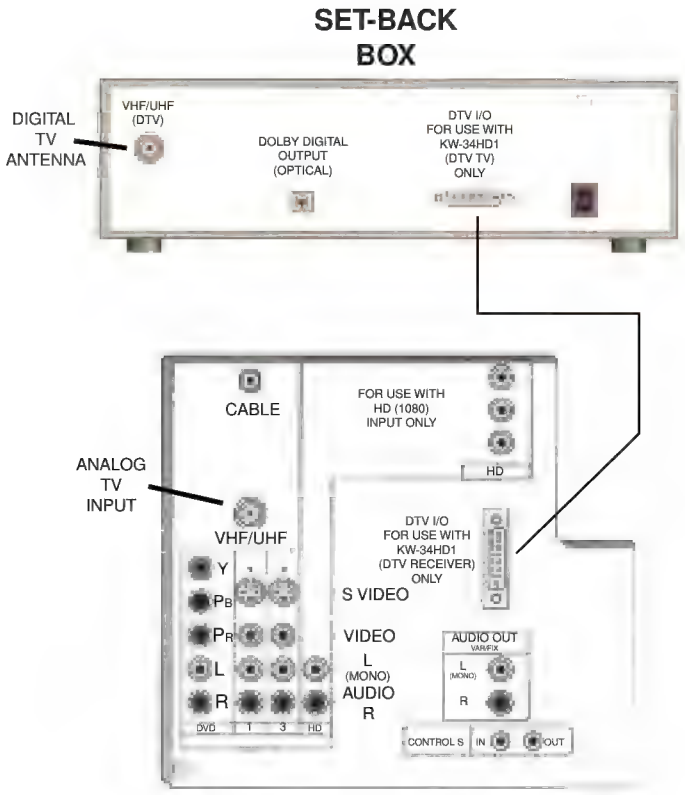


Blue screen – waveform YUV			
	Name	Location	Voltage/div
Channel 1	Y	DVD output	7.5Vp-p
Channel 2	B-Y	DVD output	5Vp-p
Channel 3	R-Y	DVD output	1Vp-p
Time base	10usec/div		

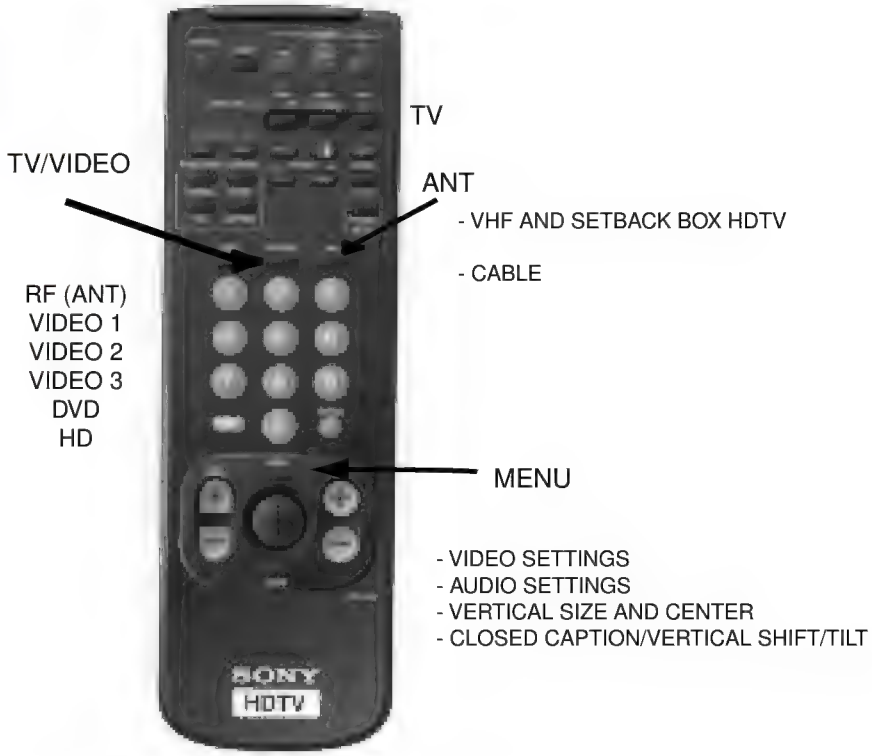
For comparison, the following component video waveforms are of a picture on a blue screen. The Y signal contains voltages of various brightness levels centered on the screen between the H. sync pulses. The B-Y and R-Y signals contain changing color levels in the middle of the screen. Note that by looking at either color signal without the Y signal level, it is not possible to know where the sync area is. It is therefore difficult for your scope to sync on the R-Y or B-Y signal alone without a reference.



Picture centered on Blue screen – waveform Ysig			
	Name	Location	Voltage/div
Channel 1	Y	DVD output	7.5Vp-p
Channel 2	B-Y	DVD output	5Vp-p
Channel 3	R-Y	DVD output	1Vp-p
Time base	10usec/div		



REAR PANEL



KW34HD1 REMOTE CONTROL

INPUTS

HDTV44

Overall Block

There are three main sections in Sony's model KW34HD1 first generation High Definition Television (HDTV):

1. Video Processing
2. Deflection
3. Power Supply

The additional circuit blocks in each section and the external box needed to receive the off the air UHF, HDTV signals distinguish this High Definition TV from a conventional TV.

Video Processing

Because no one HDTV standard has been determined, this first generation HDTV has the flexibility to accept any of the following inputs:

Sony model KW34HD1 inputs		
Input	Block Location	Signal format
VHF/UHF antenna Digital channels 1-99	HDTV external box	RF
VHF/UHF antenna Analog channels 2-69	Main & Sub Tuners via antenna switch	RF
Cable Channels 1-125	Main & Sub Tuners via antenna switch	RF
Video 1 – 3 Phono jacks	Video Selector Sw	Composite video; L & R channel audio.
DVD Phono jacks	DVD Switch	Y, Pb, Pr L & R channel audio
HD Phono jacks	Video Processor	Y, Pb, Pr L & R channel audio

The signal path for these inputs is shown below:

Digital Input

VHF/UHF antenna

HDTV Box (accepts all 18 DTV formats)

Video Processor Þ DTV Sw (twin view or SD picture)
ß MID (stores both twin pictures)
RGB Driver Sel (selects twin pix path)

CRT cathode Video processor Þ RGB Driver Þ CRT

VHF/UHF /Cable Analog Reception

Air or cable selection by the Main Micro is performed at the input antenna switch (SW). Thereafter the signal path is the same.

VHF/UHF antenna or cable

Input antenna switch (SW)

Main/sub tuners

Video selector

DVD switch

DTV switch

DRC

SEL

Video processor

RGB Driver

CRT cathodes

Video Inputs 1 – 3

Composite video from a VCR or satellite (DSB) receiver

Video selector

DVD switch

DTV switch

DRC

SEL

Video processor

RGB Driver

CRT cathodes

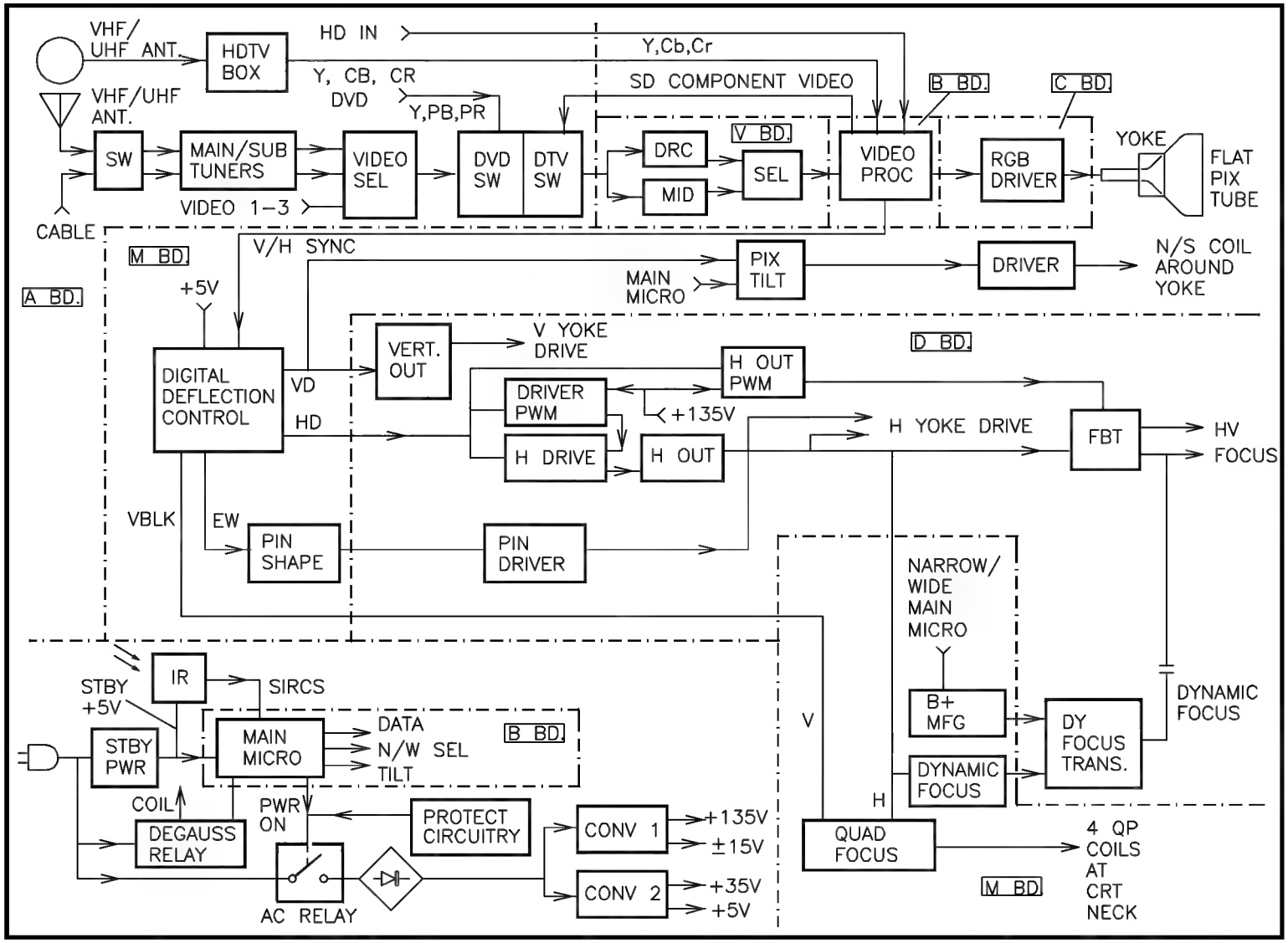
DVD Input

DVD switch

DTV switch

DRC

SEL



OVERALL BLOCK

HDTV36 1062 3 10 99

Video processor

RGB Driver

CRT cathodes

HD Input

This input is for an external HDTV (perhaps cable) box that receives and decodes the HDTV to output component video: Y, R-Y, B-Y (also called Y, Pb, Pr or Y, Cb, Cr, or Y, U, V, depending upon where you are in the world). The component video path introduces the component video directly into the video processor block. The scan width of this picture is a function of the horizontal frequency.

Video processor

RGB Driver

CRT cathodes

Deflection

The deflection control IC develops signals for:

- Vertical and horizontal deflection (VD & HD)
- Horizontal pincushion (EW)
- Picture tilt & horizontal trapezoid correction (VD)
- Focus (V blk)

Vertical and horizontal deflection

The vertical stage is conventional, but the horizontal stage is not. Both the horizontal driver and output stages have individual PWM stages that supply regulated B+ voltage to them. The H. output B+ comes from the PWM stage through the flyback.

Horizontal Pincushion

The horizontal pincushion correction stage compensates for a picture that is bent inward at the middle of the screen. The E/W correction signal from the deflection controller is amplified and applied to the yoke at the horizontal output transistor's collector to correct for insufficient scan.

Picture tilt and horizontal trapezoid correction

Vertical drive (VD) signals not only feed the vertical deflection stage, but also the picture tilt stage that handles trapezoid correction. A controlled level of vertical sawtooth (VD) signal is used for trapezoid correction. This correction signal is mixed with a DC voltage for tilt correction and applied to the N/S coil suspended about the bell of the picture tube by the yoke.

Focus

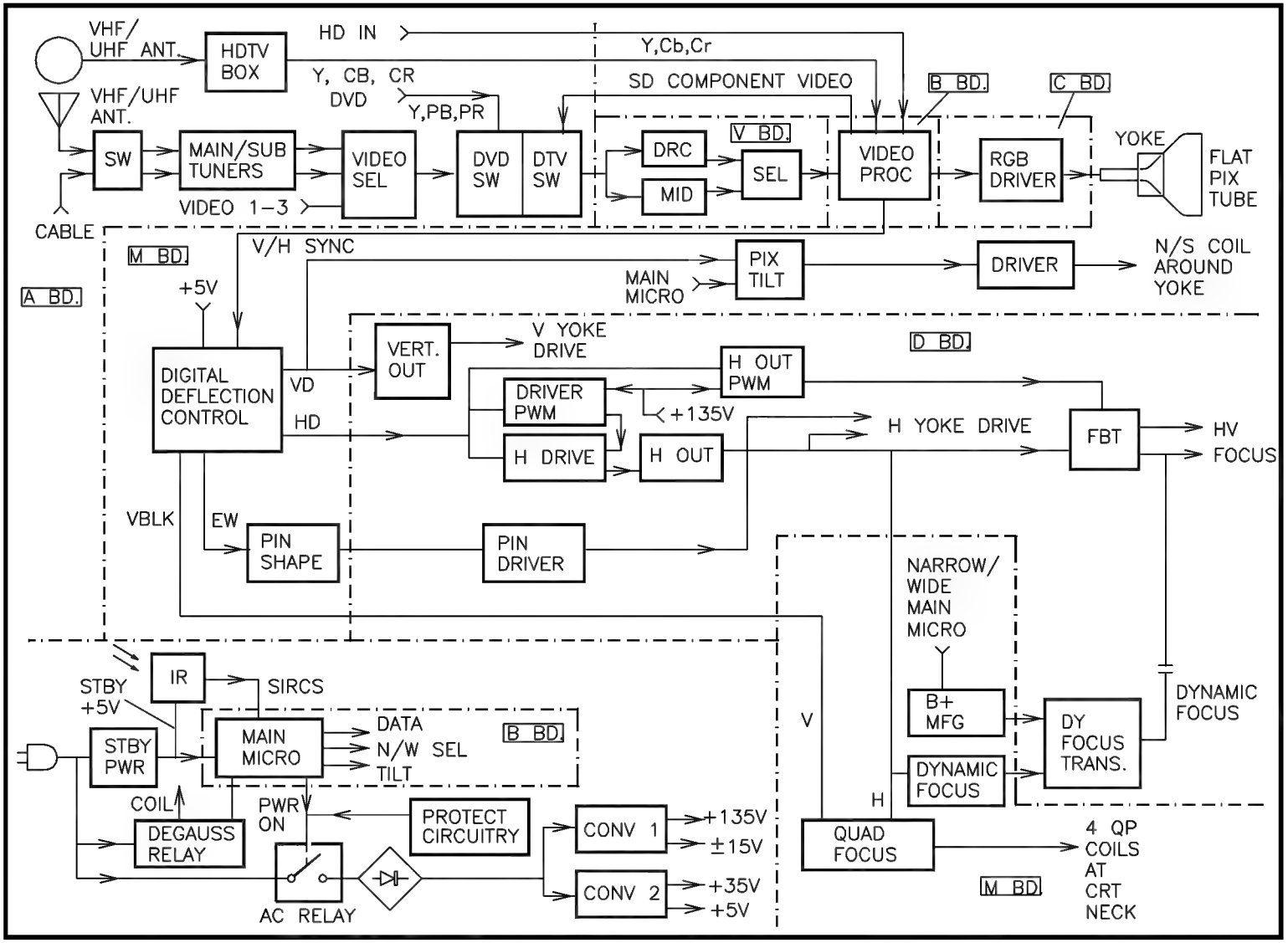
There are two focus circuits used in this TV. The dynamic focus circuit uses horizontal pulses to correct the left and right side picture focus caused by the flat screen. The dynamic correction voltage is added into the static (DC) focus voltage that is applied to the picture tube.

The quad focus circuit uses both H & V signals to correct spot shape at the four corners of the screen. The circuit's correction voltage is output to four "QP" coils mounted on a board surrounding the picture tube's electron gun.

Power Supply

The power supply consists of:

- A small 60Hz standby power supply that supplies standby +5V to the Main Micro.
- A Main Micro IC that controls the power relay as well as the deflection, video, and audio stages.
- A degaussing circuit.
- Two almost identical converter stages. Converter 2 turns on converter 1. Different voltages are output from each converter to power the TV.
- A protection circuit to detect excessive voltage and excessive current in various parts of the TV. The protect circuit also monitors vertical drive. A failure in the detected areas causes the power ON command to be removed from AC relay.



OVERALL BLOCK

HDTV36 1062 3 10 99

Video Block 1

Input Formats

This direct view 34" model KW34HD1 High Definition TV can accept various formats and present them in a single or double Twin View Ò picture. To perform this, each input signal must be processed into a common format, then selected for viewing. The inputs are:

Sony Model KW34HD1 Inputs		
Input	Format	Processing
NTSC analog VHF/UHF channels 2-69	RF	Demodulation into video. Video into Y & C. Y & C into component video (Y, Cb, Cr.) Component video into RGB
Cable (analog) channels 1-125	RF	Same as above except different RF frequencies are received.
Video 1 – 3	Composite video L & R audio	Video into Y & C. Y & C into component video (Y, Cb, Cr.) Component video into RGB
DVD	Component video L & R audio	Component video into RGB.
HD	Same as above	Component video into RGB

Signal Flow

RF Input

The RF signals input to the main and sub tuners are channel selected and RF demodulated into composite video. The composite video from the tuner is applied to the video Switch IC2006 along with composite videos 1-3 from the rear and front panel for user selection.

Video Inputs

Video Switch IC2006 selects the video for the main and sub pictures. It also sends the video through comb filters. The comb filters separate the composite video into their luminance (Y) and chroma (C) parts.

The main and sub (Y & C) outputs run parallel paths through similar ICs before leaving the A board. The main and sub signals are converted to component video in Chroma Decoders IC2403 (sub path) and IC2404 (main path). The Y, R-y, B-Y signals are applied to switches IC2405 and IC2406 to enable DVD input selection.

DVD Input

Switches IC2405 and IC2406 can now select between the processed composite video signal and the rear panel DVD input. The DVD signal must also be applied to the sub input line so that it can appear as the second or sub picture in the Twin View mode. Whatever is input on the main picture path is duplicated in the sub path. Switch selection is performed using serial data from the Main Micro IC3251 (not shown). The switched signal is applied to the next switch in both signal paths.

DTV Input

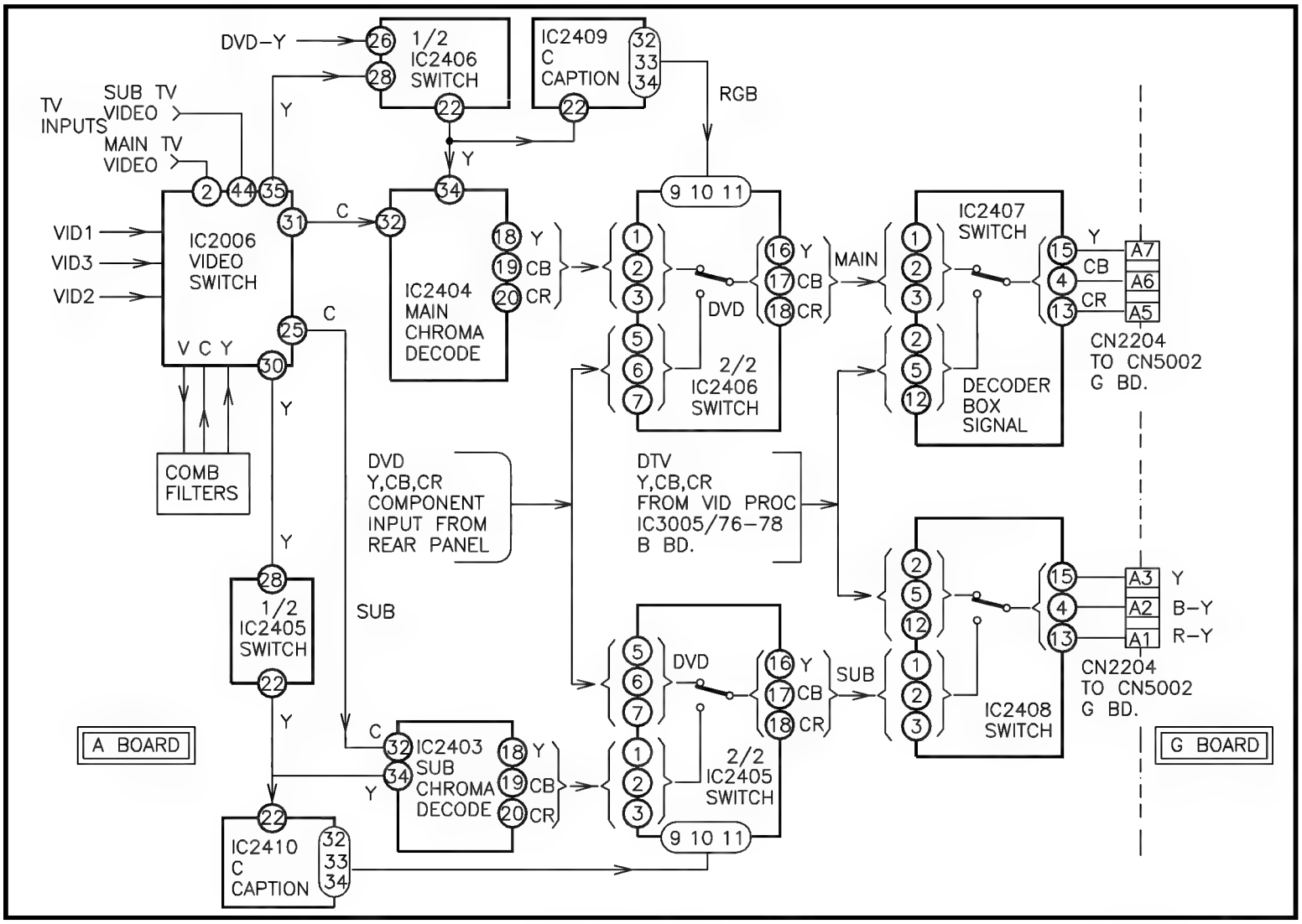
Switches IC2407 and IC2408 introduce the digital TV from the external setback box. This DTV signal path is used when:

- Viewing the HD or SD Digital TV signal as a sub picture (Twin View mode); or
- The DTV signal is of standard definition (525 lines/480 lines viewable) and line doubling is required.

When viewing just the single HDTV picture, the DTV signal is applied directly into the video processor IC3005 (Video Block 3) and does not come this way (except during Twin View).

A Board Output

The main and sub picture paths leave the A board and are passed through the G board into the digital processing stages on the V board. This signal routing through the G board is necessary because both the vertical A and V boards plug into the horizontal G board.



VIDEO BLOCK 1

HDTV6 1009 3 10 99

Video Process A

The external video input from the rear panel and internal video from both main and sub tuners is applied to this stage for selection and conversion to (Y, R-y, B-y) component video. The major parts in this early video processing are listed below:

Major Video Processing Components Shown			
Name	Input	Output	Purpose
Video Switch IC2006	2 tuners, 3 video inputs Y & C from 2 comb filters	Main Y & C Sub Y & C (similar processing not shown)	Selects composite video Routes to comb filter
Buffers Q2016, Q2420, Q2422.	1Vp-p of Y from IC2006/pin 35	1Vp-p of Y to IC2406/pin 28	Y buffers
YUV Switch ½ IC2406	1Vp-p of Y at IC2406/pin 28	2Vp-p at pin 22	6db amp
Buffers Q2015, Q2421	1Vp-p of C from IC2006/pin 31	1Vp-p of C to IC2404/pin 32	C buffers
Chroma Decoder IC2404	Main Y & C at pins 34 and 32 Y=2Vp-p, C=1Vp-p	Y = 1Vp-p; Cr, Cb = 0.5Vp-p @ pins 18-20	Changes Y/C to component video

All signal levels were taken using a color bar input.

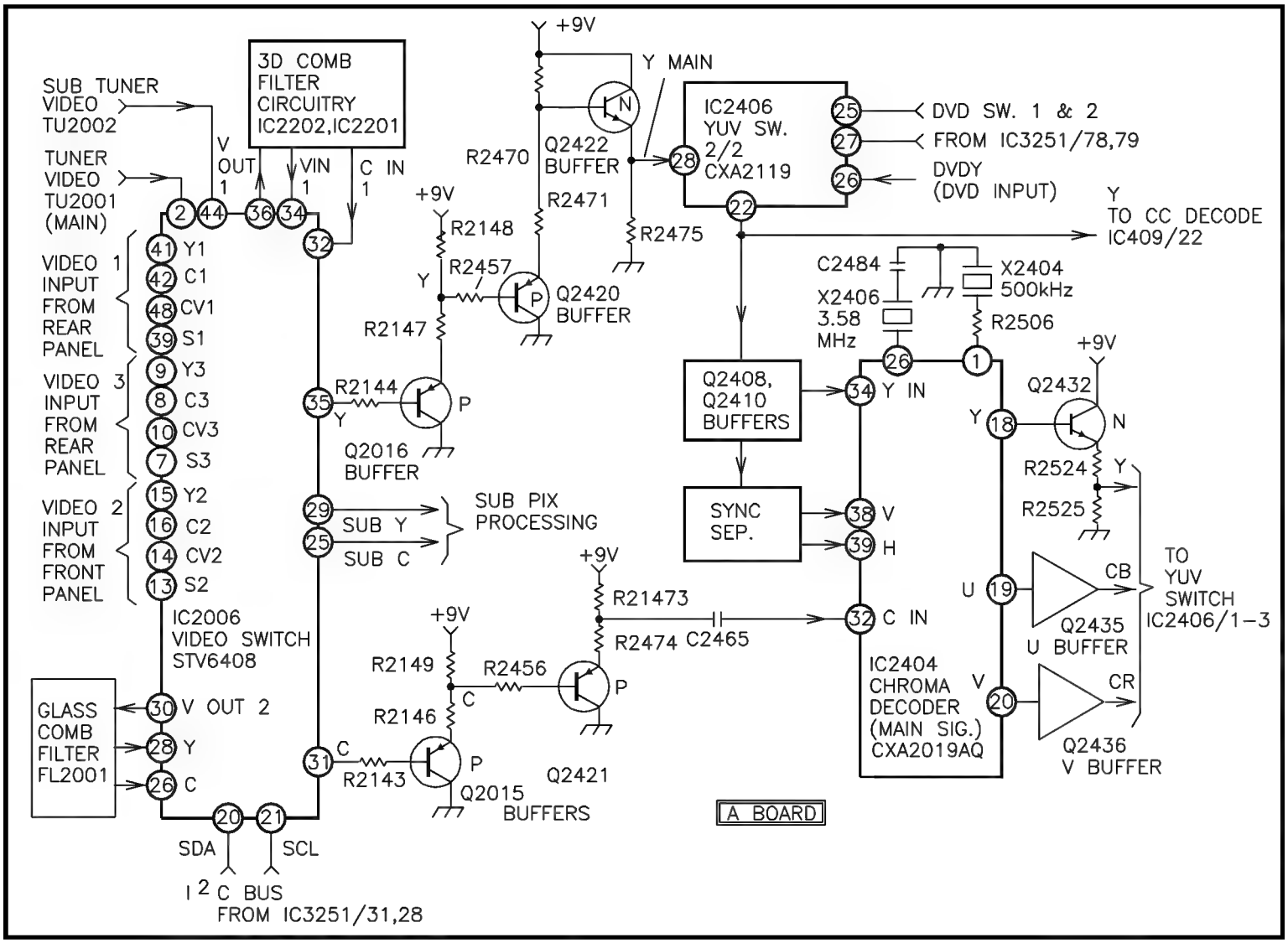
Video Switch

Five composite video inputs are applied to video switch IC2006. Serial data from Main Micro IC3251 (not shown) chooses which input signals take the main and sub picture signal paths. The chosen signals go to their respective comb filters. The 3D filter is always kept in the main picture path and the glass filter (FL2001) is used in the sub picture path.

The Y & C outputs from both comb filters are returned to IC2006 and output again. The main picture path is from pins 31 and 35. The sub video path is from switch IC2006/pins 25 and 30 and runs a parallel route to the main one (Video Block 1) for identical processing.

Component Video

Then the Y signal is input the Chroma Decoder. The chroma (C) signal is also buffered and input to Chroma Decoder IC2404/pin 32. IC2404 uses both the Y & C inputs for level conversion to Y, Cr, Cb (component video).



VIDEO CIRCUIT A

HDTV1 1011 3 9 99

Video Process B

Signal Flow

Input Selection

Main component video from the Chroma Decoder IC2406 is only one input into switch IC2406. The second input to IC2406 is DVD component video from the rear panel phono jacks.

The Main Micro IC3251/pin 78 and 79 sends logic level voltages into IC2406/ pins 25 and 4/27 for the input selection. The chart shows the switching voltages for selecting an input:

IC2406 Selection		
Input selected	IC2406/pin 25	IC2406/pins 4, 27
Main (RF, video)	L	H
DVD	H	L

Closed Caption

The luminance passes through switch IC2406, which adds closed caption or XDS station information as an OSD. If the user requests this feature, this caption information enters IC2406 as an RGB signal from IC2409. The take off or input signal for the closed caption decoder IC2409 is at the output of this YUV switch at IC2406/pin 22.

Filtering

When high frequency analog signals are sent into a digital stage, the high frequency component can create a secondary signal. This second signal is called an alias component. Alias signals are eliminated by low pass filtering (LPF) the analog input. That is the purpose of the filter networks at the output of IC2406.

DTV Selection

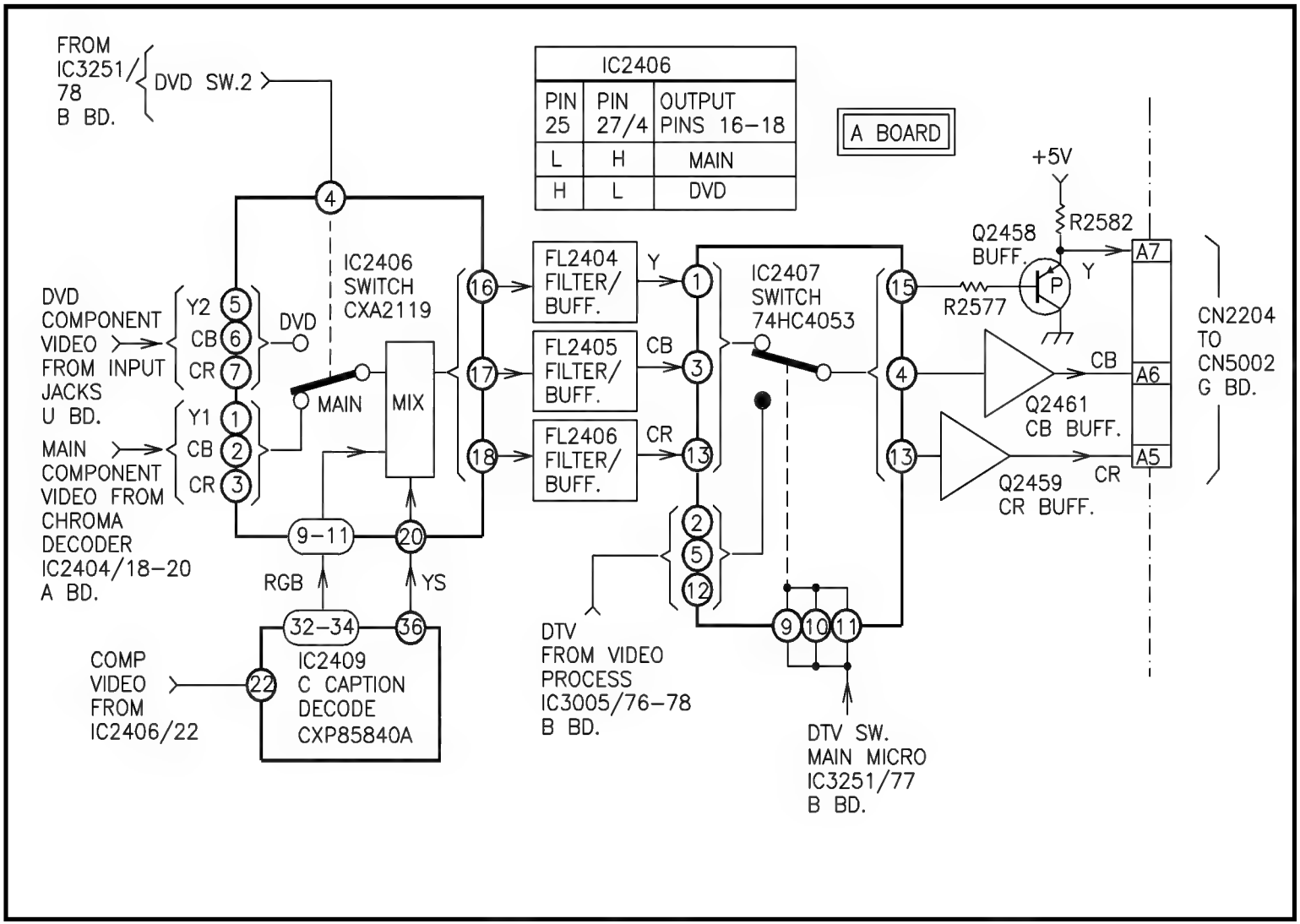
Switch IC2407 chooses between the main and DTV signal for the main picture path. The DTV signal is chosen only when:

- Viewing the HD or SD Digital TV signal as a sub picture (Twin View mode) or
- The DTV signal is of standard definition (525 lines/480 lines viewable) and line doubling is required.

The DTV path is chosen when IC2407/pin 9-11 is low:

IC2407 Selection	
Input selected	Sw signal IC2407/pin 9, 10, 11
Main (RF, video)	H
DTV	L

The output of the DTV/Main switch IC2407 is buffered and sent through the G board to the V board for digital processing.



VIDEO PROCESS B

HDTV2 1013 3 9 99

Video Block 2

Overview

The V board is fully shielded and contains the digital signal processing. The V board is sandwiched in-between the analog A and B boards. All three of these boards plug into the horizontal G board. The V board has the following inputs and outputs:

V Board Signal Processing		
Input (Y, Cr, Cb)	Output (Y, Cr, Cb)	Purpose
Main Signal CN503/pins 7, 9, 11	DRC processed main picture or MID IC506 processed twin view picture.	Simulates a 960-line picture from an active 480 line NTSC input signal. Selects one (main) or two simultaneous (Twin View) pictures.
Sub Signal CN503/pins 1, 3, 5		

Signal Flow

The main picture signal is applied to both the DRC and MID digital circuitry for processing:

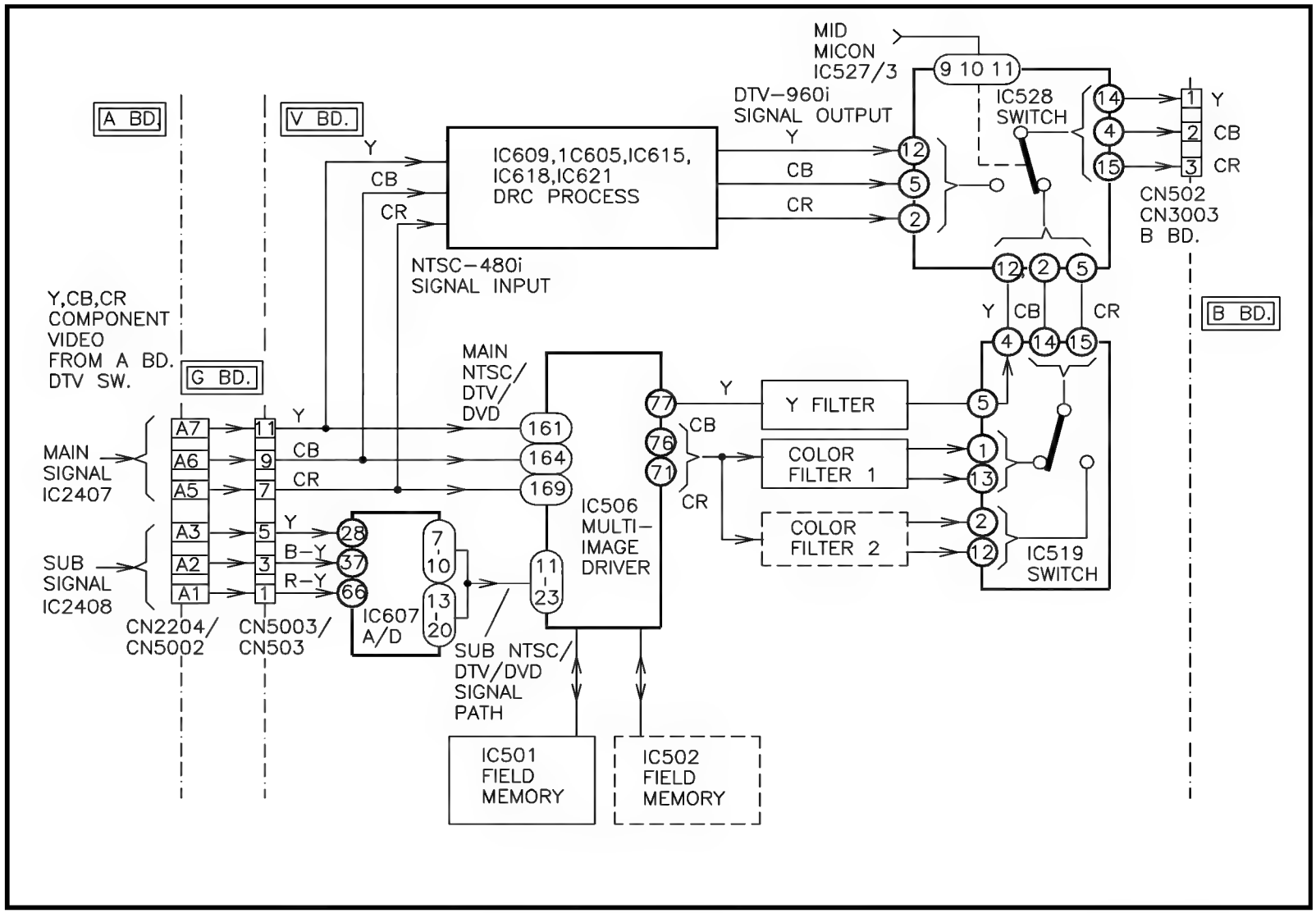
Digital Circuitry	
Name	Purpose
DRC – Digital Reality Creation	Doubles scanning lines and pixels after massive present and previous line information analysis.
MID – Multi Image Driver	Accepts both 480-or/and 960-line component video images (main/sub) and converts them into a twin picture.

The DRC digital circuitry does more than just double the lines, though that is the primary objective. There are 525 NTSC interlaced lines input (480 viewable lines) to the DRC and 960i (i = interlaced) lines leaving. It is the manner in which the extra lines are created that makes the DRC circuit unique. DRC and MID concept explanations are in the pages that follow.

The main picture signal is input to the MID IC directly. The sub picture signal is converted to a digital signal by A/D Converter IC607 before becoming the other input for the MID IC.

The MID digital circuitry reduces this sub and the main picture to fit on the screen at the same time. This coexistence feature is called Twin View. The analog output of the MID IC is low pass filtered by filter 1 to reduce D/A converter noise. Filter 2 is selected in the Japanese version of this TV set when there is a computer signal input to that version. In the USA TV, IC519 is never toggled from the position shown.

Either the main or the Twin View picture is selected by IC528 and this resultant signal is sent to the next (B) board.



VIDEO BLOCK 2

HDTV7 1008 3 9 99

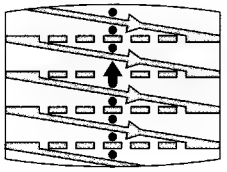
DRC - Digital Reality Creation

Another picture quality issue has been with us since the dawn of television. Deeply ingrained in our television system is the question of visible scanning lines.

All about scanning lines

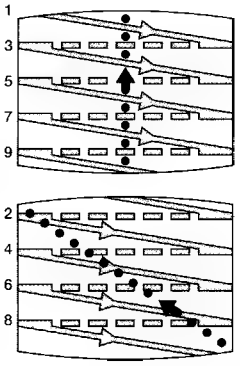
A television picture is "painted" across the CRT screen by an electron beam that scans on a horizontal line from left to right. Once the beam reaches the ridge edge, it shuts off and returns to the left edge to start another line. All told, there are some 525 scanning lines in the American NTSC (National Television Standards Committee) television system, and they create a new television picture or "frame" some 30 times a second.

The TV picture is "painted" on the CRT screen by an electron beam that scans in horizontal lines.



In reality, you don't see the full 525 lines on the screen. Over 40 lines are consumed by the Vertical Blanking interval. This leaves roughly 480 lines for the actual picture. And you don't even see the 480 lines all at once. Each video frame is divided into two "fields", which last for 1/60th of a second. The first field is composed of all the odd-numbered lines (1, 3, 5 and so on). The second field "fills in" with the even-numbered lines. This technique of alternating odd and even fields is called "interlacing." The NTSC system is often referred to as "525/60" (for 525 total scanning lines and 60 fields per second). It is also called "480I" (for 480 net scanning lines, interlaced).

The first field displays the 240 odd-numbered lines. The next field displays the 240 even-numbered lines.



Over the years, the 480i system has worked remarkably well. But with only 240 lines on-screen at any one time, the scanning lines can become painfully obvious, particularly when you're sitting close to a large-screen display.

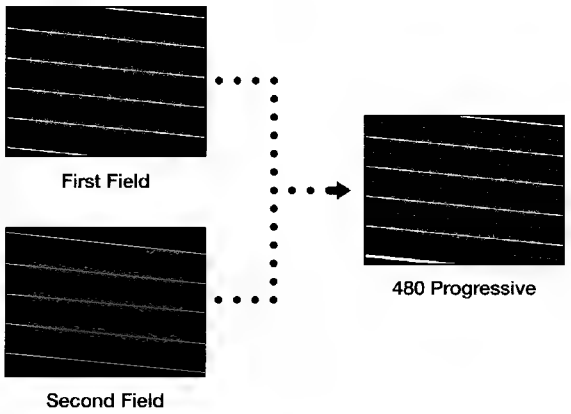
Problem: Visual scanning lines

Originally, television engineers designed the NTSC system so that the picture would appear seamless when viewed from a distance of 8 times the picture height. This worked well in an era when the biggest commercially available screens were 12 inches diagonal. But in today's big-screen era, viewers tend to set far closer to their televisions in order to get wrapped up in the action. Under these conditions, the scanning lines become blatantly visible.

One solution: Line doublers

Demanding home theater enthusiasts, videophiles and video professionals have long sought a cure for this problem. One solution is to double the number of scanning lines with a circuit called a line doubler. Sony has been an active supplier of line doublers, particularly for professional video projectors.

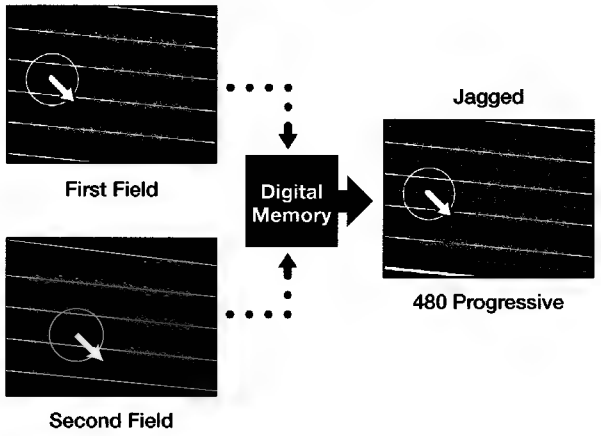
Line doublers attempt to de-interlace the signal, converting an interlaced "480i" signal into a progressive-scan "480P."



Many line doublers attempt to de-interlace the 480i NTSC signal, displaying both fields simultaneously in a 480-line "progressive" scan. Progressive scanning combines the separate fields of odd-numbered lines and even-numbered lines. Progressive scanning displays every line in a frame in numeric sequence – line 1, 2, 3, 4 and so on up to line 480. Progressive scan plays a central role in computer displays – where it helps to make text more legible. Line doublers turn interlaced 480i signals into a progressive 480P.

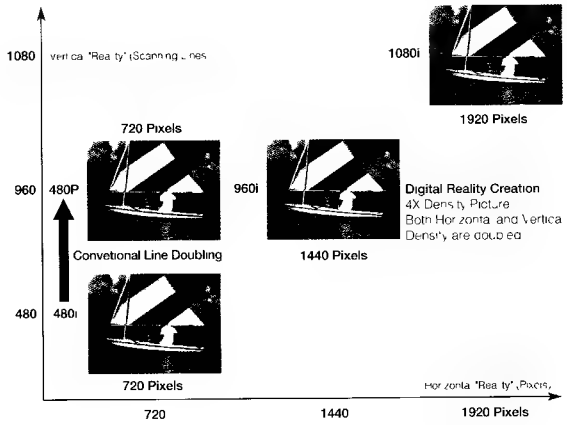
This concept works perfectly for still images, because the two fields match up completely. But on moving images, the even field is captured 1/60th second *later* than the odd field. So a car traveling on the screen has driven 1/60th second further down the street. And a baseball has slid 1/60th second closer to home plate. For this reason, line-doublers require elaborate motion-detection, motion-compensation and memory circuits. This can get expensive, with the better line doublers costing $2,500 or more.

Line doublers are challenged when there's motion in the video scene. They require motion compensation.



A new solution: DRC

Sony's new Digital Reality Creation (DRC) circuitry is an all-new approach to the problem of visible scanning lines. Not only does DRC create a clearer picture by doubling the number of active scanning lines – *it also doubles the number of pixels on each scanning line.* You get four times the picture density of standard 480i, making this a significant step toward the picture quality of true High Definition TV (HDTV).

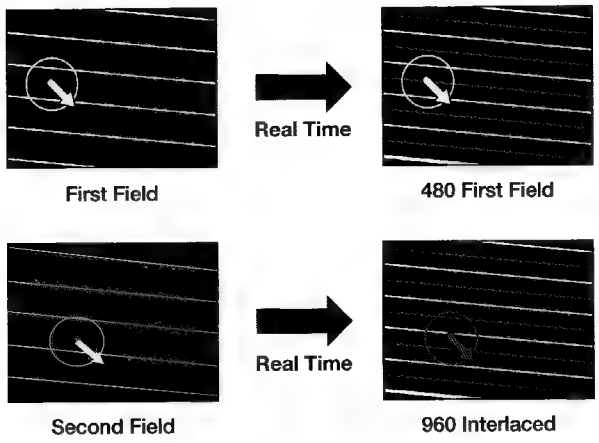


Sony's Digital Reality Creation circuitry moves the standard 480i picture a significant step toward High Definition 1080i.

How it works

The new DRC circuit is based upon a massive analysis of over tens of thousands of High Definition TV picture patterns. Because there is a fixed relationship between NTSC patterns and their HDTV equivalents, Sony's exclusive microprocessor can simply *replace* the NTSC signal with its correct DRC counterpart. In operation, the DRC circuit accepts a digitally sampled 13.5 M H z input and generates a quadrupled 54.0 MHz digital output.

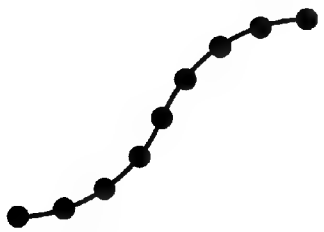
Moreover, with DRC, each field is processed separately, so there's never a need to compensate for motion between two fields. And while the doublers typically produce a scan of 480P, the DRC circuit produces a higher line rate, 960i, for even greater image density.



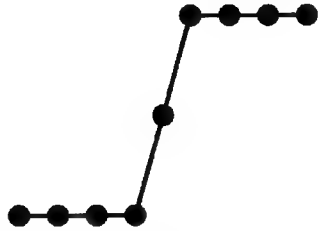
Line doubling (left) requires memory to avoid artifacts on moving objects. Digital Reality Creation circuitry (right) maintains the integrity of each video field.

What it all means

Digital Reality Creation circuitry greatly enhances the television viewing experience. Now you can sit up close to the screen, immersing yourself in the magic of home entertainment – and still not be bothered by visible scanning lines. Pictures appear denser and more seamless. And in the coming world of Digital TV (DTV) broadcasting, televisions with Digital Realty Creation circuitry will narrow the perceived gap among NTSC analog sources, standard definition digital and full High Definition digital video.



Line doubling improves vertical density



DRC doubles both vertical and horizontal density

NOTES

MID - Multi Image Driver

The world of NTSC has been a simple world. The 480i video cameras give their signals to 480i video recorders, 480i production switchers, 480i broadcasting, 480i videocassettes, 480i videodiscs and ultimately 480i home television receivers. This world is comfortable and compatible, but it's already rapidly changing.

A blossoming range of image standards

Unlike entertainment-oriented television, computers have long used progressive scanning to maximize the legibility of on-screen text. For example, the popular VGA computer standard uses progressive scanning 640 h x 480 V pixels. In video terms, that's 480P.

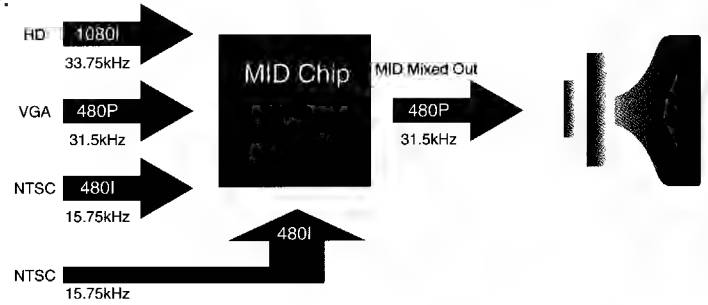
Digital Television (DTV) broadcasting embraces both interlace scanning and progressive scanning. A convergence technology is needed to link the two previously separate worlds of entertainment and information.

Sony's solution

Sony's new Multi-Image Driver (MID) circuitry contains a special "Twin-View" function that can display either a High Definition or a Standard Definition video signal together with any VGA source. This is a proprietary integrated circuit based on company expertise in broadcast-quality Digital Multi Effects systems. Some (but not all) Sony televisions with MID will enable viewers to combine two different signal formats on the same screen. MID works by converting both signals to VGA (480P) display. Supported signal combinations include:

- NTSC + NTSC
- NTSC + HD
- VGA + NTSC
- VGA + HD

In the digital future, the unique capabilities of the Multi-Image Driver circuitry will open up unprecedented applications. You'll use Picture-in-Picture with High Definition, standard definition and NTSC sources. You'll be able to watch a movie in High Definition, while you visit a website to learn more about how that movie was produced. And you'll be able to see both images with exceptional quality and highly advanced Picture-in-Picture functionality.

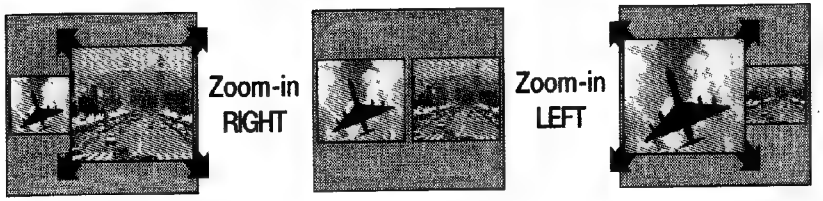


Sony's Multi-image Driver bridges the gap between computing and television. You can surf the net at VGA resolution while you watch High Definition TV on the same screen.

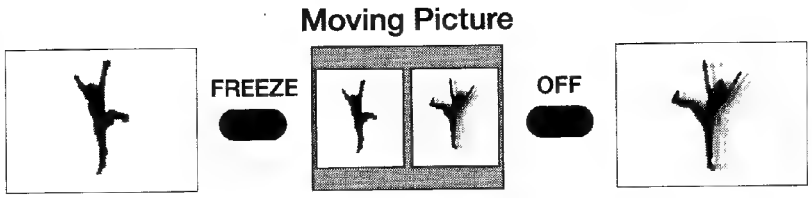
A new generation of PIP functionality

Multi-Image Driver circuitry also delivers powerful picture-in picture advantages, such as:

- **Flexible Twin-View™ Function.** Not only can you view two images side-by-side, but you can continuously expand either picture, up to two times its normal size.



- **New Favorite Channel.** Automatically shows your eight favorites or the last eight channels you've watched.
- **New Freeze Mode.** Lets you freeze a broadcast screen to write down a telephone number or website URL while the program continues as a side-by-side TwinView picture.



Video Process C

The V board is the second board (of four) in the video processing chain. Its purpose is to take the main component video and either reduce the number of scanning lines for a Twin View picture or double the number of lines for a picture that will simulate that of an HDTV picture. The signal path is dependent upon whether a single or twin picture is called for.

Single Picture

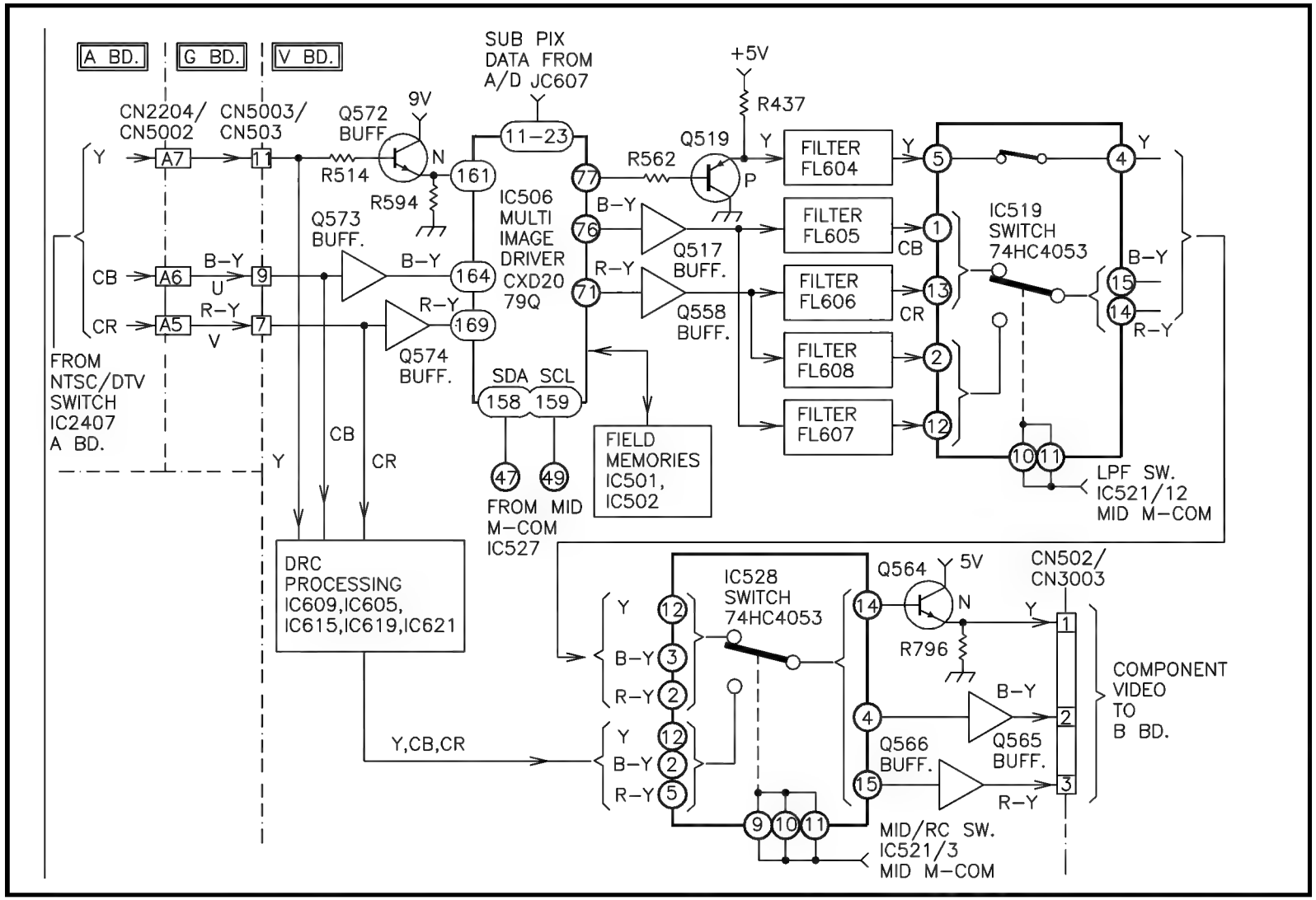
The single picture main signal path is through the Digital Reality Creation circuitry. The output is component video that is selected by switch IC528 to feed the Video Processor IC on the next (B) board.

Single Picture Main Signal Path			
Component	Input	Output	Purpose
DRC Processing	Main component video input CN503/pins 7, 9, 11.	Single (main) picture	lines doubled 480i to 960i lines
Switch IC528	Twin picture Single (main) picture	Component video	Selects single or double (twin) picture
Buffers Q564 – Q566	Component video	Component video	Current amplifiers

Twin View Picture

When Twin View is selected, the main picture path is through the MID IC. This IC uses two external memories (IC501 and IC502) to hold the information from each picture. When the information is needed, this can be selected at the right time to produce two pictures on the screen simultaneously. The second picture comes from the sub picture information input at IC506/pins 11-23.

Twin View Picture Main Signal Path			
Component	Input	Output	Purpose
Buffers transistors Q572-Q574	Main component video input CN503/pins 7, 9, 11.	IC509/pins: 77 (Y) = 2.3Vp-p 76 (Cb) = 1Vp-p 71 (Cr) = 1Vp-p	Supplies sufficient current to drive the next input stage.
Multi Image Driver IC506	Component video from: ♦ Main path - Buffer transistors. ♦ Sub Path – IC607	Combined main and sub picture in one component video output – pins 71, 76, 77.	Reduces main & sub picture size. Stores remaining info in external memories. Combines both pictures into one output (Twin View) picture.
Filters FL604-FL606	Twin View Component video	Twin View Component video	Reduces remaining digital noise.
Filters FL608 & FL607	Twin View Component color (Cr, Cb)	Twin View Component color (Cr, Cb)	Not used in USA model.
Switch IC519	Twin View Component video pins 1, 5, 13. Component color pins 2, 12.	Twin View Component video	Switch remains in the fixed position shown (USA model).
Switch IC528	Twin picture Single (main) picture	Component video. Y =.8Vp-p, Cr/Cb =.5Vp-p	Selects: single or double (twin) picture



VIDEO PROCESS C

HDTV3 1014 2 25 99

Video Block 3

Video Processor IC3005 Inputs

There are several inputs to the Video Processor IC3005. The most important inputs are:

- Two identical HDTV component video signals from the set-back box are input (# 4 and 5).
- The RF, DVD or Twin View video component video is input (# 1).
- OSD for menu or channel numbers (RGB) – OSD input.
- IK signal is returned from the CRT cathodes for RGB beam current balance.

The HDTV or main line video input is selected by serial data from the Main Micro (not shown). IC3005 converts the component video selected into RGB. After the video is converted to RGB format, the OSD information (also RGB format) is inserted.

The closed caption is usually introduced with the OSD signal at this point. However, in this set it is introduced earlier in the video chain (Video Process 1) so both twin pictures will have their own closed caption information.

Video Processor IC3005 Outputs

The signal outputs are:

- RGB video output signal is sent to the CRT cathodes (pins 35, 37 and 39)
- IK pulses that output the RGB signal lines are used to white balance the picture (pins 35, 37 and 39)
- DTV's component video signal (from the external set-back box) is returned to earlier stages (Video Block 1) for:
  - A twin View picture (pins 76-78); or
  - Line doubling if the setback box is receiving a DTV standard definition picture of 525 lines (480 lines viewable).

RGB Video

The RGB Video Processor signal outputs (pins 35, 37 and 39) are amplified and inverted by the three Video Output ICs IC9001-3. Then they are applied to the picture tube's cathodes to control electron intensity.

Automatic Cathode Balance (AKB) Circuit

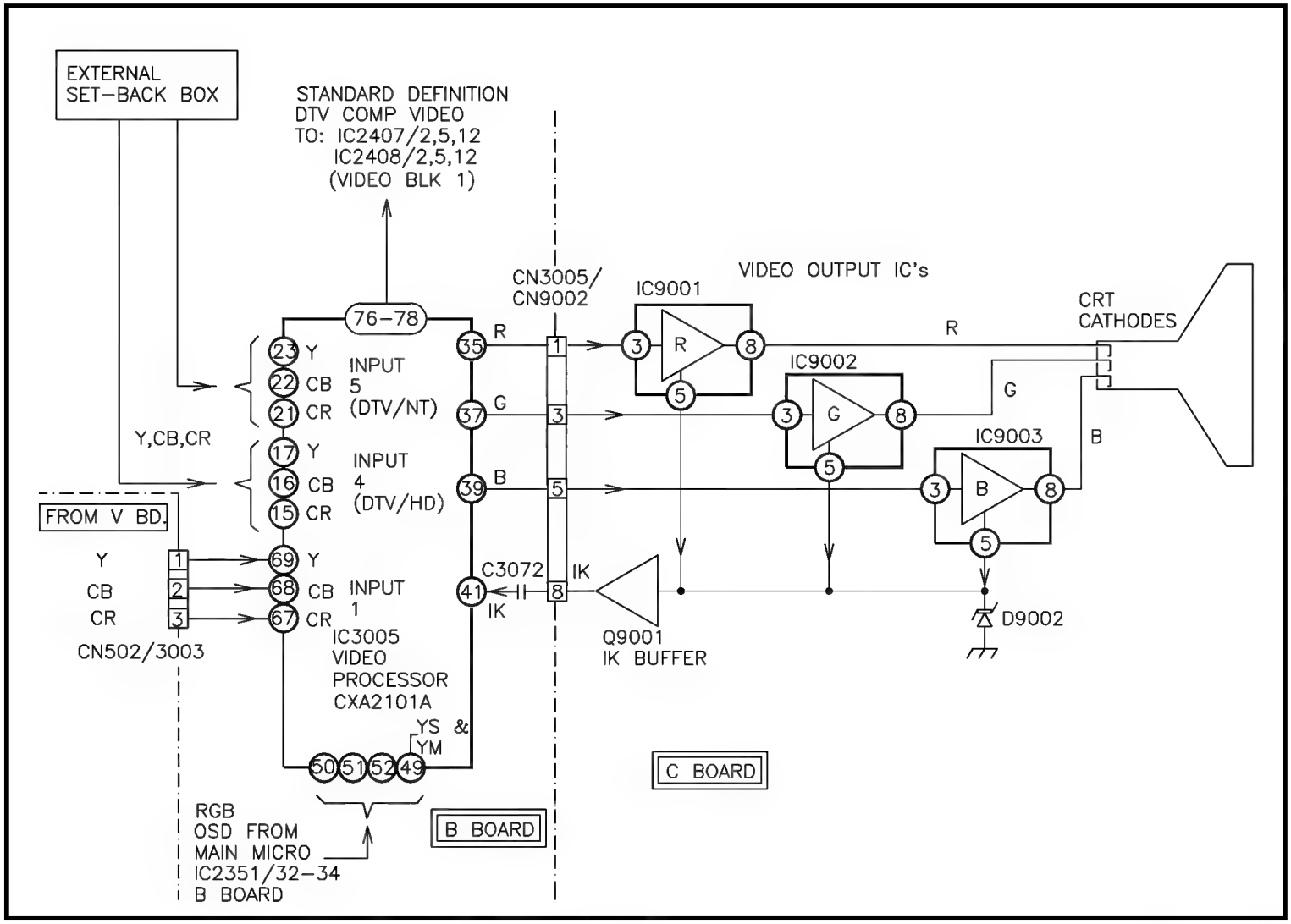
The purpose of the AKB circuit (also known as the IK circuit) is to adjust the level of the R, G or B drive signal to compensate for picture tube aging. The current drawn by the CRT cathodes is sampled and output pin 5 of each output IC. The outputs are multiplexed, buffered and AC coupled (C3072) to the Video Processor IC3005/pin 41 for analysis. The RGB levels are adjusted to compensate for a weak cathode.

The AKB circuit starts in IC3005 at turn on by outputting a one-line pulse to each cathode (from RGB, pins 35, 37 and 39). These three pulses occur on different lines and in the blanking area (above the picture) so they are never seen. The three drive pulses are output when the video processor IC3005 receives Vcc.

While the picture remains blanked, CRT drive current from these pulses produces a corresponding voltage pulse at pin 5 of each video output IC. The three pulses are combined and buffered. These pulses are called the AKB signal and their amplitudes represent the potency of each cathode.

The three pulses are returned to IC3005/pin 41 for analysis and drive signal adjustment. The drive output for example will be boosted to compensate for a reduced cathode output so the colors appear equal in performance. This is why this AKB circuit is commonly called a white balance circuit.

A loss in a picture tube cathode results in this AKB circuit's inability to balance. However, once the cathode emission is out of operating range, the AKB circuit will **not** blank the picture like previous AKB circuits. The front panel standby light will blink five times, pause and repeat, indicating a white balance adjustment failure. The standby light will blink with the TV on or off. The circuit is reset when the TV is unplugged, but the light will blink again if the problem persists.



VIDEO BLOCK 3

HDTV8 1007 3 9 99

Video Process D

The B board contains the Video Processor IC3005 and the Main Micro (not shown). The Main Micro controls the video processor, TV power and interfaces with the user. The Video Processor:

1. Selects component video to be input
2. Converts component video into RGB voltage for the picture tube
3. Monitors picture tube cathode current to adjust RGB drive level (IK, AKB, or white balance circuitry)
4. Adds on screen display (explained in another section)

The first two functions are part of the video processing. The third function is the automatic cathode balance circuit. It has changed dramatically in this set for ease of servicing. The fourth is for user information such as menus.

Video Processing

Several inputs are available for selection by the Video Processor IC3005. The selection is based upon serial data from the Main Micro IC3251/pins 28 and 31 into IC3005/pins 55-56. The inputs are outlined below:

IC3005 Input Selection	
Input	Operating Mode
DTV from set-back box at pins 13-23. Pins 13-17 contain identical information as pins 19-23.	Main Micro has instructed the set-back box to tune to a UHF channel and output that channel as component video (Y, R-Y, B-Y).
Single or Twin View picture information from the V board into pins 65-69	Either VHF TV, UHF TV, cable TV, Video, or DVD has been chosen from the remote control.
Rear panel HD (1080i) component video	HD is selected from the TV/Video remote control button.
OSD (see the OSD diagram)	When menu or display is pressed.

Once the input is chosen by IC3005, this video is internally matrixed into individual RGB levels. They output IC3005/pins 35, 37 and 39 for the picture tube (cathodes).

Automatic Cathode Balancing (AKB) Circuitry

The purpose of the AKB circuit (also known as the IK circuit) is to adjust the level of R, G or B drive signal to compensate for picture tube aging. The AKB circuit starts in IC3005 at turn on by outputting a one-line pulse to each cathode (from RGB pins 35, 37 and 39). These three pulses occur on different lines and in the blanking area (above the picture) so they are never seen. The three drive pulses are output as long as the video processor IC3005 receives Vcc (supply voltage).

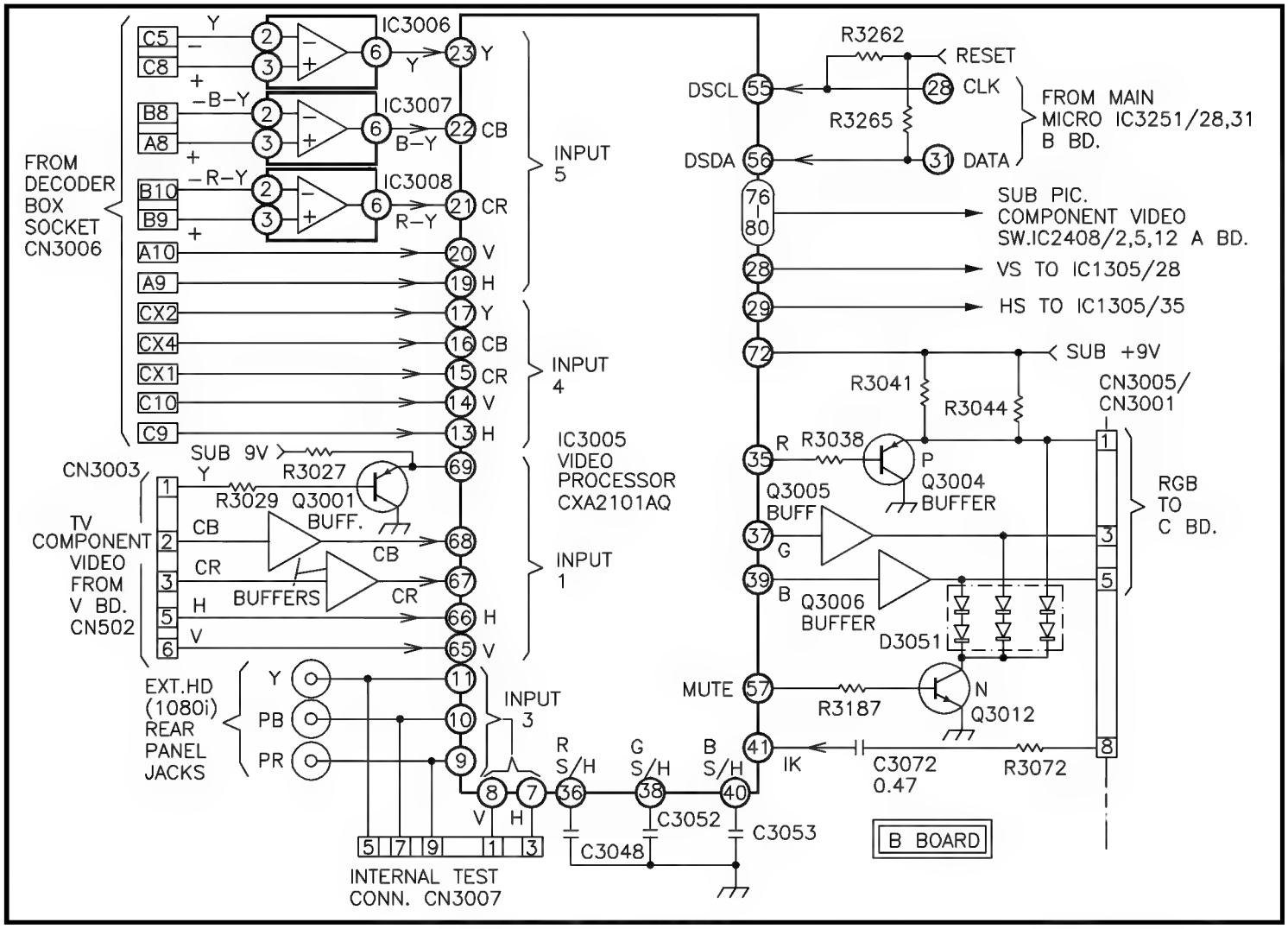
While the picture remains blanked, CRT drive current from these pulses produces a corresponding voltage pulse at each video output IC. Although these three AKB pulses are combined and buffered, their individual amplitudes represent the potency of each cathode.

The three pulses are returned to IC3005/pin 41 to charge their respective capacitors at pins 36, 38 and 40. The average charge is used for analysis and drive signal adjustment. For example, a drive output will be boosted to compensate for a reduced cathode output so the colors appear equal in performance. This is why this AKB circuit is commonly called a white balance circuit.

A picture tube cathode loss results in this circuit's inability to balance. However, once the cathode emission is out of operating range, the AKB circuit will **not** blank the picture like previous AKB circuits. The standby light will blink five times, pause and repeat, indicating a white balance adjustment failure. The standby light will blink with the TV on or off. The circuit is reset when the TV is unplugged, but the light will blink again if the problem persists.

The voltages measured at the three capacitors of this sample TV represent the efficacy of the cathodes. For example, when the red cathode is disabled, its capacitor voltage rises (see bold).

IK Capacitor Voltages		
IC3005/pin	Normal	R drive shorted CN9001/pin 1 = gnd
36. Red IK voltage	5.6V	**6.8V (abnormal)**
38. Green IK voltage	5.9V	4.8V
40. Blue IK voltage	5.6V	5.5V



VIDEO PROCESS D

HDTV4 1012 2 24 99

On Screen Display

OSD Components

The on screen display circuitry consist of the following major parts:

On Screen Display Parts			
Parts	Input	Output	Purpose
IC3251 Main Micro	Vertical sync – pin 95 Horizontal sync – pin 97 Remote control input – pin 7	R,G,B characters pulses from pins 32-34. Ys – Full blanking pulse Ym – ½ blanking mixing pulse	Generate character pulses. Generate character window pulse
IC3005 Video Processor	RGB character info – pins 50-52	R,G,B drive output to CRT cathodes	Mix or replace active video with characters.

OSD Operation

Character Manufacture

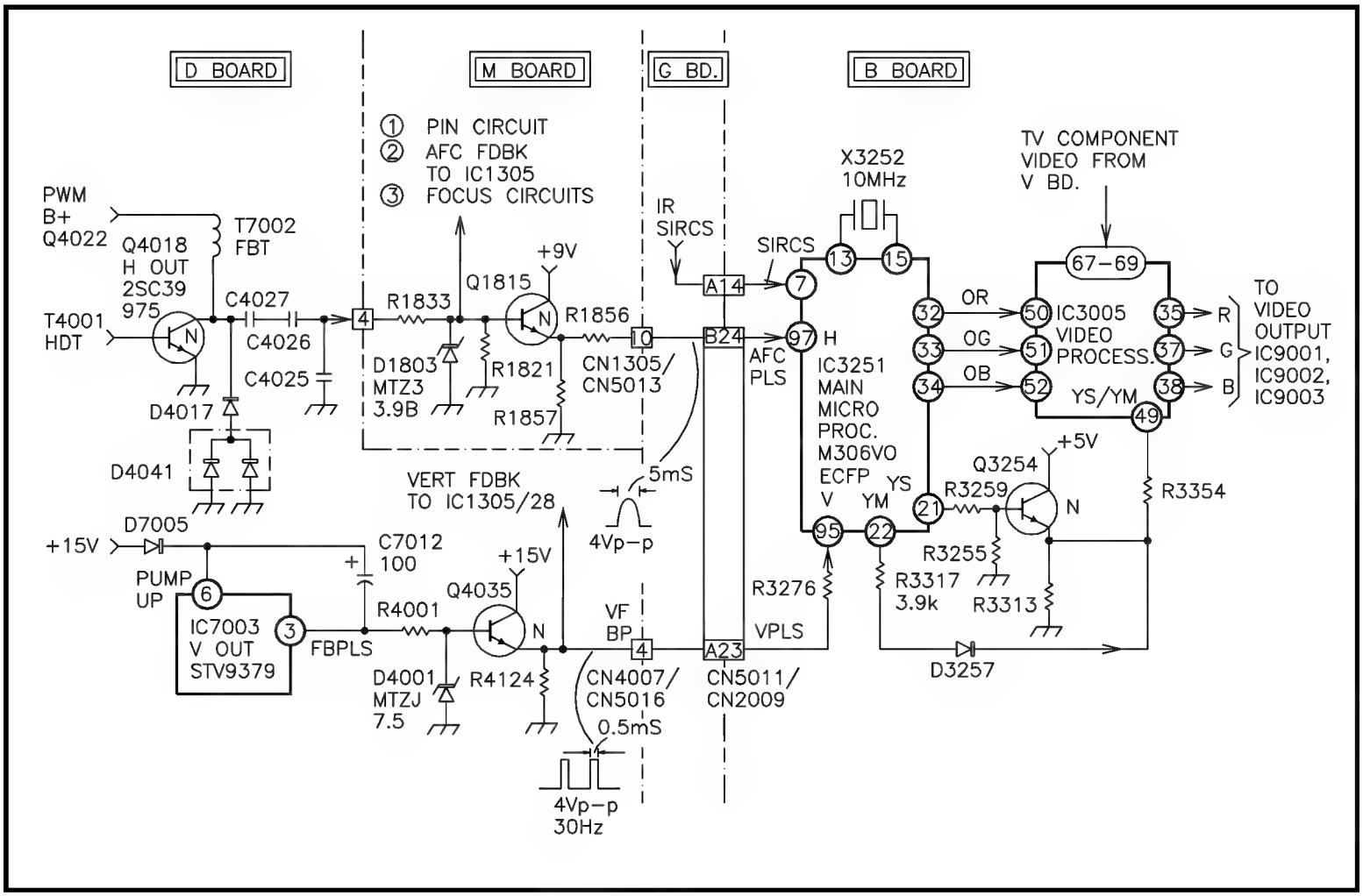
The on screen display circuitry within Main Micro IC3251 places channel numbers and menu information on the TV screen. To perform this it needs to identify the picture tube's beam location by using vertical and horizontal deflection (not station sync) signals. These signals are shaped into 5Vp-p pulses which are input to IC3251/pins 95 and 97. Without either signal there would be no OSD.

Main Micro IC3251 provides a visual indication of the user command. To perform this characters are output as pulses on the respective Or, Og and Ob outputs.

Character Insertion

To make the display appear clean, the active video is blanked for that moment while the character is inserted into the scan. The YS signal from IC3251/pin 21 requests that IC3005/pin 49 perform this full blanking function. When YS goes high, Q3254 is turned on to place +5V into the video processor IC3005/pin 49. The active video is blanked and the OSD character is enabled.

When the menu is called for, the characters are placed on a lower ½ brightness mat. A wide window pulse from IC3251/pin 22 creates this mat. The 4-volt Ym signal output is reduced to 2V at the video processor input IC3005/pin 49. When this window pulse is high internally, the active video is reduced in intensity to create the video mat, as well as enable the OSD signals on the TV screen.



ON SCREEN DISPLAY

HDTV24 1055 2 24 99

Video Process E

The video output stage has only two functions:

1. Amplify the video signal to sufficient levels to drive the picture tube; and
2. Combine the IK pulses and return them to the AKB circuit on the B board.

Video Signal Amplification

The chart below shows the red drive levels with a color bar signal input to video 1 jack.

Red Drive Signal Levels		
Name	Location	Vp-p *
Video Input	CN9001/pin 1	2Vp-p
Video Output	IC9001/pin 8	170Vp-p
Red IK output	IC9001/pin 5	10Vp-p
Common IK return	Q9001/Emitter	3Vp-p

* Noise in not included in the peak to peak measurement.

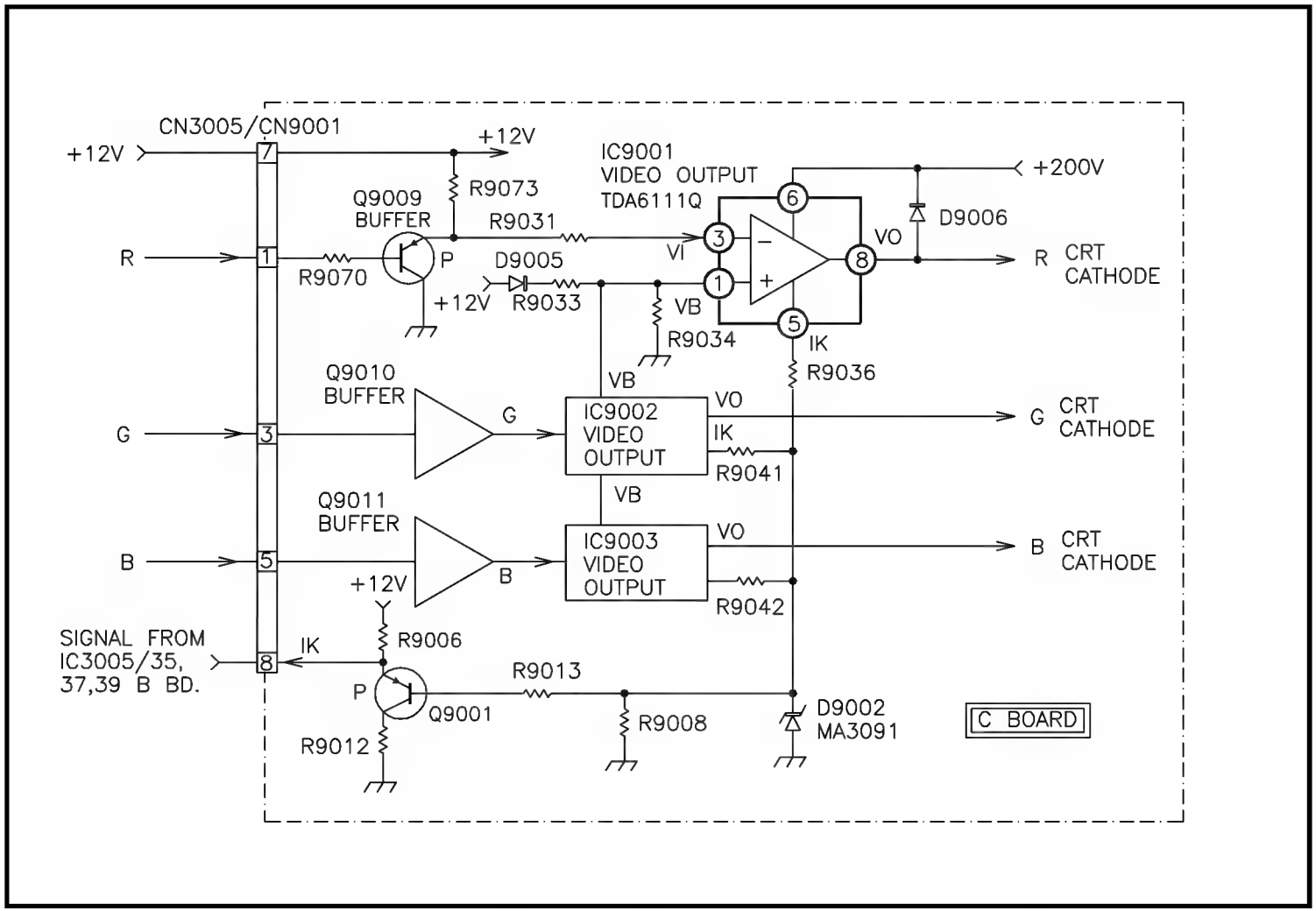
DC Voltages	
CN9001/pin 1 board input	4.5V
IC9001/pin 3 IC input	3.6V
IC9001/pin 8 IC output	144V
IC9001/pin 5 IK output	9.05V

The red video signal from the video processor is input to the C board and buffered by Q9009. The output is applied to the video output IC. This voltage amplifies the input to drive the picture tube.

IK Output Circuitry

The picture tube's cathode current flows through the video output ICs. A sample of that current is output from each IC at pin 5. The three IC outputs (one for each color) are connected in parallel. This way all three IK signals can be returned to the video processor on one input at CN9001/pin 8.

The three IK pulses are located in the vertical blanking area just before the first scanning lines at lines 17, 18 and 19. It is difficult to determine if all three pulses are present at CN9001/pin 8 because they are so small. You can see them with an oscilloscope if you trigger to the larger IK drive pulse from the R, G or B output at CN9001/pins 1, 3 or 5. They are located in the vertical blanking area of the waveform after the vertical sync pulse,



VIDEO PROCESS E

HDTV5 1010 1 27 99

Screen Voltage Control

In other TV sets the picture tube's G2 screen control was either:

1. Part of the FBT assembly where a single lead was brought to the picture tube's C board; or
2. There was a special high resistance, high voltage potentiometer on the C board that permitted adjustment of the screen voltage.

In this set the screen control utilizes three transistors and a small ¼ watt standard potentiometer for control of the final 400 to 600 volt G2 voltage. The configuration is difficult to understand the way it is drawn in the service manual so it has been redrawn here for clarification.

Circuit Operation

This stage has several major parts:

Screen Control Major Components	
Parts	Purpose
R9055, R9085, R9067, R9084	Reduce FBT source voltage and current for control (series dropping resistors). Many resistors are used to prevent HV arcing.
Q9014	Active resistor (biased with +12V at its base).
Q9008	Prebiases the emitter of Q9012 at 4.8 volts.
Q9012	Active resistor and regulator. Q9012 conduction is set by screen control RV9002 and a sample of the screen voltage.
Q9002	Turns ON mute. Remains ON for three seconds each time the TV is turned ON.

G2 Voltage Source

The pulse from the horizontal output transistor's collector is rectified by D4022 so it appears at CN9002/pin 1 on the C board as approximately 1000 volts DC. This voltage is applied to a voltage divider consisting of resistors and transistors to reduce and control the voltage before it is applied to the picture tube's G2 grid.

G2 Path

The current path from CN9002/pin 1 to ground is:

1. R9055, R9085, R9067, R9084
2. Q9014
3. Q9012
4. R9081

Both Q9014 and Q9012 transistors are biased on, completing the current path to ground.

The picture tube's G2 voltage is taken at the junction of the resistors and Q9014. Consequently, a change in the transistor's conductance will change the G2 voltage, permitting control.

Transistor Q9012 is used for G2 voltage control and regulation. Q9012's conduction is set by the screen control RV9002 at its base. This sets the picture tube's screen voltage. If Q9012 conducts harder, the G2 voltage is reduced and the picture is darker.

Q9012 is also used for regulation. Some of the G2 voltage is sampled by R9067 and applied to the base of Q9012. An increase in G2 voltage will cause Q9012 to conduct harder, decreasing the G2 voltage to its nominal value.

Video Mute

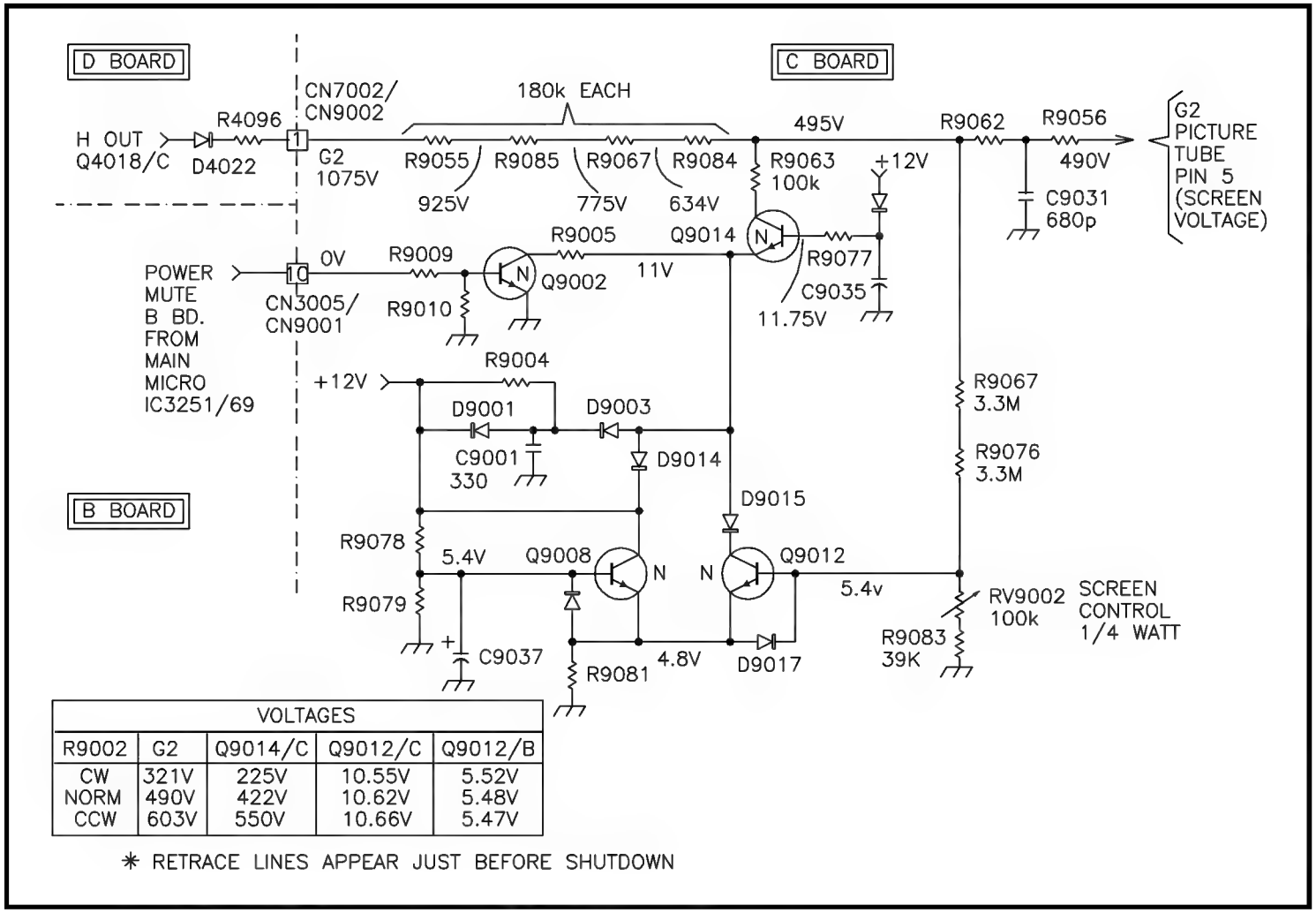
At TV turn ON, the G2 voltage is lowered so the picture is blanked. This is controlled by the main micro IC3251 and performed by Q9002. Q9002 is also in parallel with Q9008. Therefore, when Q9002 is turned ON for three seconds at turn ON, the G2 voltage drops to darken the screen.

G2 Control Range

The normal effects of a misadjusted G2 control are:

CW from the back = Picture reduces in brightness, but does not black out.

CCW from the back = In the 4:3 aspect ratio picture, left and right borders appear as the screen gets brighter. Retrace lines then appear and the TV shuts down.



VOLTAGES				
R9002	G2	Q9014/C	Q9012/C	Q9012/B
CW	321V	225V	10.55V	5.52V
NORM	490V	422V	10.62V	5.48V
CCW	603V	550V	10.66V	5.47V

* RETRACE LINES APPEAR JUST BEFORE SHUTDOWN

SCREEN VOLTAGE CONTROL

HDTV10 1057 2 24 99

Power Supply Block

The power supply consists of several stages. Except for the standby power supply, the Main Micro IC3251 controls the operational sequence of the remaining stages. The stages are listed in the order of operation:

- Standby Power supply
- Power ON stage
- Picture tube Degaussing
- Converter 2 stage
- Converter 1 stage
- Protection stage

Standby Power Supply

This stage is active as long as the TV is connected to AC. Therefore it always supplies standby +12 volts and standby +5 volts.

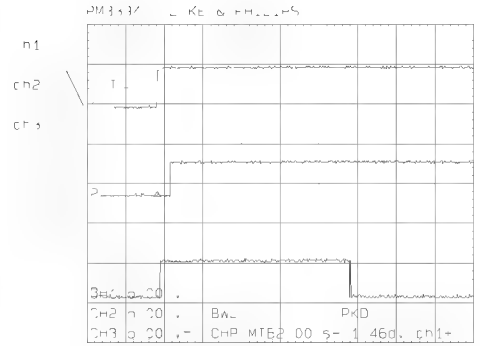
Standby +12 volts is applied to the master power switch which is routed to the AC relay's coil when the switch is pressed (latched ON). The +5 volts powers the Main Micro IC3251 and infrared receiver so they can detect a power ON command.

Power ON

When a power ON command is received by the Main Micro IC3251, it first powers the AC relay RY5501. RY5501 feeds the converter 2 circuitry. It then powers the Degaussing coil relay RY5503 and the converter 1 stage. It is the converter 1 stage that makes +135Vdc for high voltage development.

Picture Tube Degaussing

Degaussing is a common method color TV manufacturers use to eliminate residual magnetism in the picture tube. The residual magnetism in the picture tube acts as a magnet, causing the electron beam to be pulled away from its target. AC current applied to the degaussing coil creates an alternating magnetic field to disorient the tube's residual magnetism, assuring proper beam landing and color purity.



Waveform PSblk - Power Sequence

Channel 1 - AC relay output of Main micro IC3251

Channel 2 - Main relay output of Main micro IC3251

Channel 3 - DG output of Main micro IC3251 to RY5503

All waveforms are 5Vp-p; time base = 2 sec/div

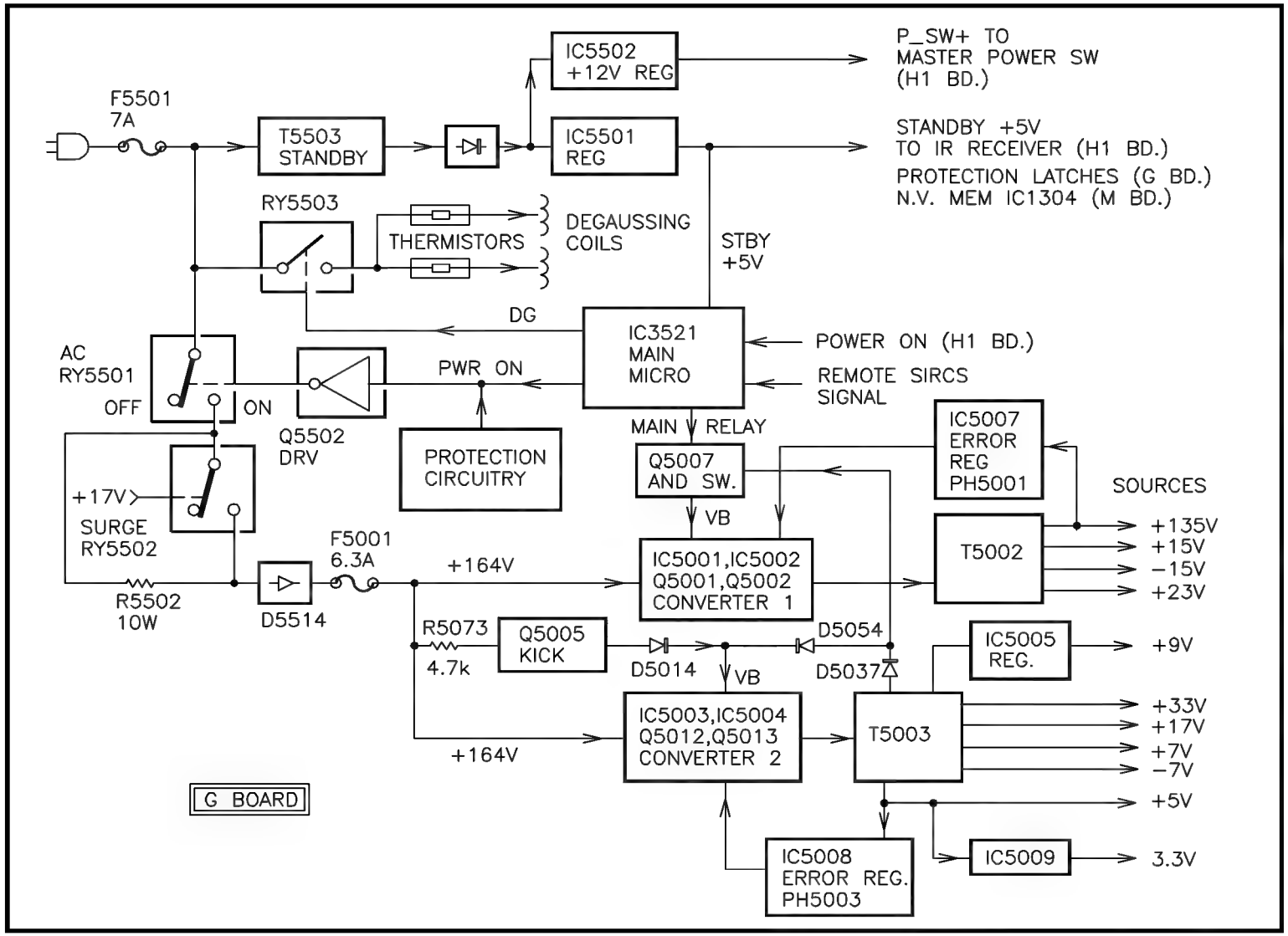
This degaussing stage is powered with 60Hz AC immediately after the AC relay is energized. The heavy current that passes through the two low resistance degaussing coils also passes through the negative temperature coefficient thermistors. As these thermistors heat up from the current flow, their resistance increases until the coil current and magnetic field is negligible, concluding degaussing. As a precaution, the degaussing coil relay is de-energized 9.5 seconds after being powered.

Converter 2 Stage

Converter 1 and converter 2 stages are similar. Their only differences are how they first power up and what voltages they deliver to the TV.

After the AC power relay is energized, Converter 2 gets a kick-start voltage from Q5005. R5073 limits the amount of current through Q5005 to start converter 2's oscillator. Once the converter is running, one output (D5037) sustains the Vdd operating voltage. The higher converter voltage reverse biases the kick-start diode D5014, blocking the start voltage from transistor Q5005.

Regulation for the converter 2 stage is accomplished by sampling the +5 volt output and returning it to the oscillator. The sample voltage causes a converter oscillator frequency change, which results in the voltage correction.



POWER SUPPLY BLOCK

HDTV11 1058 2 24 99

Converter 1 Stage

After the Main Micro turns on both the AC and degaussing coil relays, the Main Relay output (ch 2) turns ON Converter 1 using switch Q5007. However, Q5007 acts like an AND gate, requiring a second input before converter 1 is turned ON. This second input is a voltage that comes from converter 2 (D5037). Therefore, converter 2 must be ON before converter 1 can come to life.

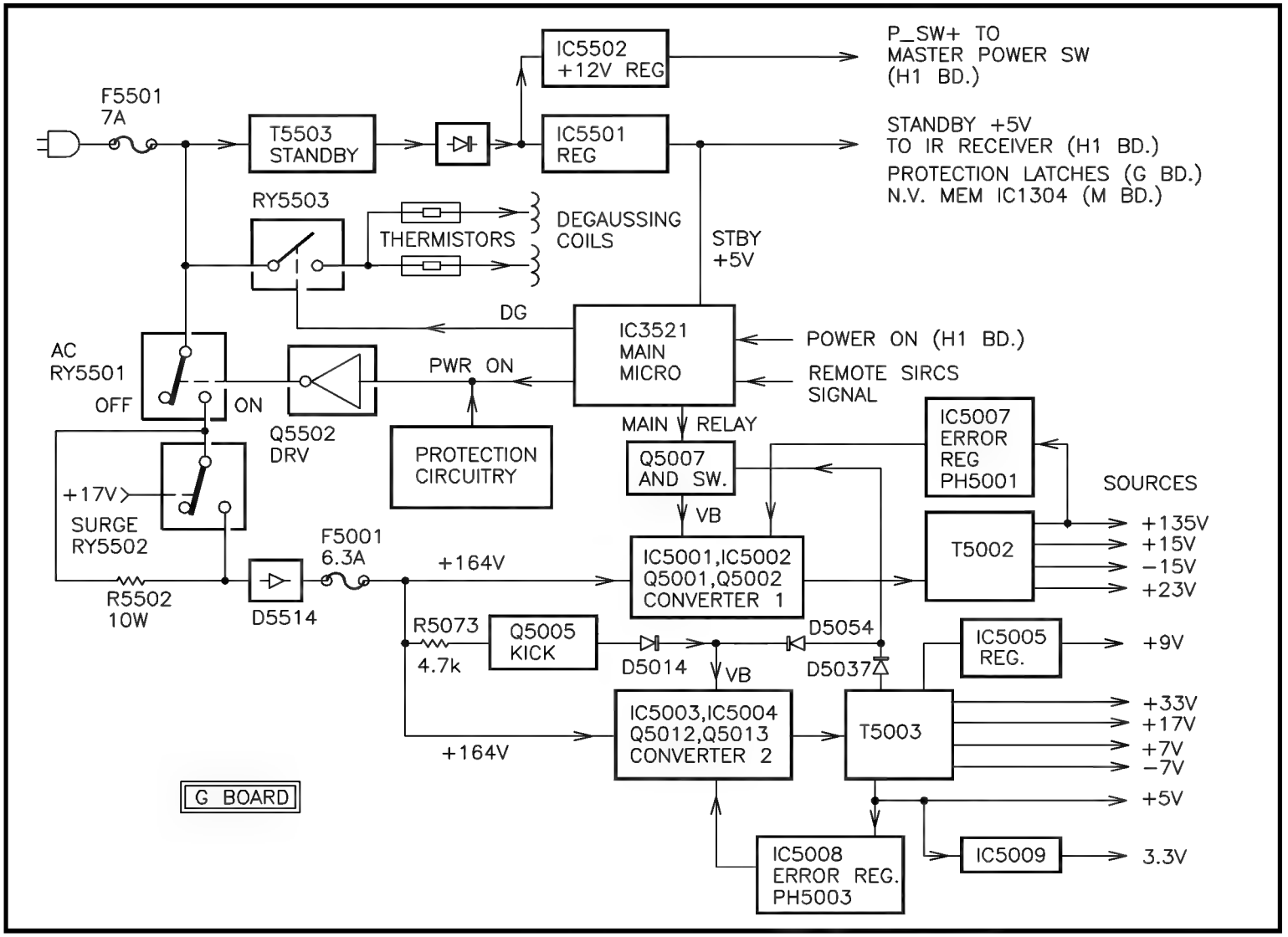
Regulation is performed using a sample of the +135Vdc that is output. An error voltage changes the converter's oscillator frequency, which corrects the +135Vdc.

Protection Stage

The protection stage has many inputs (see the Overall Protection Block diagram). When a problem is detected, this circuit latches the Main Micro's power ON output to ground so the AC relay (and TV) shuts off. Turning off the TV from the remote or front panel resets the latch.

The protection circuit monitors the following items and shuts the TV off if there is a problem:

- Vertical deflection loss
- +5V OCP
- +135V OCP
- +135V OVP
- +15V OVP
- Driver supply voltage OVP
- H. Output OVP
- H. Output OCP
- FBT Output OVP
- H Centering IC4003 OCP



POWER SUPPLY BLOCK

HDTV11 1058 2 24 99

Standby Power

Overview

When this TV is plugged into AC, the standby power supply stage becomes active and outputs standby +12 volts and standby +5 volts. The +12 volts are applied to the master power switch, which is routed to the AC relay's coil when the switch is pressed (latched ON). The +5 volt powers the Main Micro IC3251 and infrared receiver so they can detect a power ON command.

Circuitry

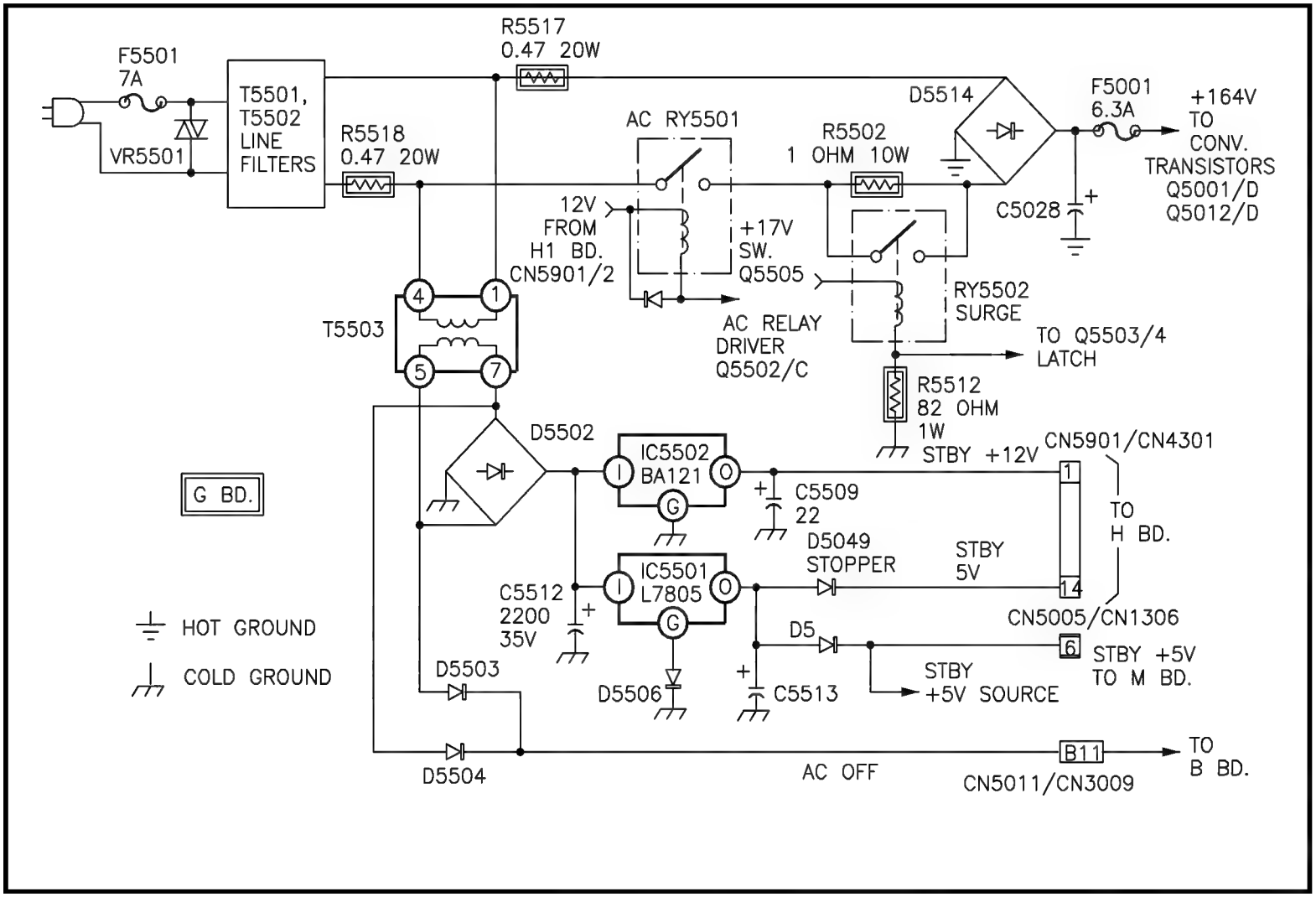
There are several components that condition the AC input before reaching the 60 Hz. standby transformer T5503:

AC Line Input Parts	
Number	Purpose
VR5501	Suppresses incoming narrow voltage spikes by reducing resistance when a high voltage threshold is reached.
T5501, T5502	Common mode rejection transformers to cancel out of phase AC input or TV output noise.
R5518	Surge limiting resistor.

The standby transformer T5503 and bridge rectifier D5502 apply approximately +23 volts to +12 and +5 volt regulators. The standby +5Vdc goes to the infrared remote control receiver and the Main Micro IC3521.

The standby +12 volts sent to the H1 board is applied to the Master Power switch. As long as this power switch is latched ON, +12 volts is returned to the high end of the AC relay coil RY5501.

The output of standby transformer T5503 is also applied to the full wave rectifiers D5503 and D5504. The output is connected to the Main Micro IC3521 to detect an AC loss. This provides enough time for the Main Micro to save user settings into memory and cause audio and video muting just before a complete power loss.



STANDBY POWER

HDTV9 1015 2 24 99

Converter 2

Converter 1 and Converter 2 stages are similar. The only differences are how they first power up and what voltages they deliver to the TV.

After the AC power relay is energized, Converter 2 receives a kick-start voltage from Q5005. R5073 limits the amount of current through Q5005 to start Converter 2's oscillator. Once the converter is running, one output voltage line (D5037) sustains the Vb operating voltage. The higher converter voltage reverse biases the kick-start diode D5014, blocking the kick-start voltage from transistor Q5005.

Converter Operation Sequence

There are several parts to the converter stage. They are listed in the order of operation:

Converter Stage Parts			
Name / Major Components	Inputs	Output	Purpose
Kick start Q5005	Current limited +164V from R5073	+12V through blocking D5014 to IC5004/pin 12	Starts the IC5004 converter oscillator and supply IC5003.
Driver/Osc Control IC5004	Vcc - pin 12 Freq. control - pin 6	Out of phase 63.4kHz square wave – pins 9 and 10	Oscillator Freq. control Driver
Amplifier / Driver IC5003	Logic supply voltage – pin 9. Output supply voltage – pins 3 and 6. Complementary inputs 12Vp-p – pins 10 and 12.	Gate drive output – pins 7 and 1.	Outputs in phase with inputs. Level shifting for top MOSFET Q5012.
Output MOSFETs Q5012 & Q5013	12Vp-p drive signals from IC5003/pins 1 and 7.	150Vp-p square wave 63.4kHz @ Q5012/Source	
Transformer T5003	286Vp-p rough sine wave @ T5003/pin 8	Multiple secondary voltages	Ground isolation. Provide various TV voltages.
IC5008, PH5003, D5024, D5030	+5V source from D5041.	Reduction of voltages at IC5004/pins 1 and 6.	Converter 2 regulation using +5V output as fdbk.

Kick Start

When switched AC is applied to D5514, unregulated +164V is applied to the converter MOSFETS Q5012 in Converter 2 and Q5005. Kick-start transistor Q5005 regulates this voltage to +12 using zener D5018. Q5005 is current limited by a low wattage R5073 at its collector. Q5005 is not designed to run continuously.

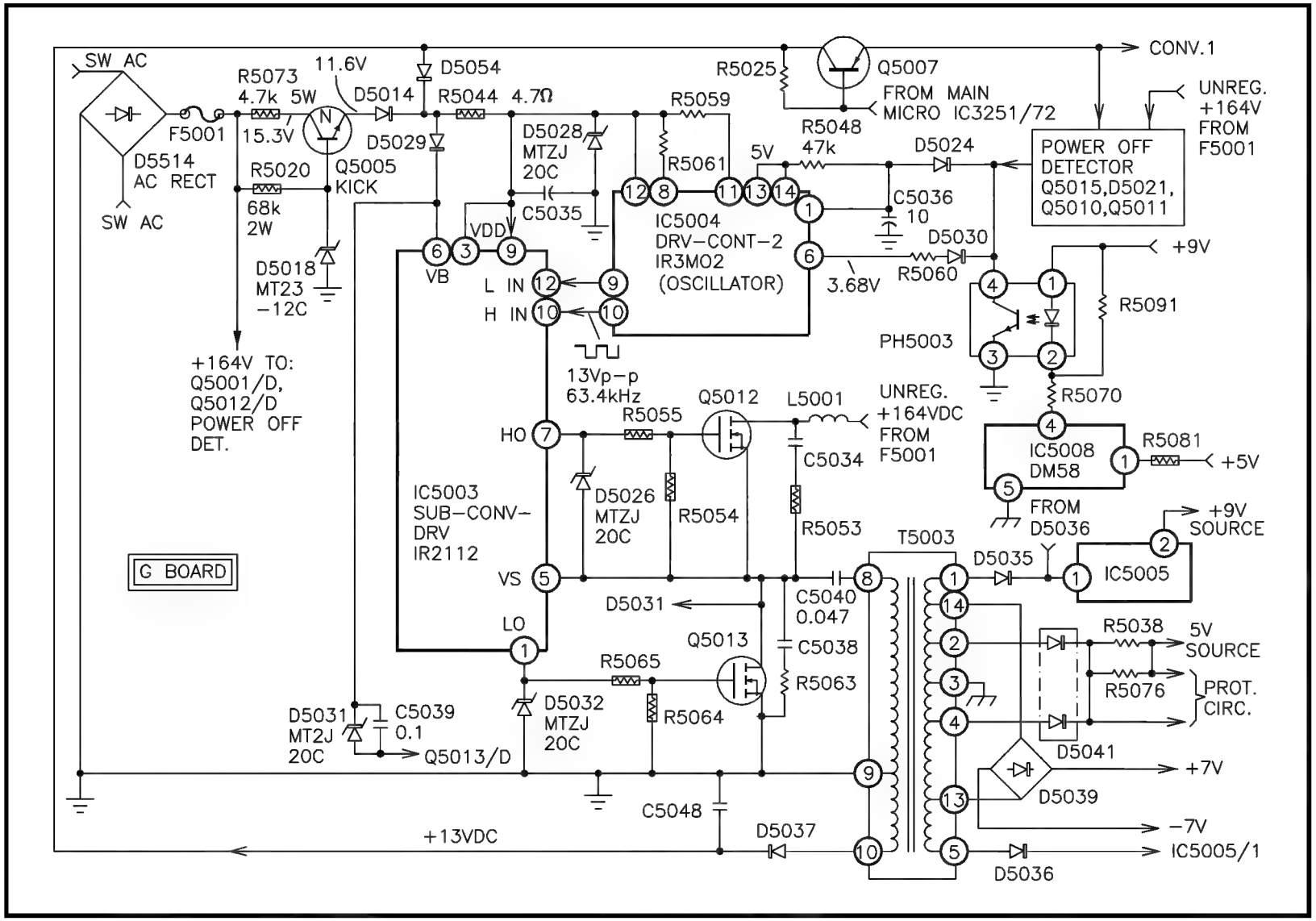
Oscillator/Driver/Output

When IC5004 receives this start voltage at pin 12, its internal oscillator runs and a square wave is output to driver IC5003. IC5003 provides sufficient current to drive the two output MOSFETs, Q5012 and Q5013. These MOSFETs feed Converter 2's T5003, which outputs various TV operating voltages.

Kick-start Cutoff

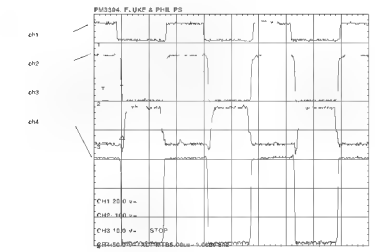
One output from T5003/pin 10 is rectified and feeds +13 volts back to power the converter logic IC5003/pins 3 and 9 and IC5004/pin 12. The higher voltage also back biases D5014, shutting off the initial kick-start supply voltage from Q5505/emitter.

The waveforms show the input (ch 1) and outputs at Driver IC5003 (ch 2 and 3). The waveforms were taken with a scope connected to hot ground and the TV connected to an isolation transformer.



CONVERTER 2

HDTV12 1035 3 9 99



Waveform Conv – IC5003 In/Out			
	Name	Location	Voltage/div
Channel 1	Input drive	IC5003/pin 10	12Vp-p
Channel 2	High drive	Q5012/gate	160Vp-p
Channel 3	Low drive	Q5013/gate	12Vp-p
Channel 4	Output	Q5013/drain	150Vp-p
Time base	5usec/div		

Regulation

+5V is returned to the oscillator stage for regulation. The +5V output is applied to error regulator IC5008/pin 1. Internally the +5V input is compared to a reference and its difference (error) is output from IC5008/pin 4 to PH5003/pin 2. This photocoupler couples the error voltage signal from the cold to hot ground into IC5004/pins 1 and 6.

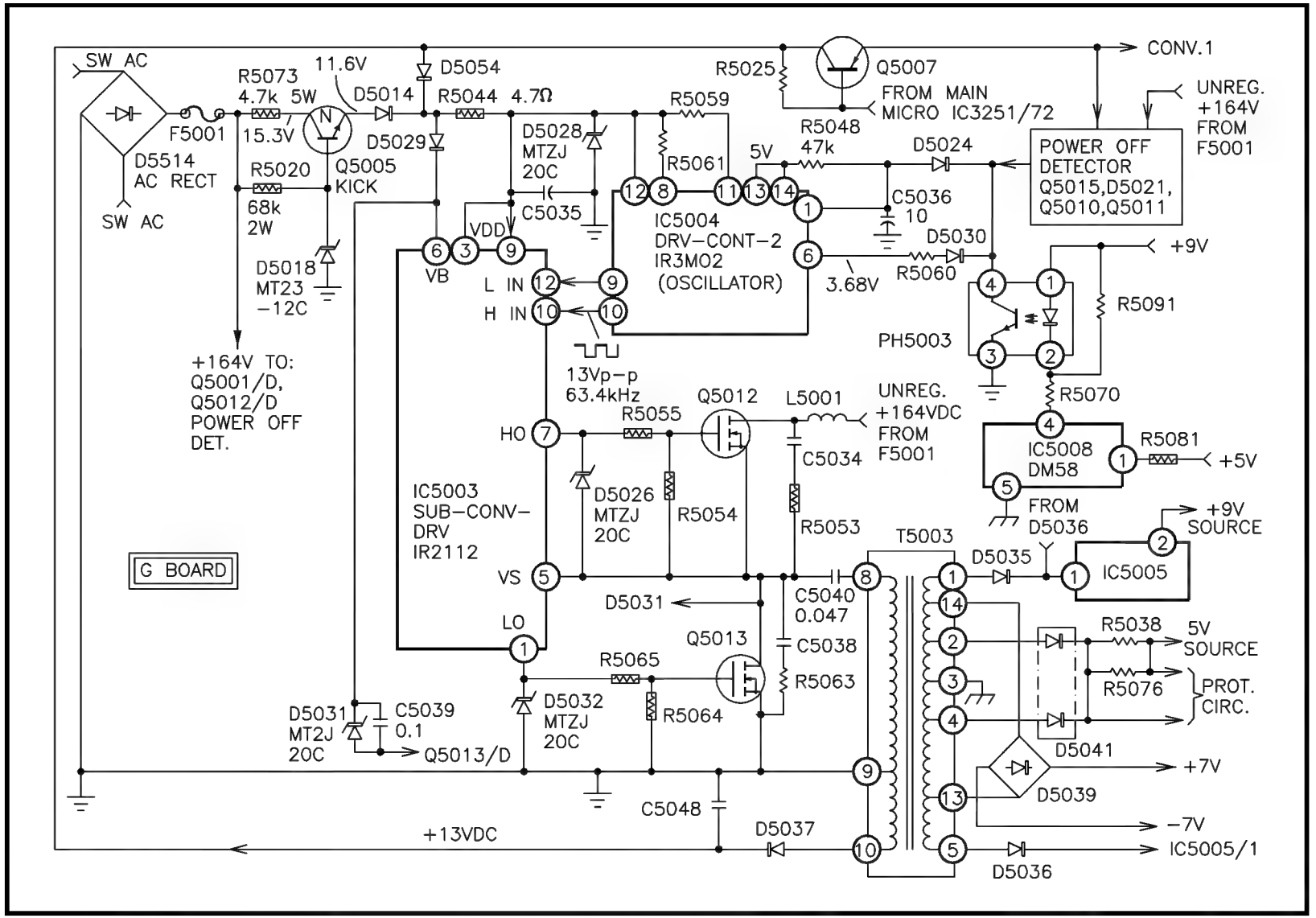
At IC5004, an increase in control voltage results in a decrease in oscillator frequency. The oscillator signal is amplified by IC5003, Q5012, and Q5013 and is applied to a LC circuit consisting mainly of C5040/T5003. The oscillator frequency is positioned above (higher than) the resonate frequency of C5040/T5003. Therefore, an increase in the oscillating frequency results in a reduced output from the T5003 transformer (L). Conversely, a decrease in oscillator frequency results in a higher secondary voltage.

Regulation Effects				
+5V @ D5041	IC5008/pin 4	PH5003/pin 4	Oscillator frequency	+5V corrective Output
↑	↓	↓	↑	↓

Effects of increased AC line voltage on Converter 2		
AC input	PH5003/pin 4	Oscillator frequency
100V	3.2V	56.2kHz
120V	3V	63.54kHz
130V	2.91V	68.57kHz

Power OFF Detector

Q5015, Q5010, Q5011 and D5021 are the major parts that comprise the power off detector. When the AC relay is turned OFF, this circuit detects a loss of +164V and grounds PH5003/pin 4. This increases the oscillator frequency, which decreases the Converter 2 output voltages during power loss. The connection to Converter 1 from this stage performs the same function, but is not shown.



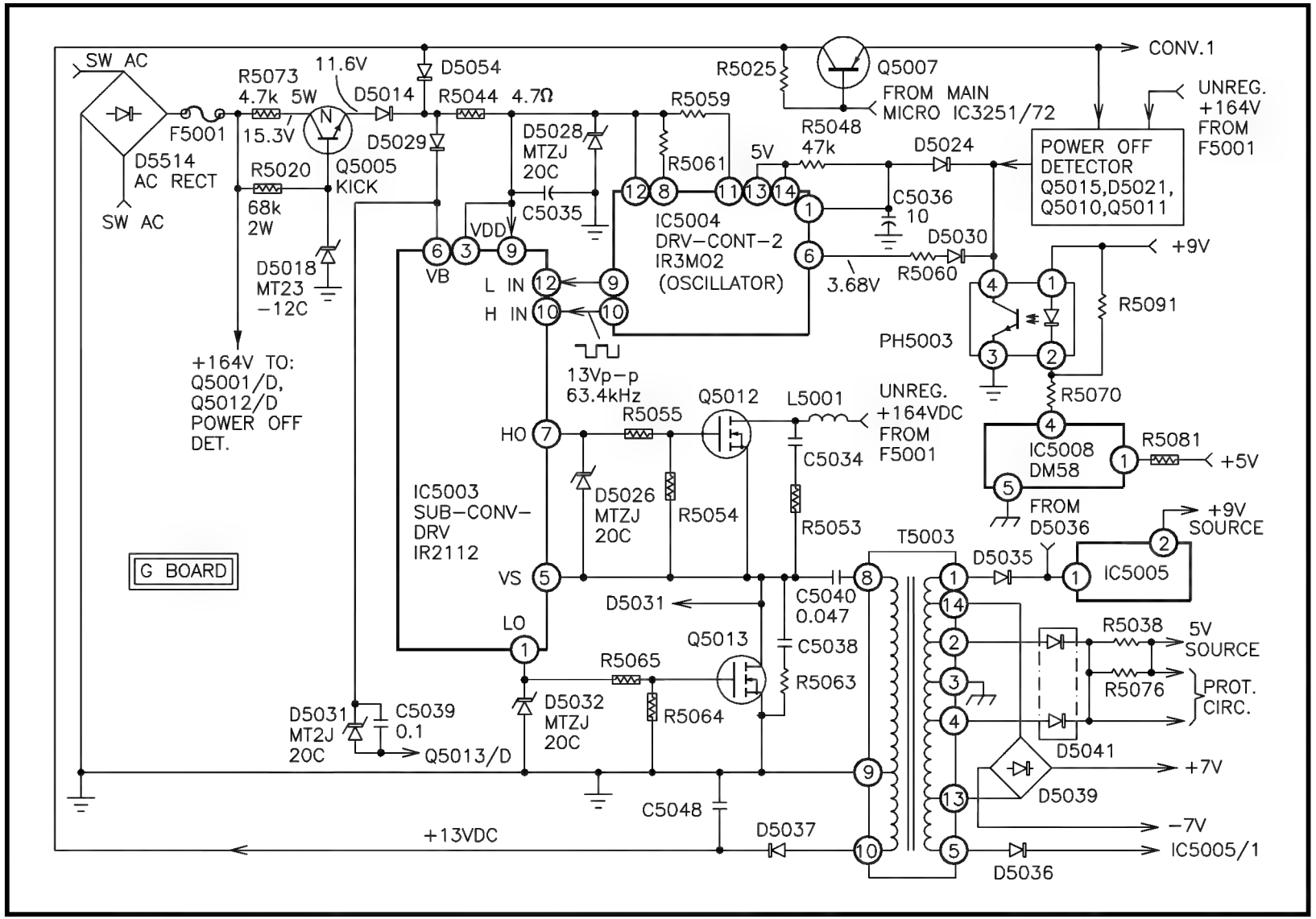
CONVERTER 2

HDTV12 1035 3 9 99

Troubleshooting

Possible Converter Symptoms/Causes		
Symptom	Cause	Reason
Dead set	MOSFET Output failure. F5001 open. Kick start R5073 burnt. D5028 shorted Conv 2 failure.	Only one or both converters is/are dead.
Relays click and stop. Timer light blinks 4 times (vertical failure).	Loss of top or bottom drive signal: a) No Top drive – D5026 shorted, Q5012 open, IC5003 Vb positive bias voltage (pin 6) missing from D5029. b) No Bottom drive – D5032, bootstrap cap C5039 or D5031 leaky/shorted, Q5013 open.	Vertical stage not working because the horizontal FBT voltages are not present, caused by insufficient voltage from Converters 1 or 2.

IC5003 Normal DC Operating Voltages @ Pins						
1	5	6	7	9	10	12
+5.4V	-5.8V	-3.1V	-5.4V	+12V	+5.5V	+5.4V



CONVERTER 2

HDTV12 1035 3 9 99

Overall Protection Block

Protection

The protection circuitry on the G and D boards monitor the following items and shuts the TV off if there is a problem:

G Board:

- Vertical deflection loss (self diagnostics - light indication)
- +5V OCP monitored (self diagnostics - light indication)
- +5V OVP monitored (self diagnostics - light indication)
- +135V OCP monitored (self diagnostics - light indication)
- +135V OVP monitored (self diagnostics - light indication)
- +15V OVP
- Surge relay RY5502 not energized.

D Board:

- Driver supply voltage OVP
- H. Output OVP
- H. Output OCP
- FBT Output OVP
- H Centering IC4003 OCP

Four general failure detectors on the G board not only shut down the TV set but also inform the Main Micro IC3251 of the failure. The Main Micro IC3251 provides a blinking light indication of the failure. This micro routine is called the self-diagnostic program and found in many Sony Trinitron TV sets made since late 1997.

Self Diagnostics

This TV also has self-diagnostics circuitry that is connected to five sensing circuits. A failure detected by one of these circuits is registered by the Main Micro IC3251 and permits it to blink the front panel standby light a number of times to identify the problem area.

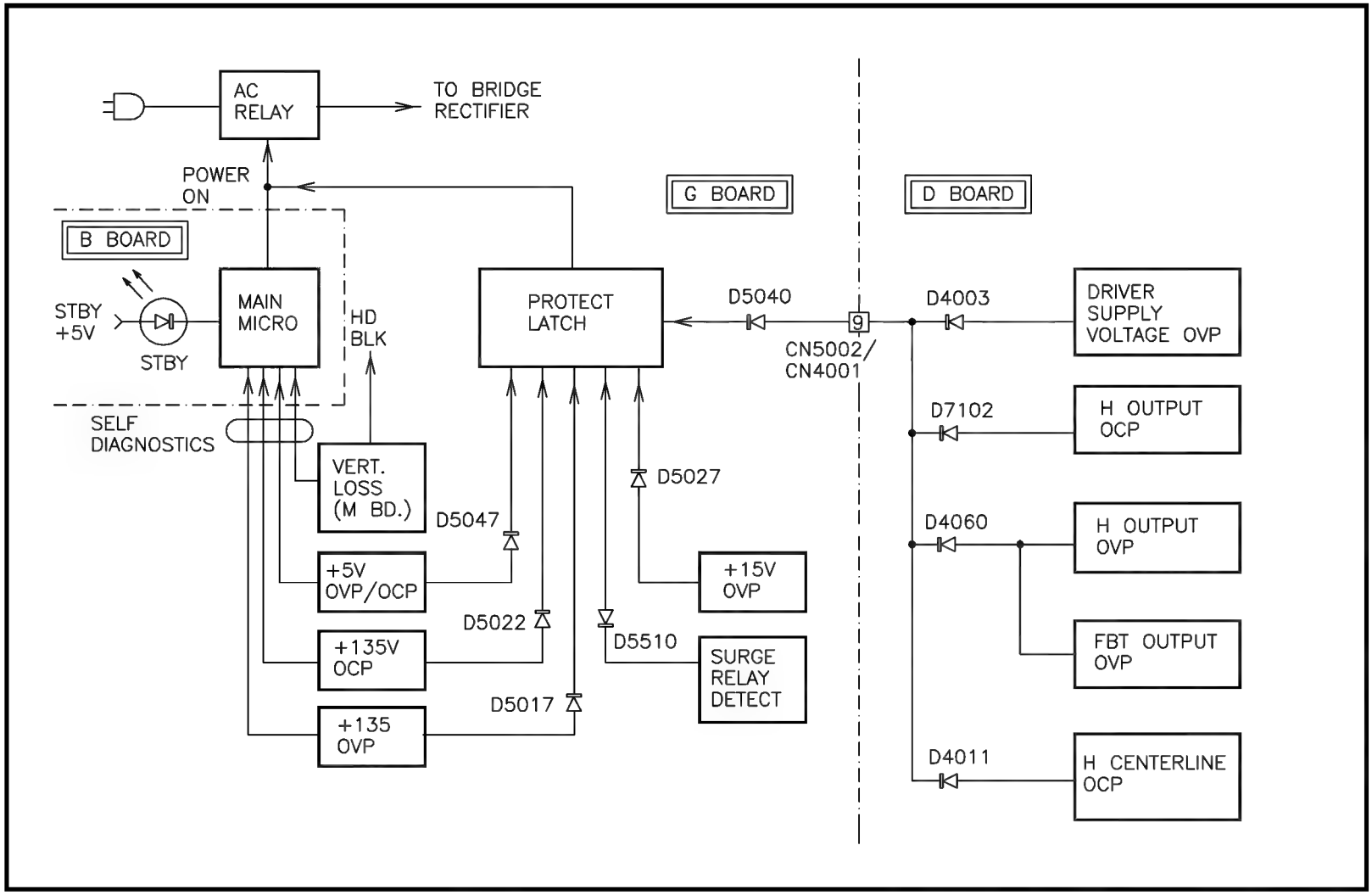
Standby Light Indication		
# times light blinks	Shutdown cause / Symptom	Possible defective circuit
2	B+ OCP / TV Shutdown	Horizontal driver, horizontal output, FBT, or PWM. Dynamic focus circuit & Pincushion correction circuit.
3	B+ OVP / TV Shutdown	Converter 1: • regulation failure • oscillator off frequency
4	Serial Data shutdown instruction from Deflection Control IC1305 to Main Micro IC3251. / TV Shutdown	Vertical failure Horizontal scan (FBT) derived voltage failure (no Horizontal) Low converter 1 or 2 voltages (causing low scan voltages)
5	Standby light blinks 5 times and repeats. Whites in the pix are not white. Sound OK / Video Processor IC3005 can't White balance (IK failure). This failure will not shut down the TV set.	Screen control setting too low. Video processor or video output stage failure. See video process. Incorrect Cr or Cb data in the service mode.
6	+5V OVP, OCP / TV Shutdown	Converter 2 regulation. Short on +5V line.

Further details about the self-diagnostics circuitry and its OSD for intermittent problems are explained in the service manual.

Repair Strategy

The strategy for identifying the cause of the TV shutdown is the same as it would be for a projection TV or even a camcorder:

1. Note the symptoms like # relays clicked, frying noise, blinking lights, station sound, OSD, etc.*
2. Check power handling devices or common failures such as the Horizontal, Vertical, Audio, and Video output ICs for shorts.
3. Narrow the problem to a board
4. Isolate the problem to the circuit using the descriptions in the protection circuitry diagrams that follow.



OVERALL PROTECTION BLOCK

HDTV43 1107 3 9 99

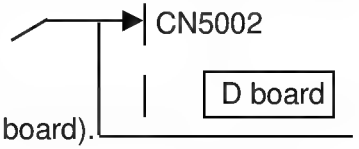
Board Determination

If the standby light does not blink but the unit shuts down, the problem is in one of the seven remaining areas that were not monitored by IC3251. Five items are on the D board; two items are on the G board.

First prove the problem is not on the **G** power supply board with a peak hold DVM. A conventional DVM (or older one with a slow gate/sample time) may not be fast enough to measure the full voltage before shutdown.

You will see if the D board is outputting the correct voltage or a shutdown demand voltage by using the following steps:

1. Latch the front panel master power switch IN (TV on).
2. Plug the set into AC. There should be no sound and the TV is off.
3. Monitor the voltage at CN5002/pin 9.
4. Press the remote's power ON button.
5. 0.3Vdc or 1.3Vdc will be measured.
   a) **0.3Vdc** (normal voltage from the D board). means the problem is on the **G board**. It can be caused by:



- A protection latch (Q5504/Q5503) defect (G board)
- Excessive +15 volts from converter 1 (G board)
- The surge relay did not engage (G board)

Measure the +15Vdc @ CN5002/pin 5 when you power ON the TV again with the remote. The trip voltage is +22 volts. If the +15V pin is below +22V, the problem is the protection latch or the parts around it (surge relay circuit). See the Protection Circuit 1 diagram.

b) **1.3Vdc** at CN5002/pin 9 means the problem is on the **D** deflection board. You will need to go to the protection circuit 3 diagram for further troubleshooting now that you have identified the board.

* Complete listings of this TV's normal operating conditions in different modes are at the beginning of this book under "Normal Operation".

Here is a partial list.

The normal sounds at power ON are:

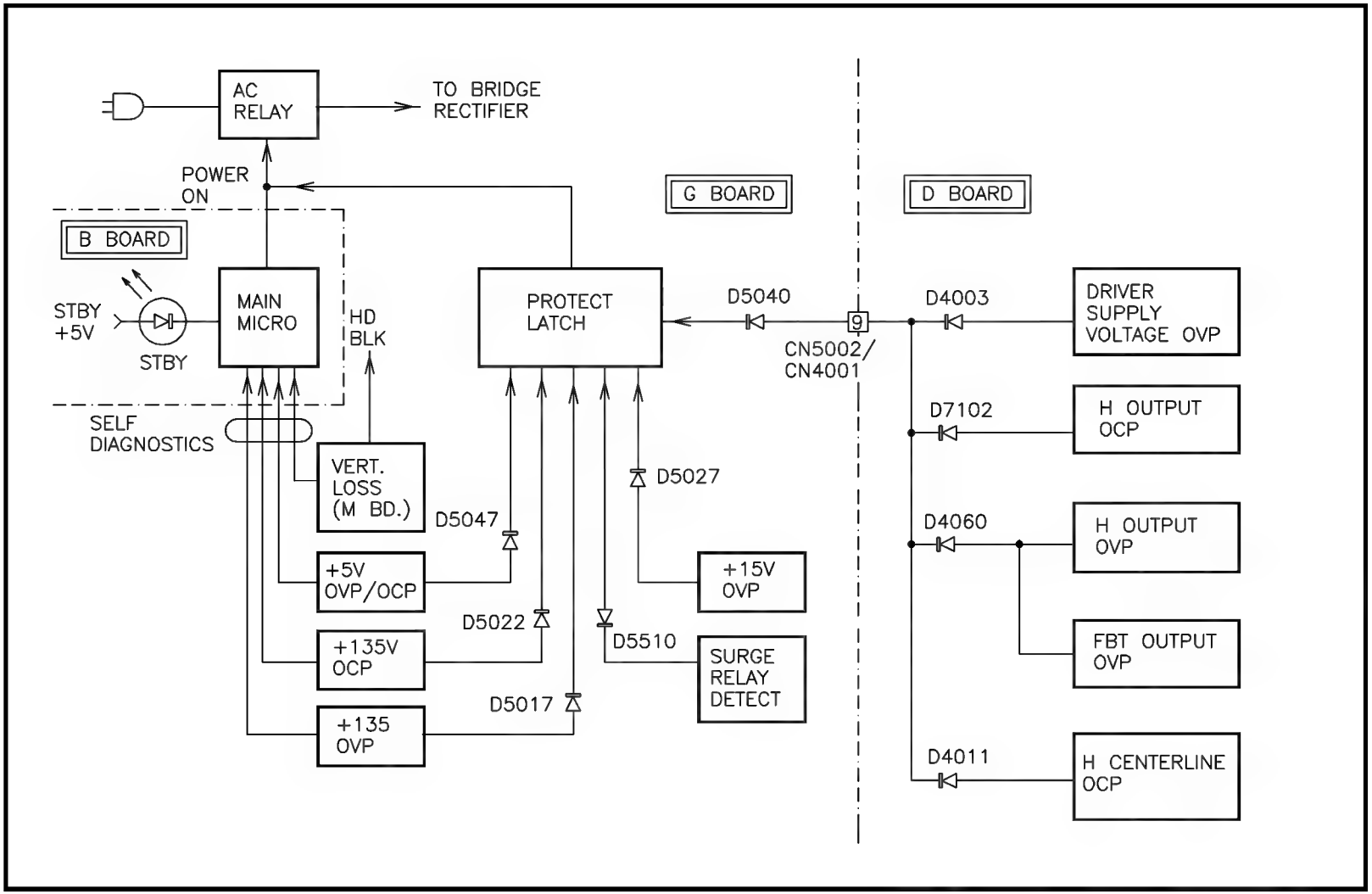
Plug into AC = no sound

When the power ON button is pressed:

1. 2 relays click (3 actually click – AC, surge, & degauss)
2. Degaussing coil thump
3. Frying noise (HV).

When the power is turned OFF:

1. 2 relays click



OVERALL PROTECTION BLOCK

HDTV43 1107 3 9 99

D Board Protection Block

Protection

The protection circuitry on the G and D boards monitor the following items and shuts the TV off if there is a problem:

G Board:

- Vertical deflection loss (self diagnostics - light indication)
- +5V OCP monitored (self diagnostics - light indication)
- +5V OVP monitored (self diagnostics - light indication)
- +135V OCP monitored (self diagnostics - light indication)
- +135V OVP monitored (self diagnostics - light indication)
- +15V OVP
- Surge relay RY5502 not energized.

D Board:

- Driver supply voltage OVP
- H. Output OVP
- H. Output OCP
- FBT Output OVP
- H Centering IC4003 OCP

Horizontal Drive Signal Flow

The D board contains power handling deflection components. The H drive signal is amplified by the horizontal driver, Q4011 and Q4018 output devices on this board. The resultant output signal is used to develop flyback voltages and yoke deflection current. Major power handling circuits on the D board are monitored for excessive voltage or/and current. TV shutdown will occur if there is a danger of this.

Driver supply voltage OVP

H. Output OVP

Both the driver and output devices (Q4011 and Q4018) need B+. The B+ is supplied and regulated by PWM circuits, Q4003 & Q4022. The voltage from both of these PWM stages is monitored by over voltage protection sensing circuits (OVP) and connected via D4003 and D4060 to the shutdown latch located on the G board.

H. Output OCP

The current to the H. output and centering stages is also monitored by the protection sensing circuits on the D board. Q7003 watches the current flowing from the +135V supply through the following sections before arriving at the Horizontal Output device, Q4018:

+135V – source voltage from converter 1

Q7003 – Current sensing

Q4022 - PWM

T7002 - FBT

Q4018 – H Output

Leakage or shorts in any component in the above path will permit voltage to pass through D7102 into the G board's protection latch.

FBT Output OVP

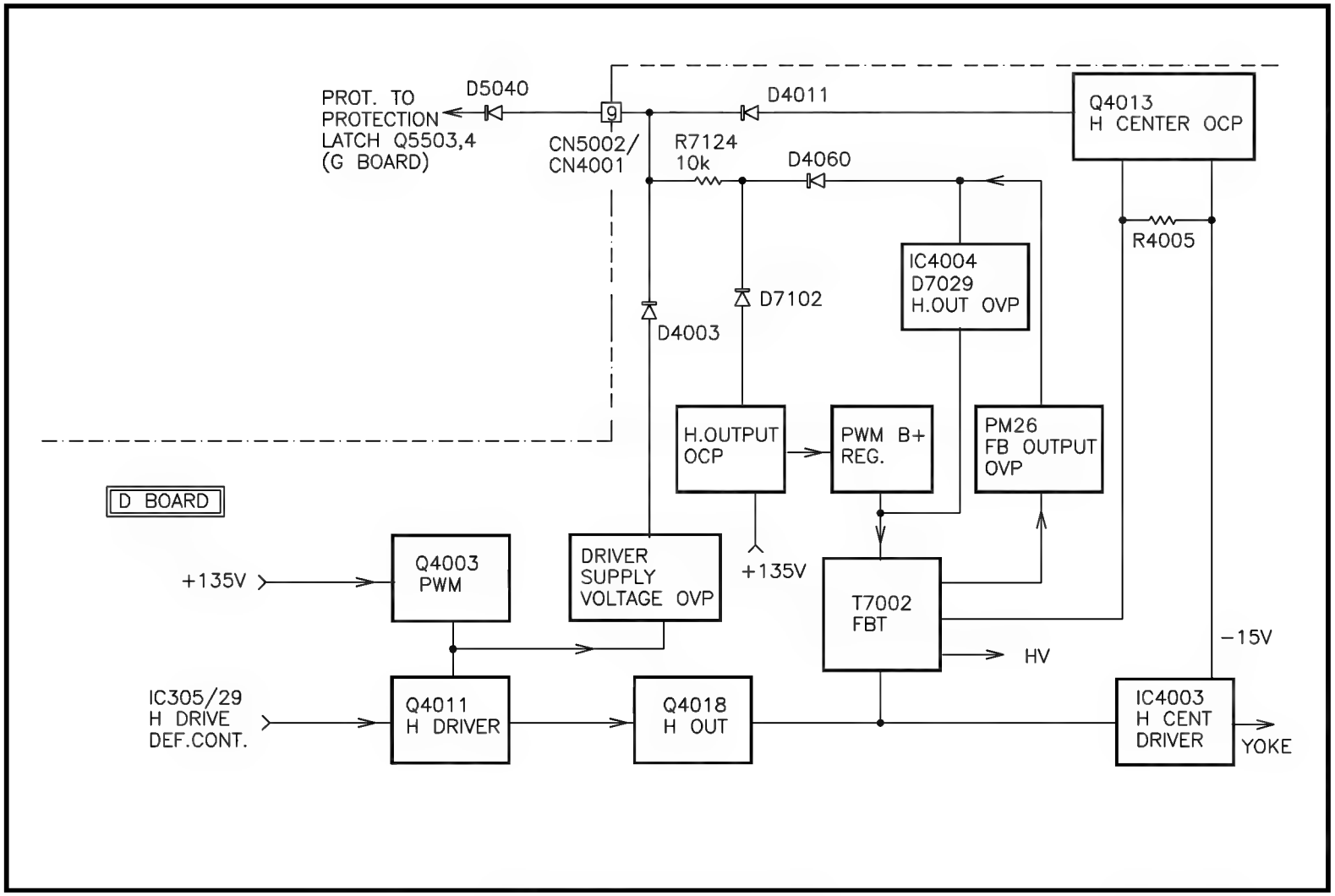
If a resonate capacitor in the H. output stage opened, or if Q4022 shorted, the high voltage from the T7002 FBT could go dangerously high. To prevent this danger, a flyback winding is monitored for excessive voltage. Reference Module PM26 detects this danger and applies voltage through D4060 into the protection latch on the G board. This will shut down the TV set.

H Centering IC4003 OCP

A shorted horizontal centering driver IC4003 could damage the FBT and the horizontal output transistor. To detect this failure, Q4013 monitors the current consumed by the centering IC4003. After the failure, Q4013 applies voltage through D4011 into the protection latch on the G board. This will shut down the TV set, preventing further damage.

Troubleshooting Concept

A failure in any one of the stages being monitored will apply a voltage through a blocking diode across the CN5002/CN4001/pin 9 board junction and trip the protection latch on the G board. You can determine which section has failed by measuring the anode of each blocking diode as the set shuts down. Normally there is no voltage. A voltage indication identifies the problem block connected to that diode.



D BOARD PROTECTION BLOCK

HDTV41 1106 3 9 99

Protection Circuit 1

Power ON

The protection circuitry is connected to the power ON circuit to shut off the TV set. The power ON path is mapped out in the chart below listing the purpose of the parts:

Power ON Parts			
Name	Input	Output	Purpose
Master power ON/OFF switch	Mechanical pushbutton – self latching	+12V for AC relay On command to Main Micro IC3251/46	Switches the +12V AC relay coil voltage. Informs IC3251 of the sw position.
Main Micro IC3251	Master power sw S4301 into pin 46. IR command from IC4301 into pin 7.	Power ON drive signal from pin 71	TV power ON control
Q5502	0.6V power ON from IC3251/pin 71	Energizes AC relay RY5501 to power the TV set.	Amplifier/relay driver
D5515, Q5505	Low from Q5502/C at turn ON	Energizes surge relay RY5502 to shunt surge resistor R5502.	Reduce inrush current extending relay contact life.

When the TV power button is pressed, the Main Micro IC3251/pin 71 outputs +5V to turn on relay driver transistor Q5502. Q5502 turns on the AC relay, as well as a second relay driver transistor Q5505. Q5505 energizes the surge relay. Therefore at power ON, the AC and surge relay turn ON. In another stage, a third (degaussing coil) relay that is not shown also turns ON. Only the first two relay clicks are heard. The degaussing coil relay clicks ON at the same time as the AC relay and turns OFF approximately 9.5 seconds later (just about the same time as picture unmuting occurs).

Protection Latch Circuitry

The protection circuit uses a latch formed by Q5503 and Q5504 to divert power ON current from IC3251/pin 71 to ground. This starves the AC relay driver transistor Q5502 by removing its base bias so the TV shuts down.

The protection latch remains active as long as the Main Micro IC3251/pin 71 is outputting a power ON command. Turning the TV OFF (IC3251/pin 71 then goes low) resets the Q5503 / Q5504 latch.

The latch can be triggered by any of 12 inputs (see the Protection Block). In this diagram, only two items on the G board are monitored:

- +15 OVP and
- Surge relay RY5502 not energized.

+15 OVP (Over Voltage Protection)

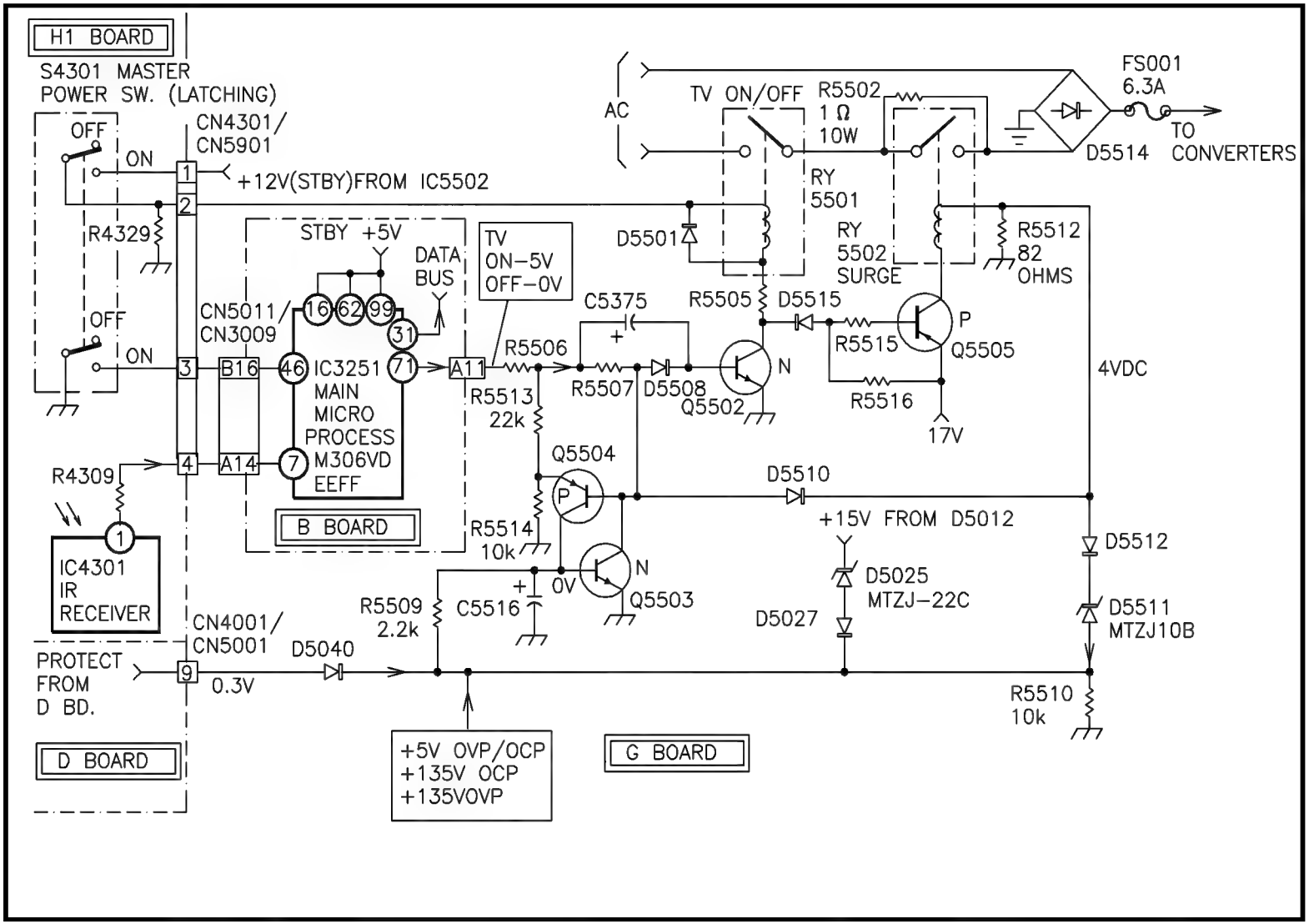
+15 volts from Converter 1 is monitored by zener D5025 for excessive voltage. If Converter 1's regulation fails, the +15 volt line may increase to 22V and trip the latch. However, Converter 1 also outputs the +135V B+ that is monitored for OVP and OCP and is connected to the failure indicator circuitry. Since the B+ is more closely monitored for OVP and OCP, it is more likely that the B+ will trip the latch before this zener will.

Surge relay RY5502 not energized

The surge relay RY5502 must engage shortly after the AC relay to bypass the surge resistor R5502 or the resistor will over dissipate. To prevent this, the TV will shut down if R5502's coil is not energized.

Normally when RY5502's coil energizes, 4 volts is developed across R5512. This is more than sufficient to back bias D5510 and keep the latch from tripping. The latch trips when the set is powered and the surge relay coil is not energized. Both ends of R5512 are now at ground potential and that turns ON the latch by bringing Q5504/base to ground via D5510.

Zener diode D5511 shuts down the TV if the surge relay coil shorts. The short will place 17Vdc at D5512's anode. This avalanches D5511, increasing the voltage at the base of latch transistor Q5503. When it turns on, the latch trips and the AC relay is de-energized, shutting off the TV. Other inputs to this latch on the G board are shown in the Protection Circuit 2 diagram.



PROTECTION CIRCUIT 1

HDTV13 1046 2 24 99

Protection Circuit 2

The remainder of the protection sensing circuitry on the G board is shown in this diagram. It monitors the following items:

- +5V OCP
- +5V OVP
- +135V OCP
- +135V OVP

The output of these four sensing circuits triggers two stages:

1. The latch circuit on the G board to shut down the TV.
2. The Main Micro for a visual indication of the section that caused the protection.

+5V OCP

The +5 volts from Converter 2 is monitored by this circuit for excessive current. The +5V from D5041 passes through both R5038 and R5076 connected in parallel. If the voltage dropped by these resistors exceeds 0.6Vdc, Q5019 conducts and raises the voltage at its collector. This voltage turns on Q5018, which turns on Q5017. A high is output Q5017's collector that takes two paths:

- Through D5047 to the protect latch, shutting off the TV; as well as
- Through D5046 to the Main Micro IC3251/pin 43 to blink the standby light six times, pause and repeat.

Q5019 Normal DC Voltages		
Emitter	Base	Collector
+5.23V	+5.14V	0V

Excessive current means that there is a shorted part on a board powered by the +5V line. In searching for the load, never unplug an M board connector when there is +135V present on the G board or the G board's H. Driver Q4011 and PWM Driver Q4003 will short.

+5V OVP

The +5 volts is also monitored for excessive voltage by zener D5042. If the +5 volt line rises above the 6.2V zener voltage, a voltage is applied to amplifier Q5018 and Q5017 to shut down the TV and blink the light six times. A higher voltage at the +5V line means that Converter 2 is not regulating. Measure the +5V line with a peak hold DVM to verify the over voltage.

135V OCP

The +135V OCP circuit is similar to the +5V OCP circuit. The +135 volts from Converter 1 is monitored by this circuit for excessive current. The +135V from D5015 passes through both R5026 and R5101. If the voltage dropped by these resistors exceeds 0.6Vdc, Q5009 conducts and raises the voltage at its collector. This voltage turns on Q5020, which turns on Q5016. A high is output Q5016's collector that takes two paths:

- Through D5022 to the protect latch, shutting off the TV
- Through D5013 to the Main Micro IC3251/pin 44 to blink the standby light two times, pause and repeat

Excessive current demand on the +135V line can be caused by: Horizontal Output Transistor Q4018, FBT 7001, Pincushion Output MOSFET Q4027, or Dynamic focus correction Q7009 and Q7012.

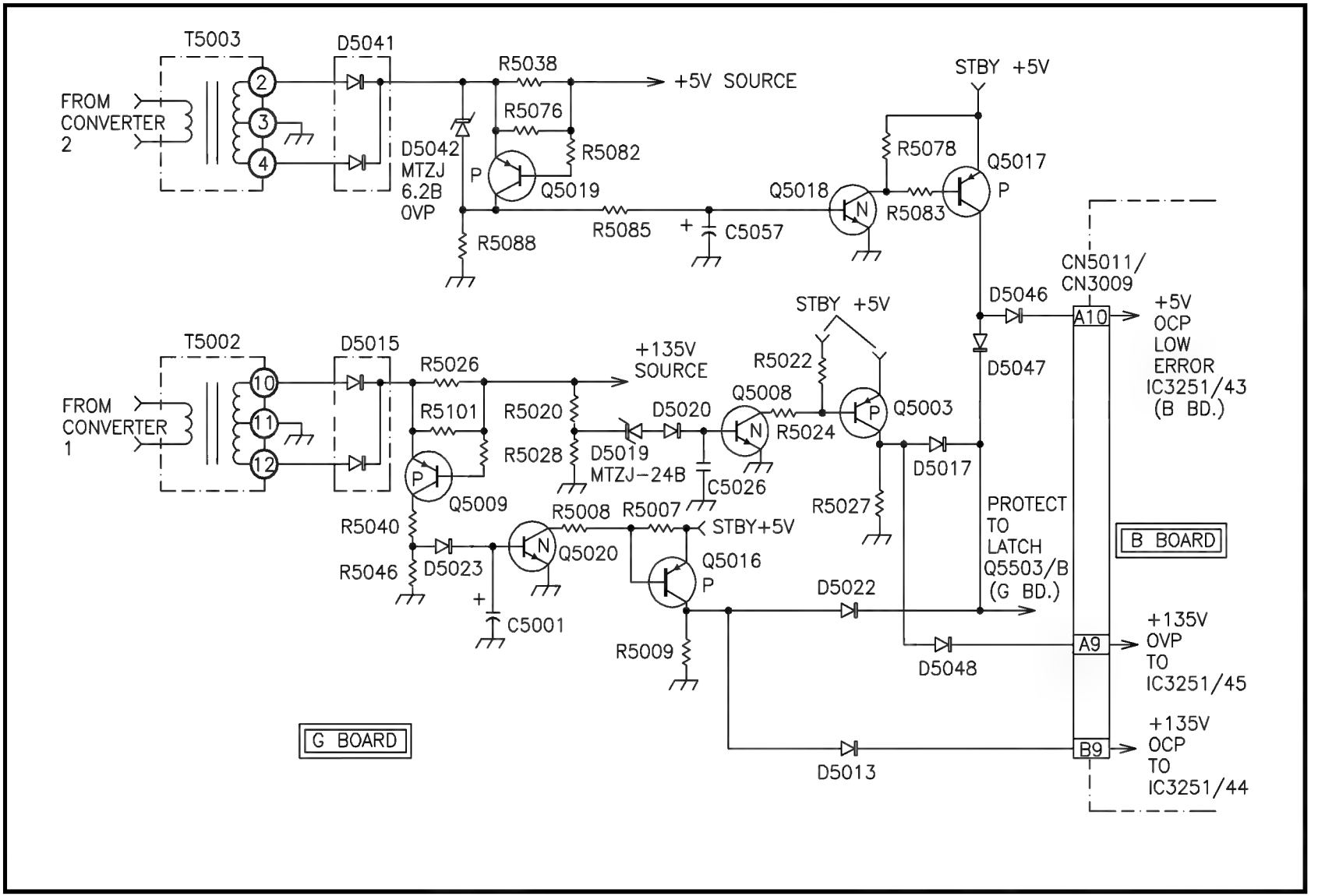
135V OVP

These parts forming the sensing circuit perform the +135V excessive / over voltage protection (OVP):

+135V OVP Parts		
Device	Normal state	Purpose
D5019 – 24 volt zener	No conduction	Watches the +135V line voltage divided by R5020 & R5028.
Q5008 – NPN	OFF	Amplifies the input (sw)
Q5003 - PNP	OFF	Amplifies the input (sw)

An excessive +135V B+ breaks over the zener and turns on both Q5008 and Q5003 transistors on to apply voltage:

- Through D5017 to the protect latch, shutting off the TV; as well as
- Through D5048 to the Main Micro IC3251/pin 45 to blink the standby light three times.



PROTECTION CIRCUIT 2

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Protection Circuit 3

The shutdown latch and the general sensing circuitry are located on the G board. These circuits sense general failures such as +5 and +135 excessive voltage and current. When a general failure occurs, the Main Micro IC3251 causes the standby light to blink, indicating one of these failures. See the Overall Protection Block.

The remainder of the sensing circuits are found on the D board. They monitor specific power handling circuits on this board. Although the D board sensing circuitry also shuts down the TV when there is a problem, there is no communications to the Main Micro. There is no visual (standby light blink) indication of the problem area. Therefore, if the TV shuts down without a visual indication, the problem is likely to be on the D board.

The sensing circuitry on the D board monitors the following:

- **Driver supply voltage OVP**
- H. Output OCP
- H. Output Supply OVP
- FBT Output OVP
- **H Centering IC4003 OCP**

The items in bold are shown in this simplified Protection Circuit 3 diagram. The remaining ones are in Protection Circuit 4 diagram.

Driver supply voltage OVP Circuit Operation

The horizontal driver stage receives supply voltage from a PWM circuit. This PWM circuit not only regulates its own output voltage, but also changes the voltage to increase picture width when required. Since a failure in the PWM circuit would result in excessive scan current, the PWM voltage is monitored.

Driver Supply Voltage OVP Sensing Circuit		
Parts	Normal Condition	Purpose
R4011, R4008, R4012 voltage divider		Samples the PWM driver supply voltage
Q4001	ON	Keeps Q4005 ON
Q4005	ON	Keeps output at 0Vdc

Initially, both Q4001 and Q4005 are turned ON when current flows from +12V through Q4001/e-b, R4009, R4008 and R4012 to ground. When Q4005 is ON, its collector voltage is at 0Vdc so the shutdown path ends here.

A sample of the PWM driver voltage is taken from Q4003/collector via R4011 and applied to Q4001's base. This voltage is normally not high enough to turn OFF Q4001, so both Q4001 and Q4005 remain ON.

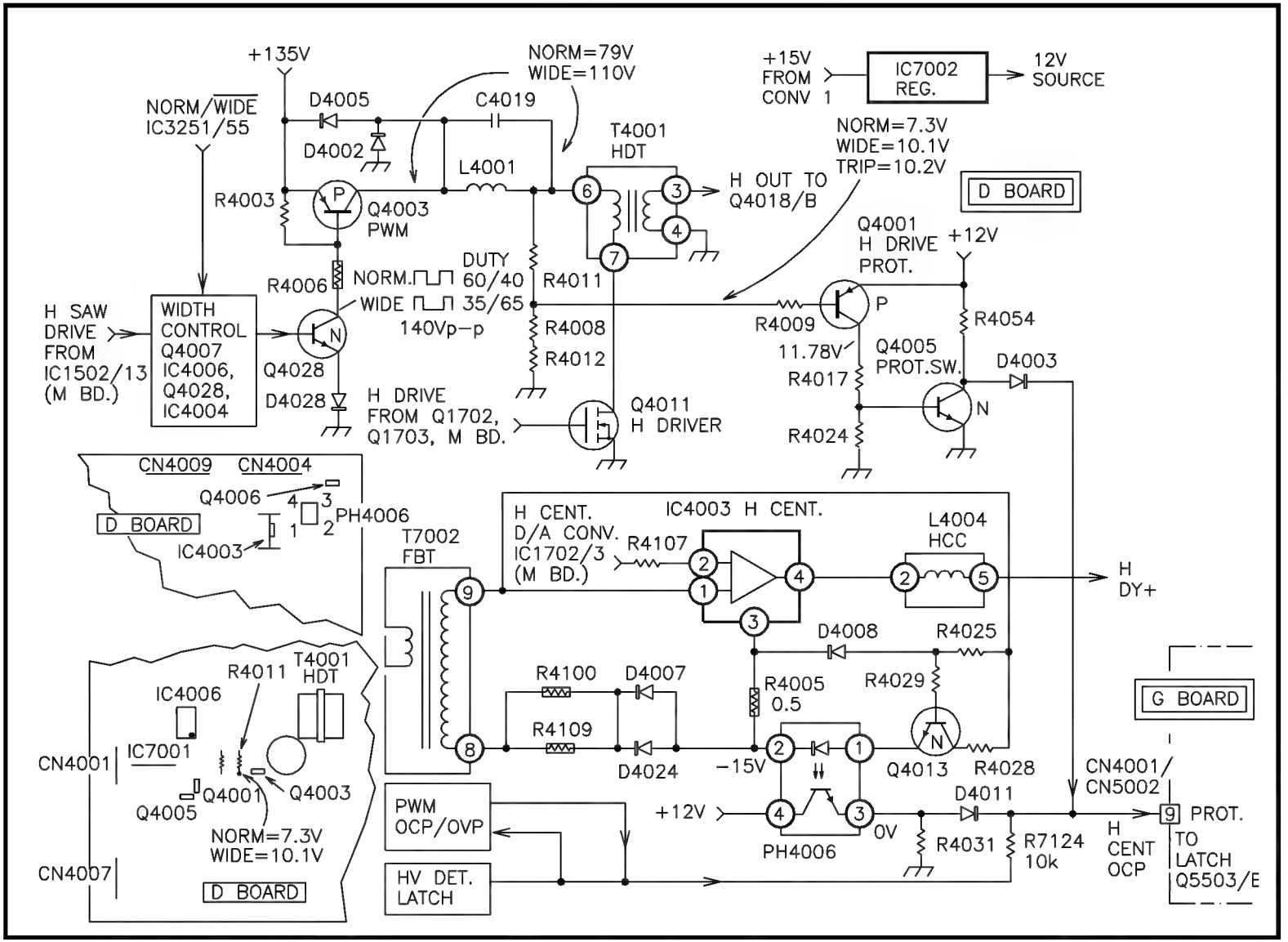
An excessive level of PWM driver voltage would cut off Q4001, causing Q4005's collector to rise. This is applied to the latch circuit on the G board (CN5002/pin 9) which causes the TV to shut off.

H Centering IC4003 OCP Circuit Operation

In this Sony model KW34HD1 TV, the user can center the picture from the menu. This centering circuit consists of a driver IC4003 that performs this function by adding DC voltage to the yoke. IC4003's failure could send a substantial current through the yoke so its current consumption is monitored as it enters IC4003/pin 3. The parts used in this OCP circuit are:

H Centering IC4003 OCP Sensing Circuit		
Parts	Normal Condition	Purpose
R4005 @ IC4003/3	0.1V across R4005	Current sensing
Q4013	ON - 0.024V across R4028	Sets the PH4006 photodiode threshold by prebiasing it.
PH4006	OFF	Couples the OCP signal without interference from IC4003's floating ±15V supply.
D4011	OFF (0V on both sides)	Output blocking diode

The yoke receives signals from both the + and – ends and therefore floats above ground. The horizontal centering signal is applied to the yoke via IC4003. The centering IC4003 is powered by ±15V from a FBT winding so this secondary floats as well.



PROTECTION CIRCUIT 3

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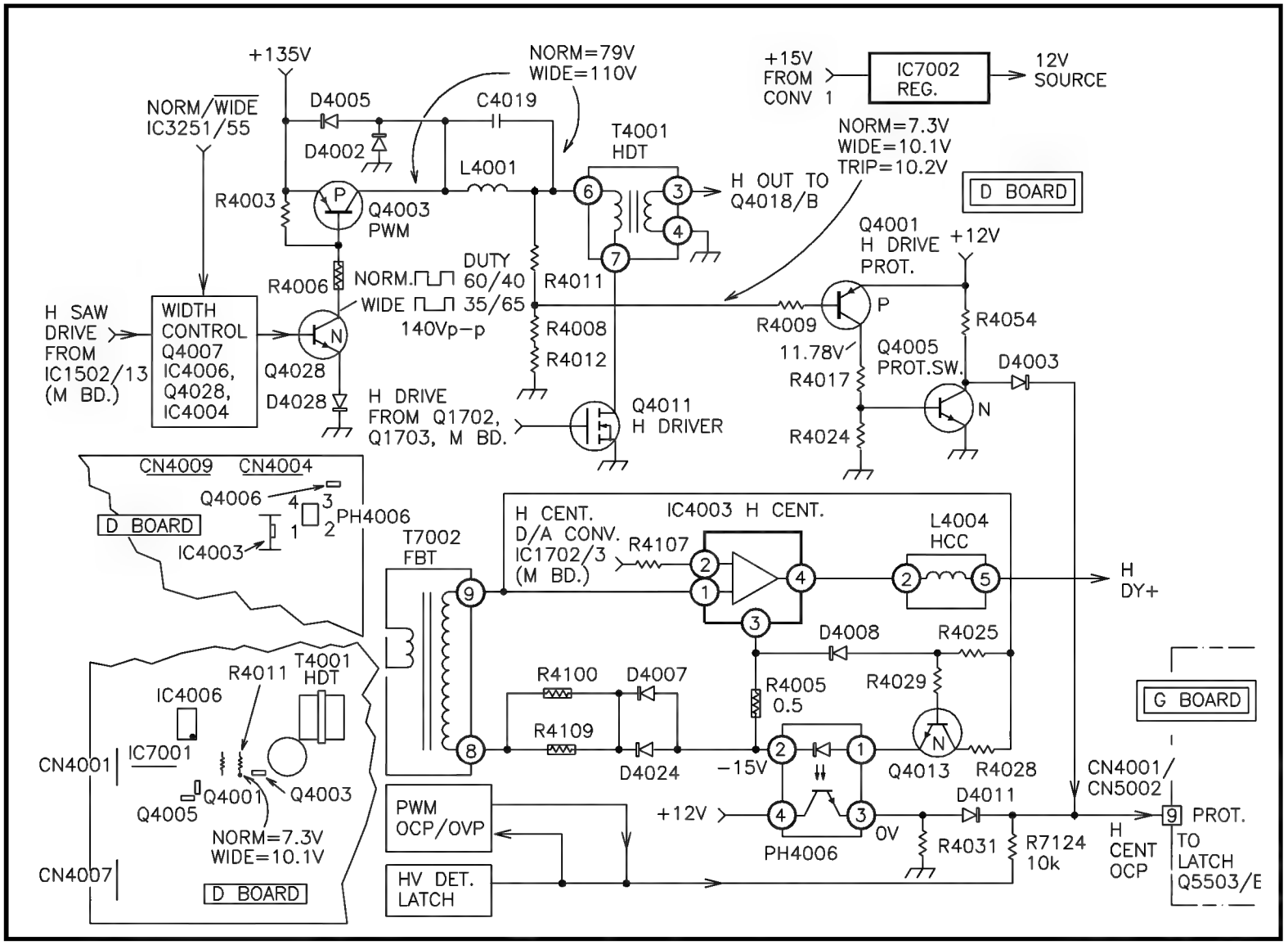
PH4006 is used to monitor IC4003's current and couple the excessive current protection signal to the protection latch that is referenced to ground. The current from the –15V supply passes through R4005 into IC4003/pin 3. The voltage dropped by R4005 is applied to Q4013, D4008 and the photodiode in PH4006. Q4013 prebiases the PH4006 photodiode and D4008 references this voltage to one end of R4005. The other end of R4005 is connected to the photodiode PH4006. Excessive current through IC4003 will increase the voltage drop across R4005. This increased voltage turns on the photodiode and the PH4006 phototransistor will conduct. Its conduction applies voltage to trip the protection latch and the TV shuts off. In normal operation though, the photodiode never turns ON and there is 0V at both sides of D4011.

D board Circuit Failure Detection

If the unit shuts down, but the standby light does not blink, the problem is in one of the seven remaining areas that are not monitored by IC3251. Five of these items are on the D board. Two of these items are shown in the Protection Circuit 3 diagram. However, all five items are checked in this procedure:

1. Monitor the shutdown trigger voltage at the D board connector CN4001/ pin 9. If this voltage rises above the normal 0.3V to about 1.3V, the problem is caused by one of the sensing circuits on the D board.
2. Locate Q4005/collector (middle lead). Monitor the voltage at this point as you turn on the set and it shuts down. Normally this point will rise to 0.022V. If it continues to rise to the trip point of 1.3V, the problem is excessive driver PWM voltage from Q4003 or the Q4001/Q4005 sensing circuit is defective. (Protection circuit #3 diagram)
3. Locate the photo coupler PH4006/pin 3 and monitor its voltage as you turn on the TV and it shuts down. The normal voltage here is 0V. If it rises to the trip point of 1.5V, the problem is a shorted IC4003 centering IC. (Protection Circuit 3 diagram).
4. Locate Q7003/collector (middle lead) or the anode of D7102 and monitor its voltage as you turn on the TV and it shuts down. The normal voltage here will not rise above 0V. If it rises to the trip point of 1.5V, the problem is excessive current to the PWM regulating circuit, FBT or Horizontal Output Transistor. (Protection circuit #4 diagram)
5. Locate IC4004/pin 14 and monitor its voltage as you turn on the TV and it shuts down. The voltage here will rise to +8.35V and stay there. If it rises and comes down just before shutdown, the problem is excessive voltage from the horizontal output PWM stage possibly caused by a shorted Q4022 PWM Output MOSFET or the IC4004, D7029, Q7001 and Q7003 sensing circuit. (Protection Circuit 4 diagram)
6. Locate IC7001/pin 8 and monitor its voltage as you turn on the TV and it shuts down. The normal voltage here will not rise above 0V. If it rises to the trip point of 1V, the problem is excessive FBT voltage. A possible defect is an open resonate capacitor in the Horizontal Output Transistor's collector circuit.
7. If all these voltages are normal, yet CN4001/pin 9 rises to 1.3Vdc, the problem is on the D board and Q4050 is probably defective (Protection circuit #4 diagram). This is because it is the only part not yet checked.



PROTECTION CIRCUIT 3

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Protection Circuit 4

The shutdown latch and general sensing circuitry are located on the G board. These circuits sense general failures. The Main Micro IC3251 causes the standby light to blink, indicating the circuit at fault.

The remainder of the sensing circuitry is found on the D board monitors specific power handling circuits on this board. Although the D board sensing circuitry also shuts down the TV when there is a problem, there is no communications to the Main Micro so there is no blinking light to indicate the problem area. Therefore, if the TV shuts down without a blinking light indication, the problem is likely to be on the D board.

The sensing circuitry on the D board monitors the following:

- Driver supply voltage OVP
- **H. Output OCP**
- **H. Output Supply OVP**
- **FBT Output OVP**
- H Centering IC4003 OCP

The items in bold are shown in this simplified Protection Circuit 4 diagram. The remaining ones are in the previous diagram.

H. Output OCP Circuit Operation

Resistors R7062/R7022 and transistor Q7003 parts perform current sensing. The current drawn by the Horizontal Output stage passes through resistors R7062 and R7022. The normal voltage dropped across them is shown in the chart below.

Voltage Across Parallel Resistors R7062 & R7022	
Generator picture	R7062 & R7022 Voltage
Black Raster	0.345V
White Raster	0.58V

If the horizontal output current increases, the voltage dropped across these resistors rises. If they rise to a dangerous level of 0.6Vdc, Q7003 turns ON and a positive voltage outputs its collector. This passes through blocking diode D7102 and trips the shutdown latch on the G board. Excessive current consumption can be caused by a shorted PWM MOSFET Q4022, shorted T7002 FBT, leaky Q4018 or just a high screen control adjustment.

H. Output Supply OVP Circuit Operation

The PWM B+ regulating circuit supplies voltage to the Horizontal Output Transistor Q4018. The following parts monitor this supply voltage:

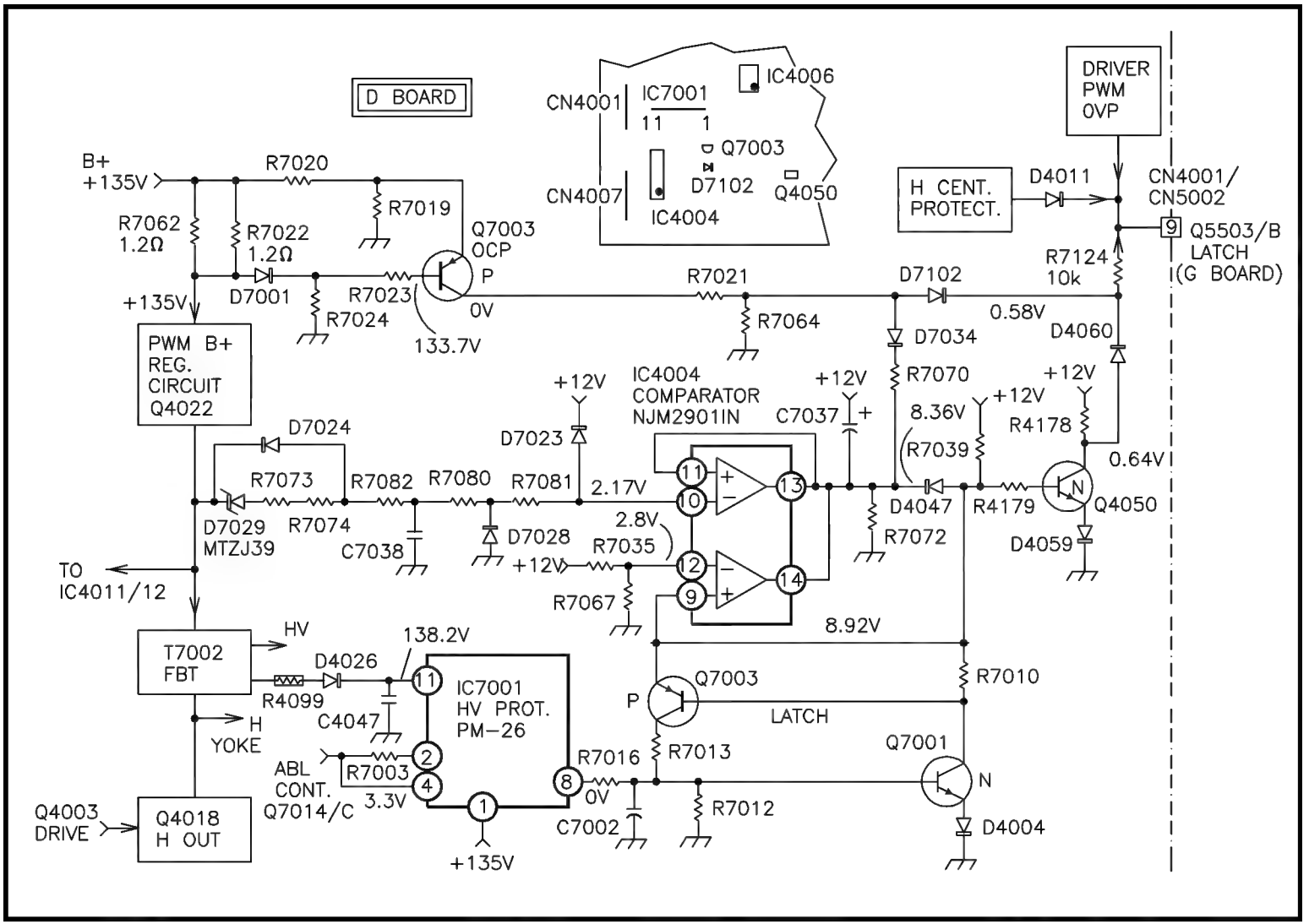
H. Output Supply OVP Circuit		
Parts	Normal Condition	Purpose
39V zener diode D7029	Cathode = 108Vdc Anode = 38Vdc	
Resistor string R7073-4,R7080-2		Series dropping resistors
C7038	2.17V	Filter capacitor
IC4004	Pin 13 output = 8.35V	Hysteresis Comparator
Q4050	ON	Inverter

At turn on, PWM pulses from Q4022 are rectified by D7024 and produce a low voltage at IC4004/pin 10. This results in an 8.35Vdc high at the pin 13 output.

If the PWM pulses become excessive or if Q4022 shorts, the higher voltage output will break over zener D7029 and be applied to IC4004/pin 10. When pin 10's voltage exceeds the 8.35Vdc reference at IC4004/pin 11, its output at pin 13 will go to 0V. This will forward bias D4047 and turn off Q4050, producing a high at its collector. The high is applied through D4060 to the latch circuit on the G board, which shuts down the TV.

FBT Output OVP

A flyback transformer T7002 secondary is used to represent the FBT outputs. It is monitored for excessive voltage. This voltage is rectified by D4026 and applied to HV protection IC7001 for comparison to an internal reference voltage. If the input voltage is exceeded, IC7001/pin 8 will output a 1-volt high, tripping the Q7001/Q7003 latch. The latch grounds the +12V from the FBT that forward biased the base of Q4050. This turns the transistor OFF so voltage can be applied through D4060 to the G board latch that shuts down the TV.



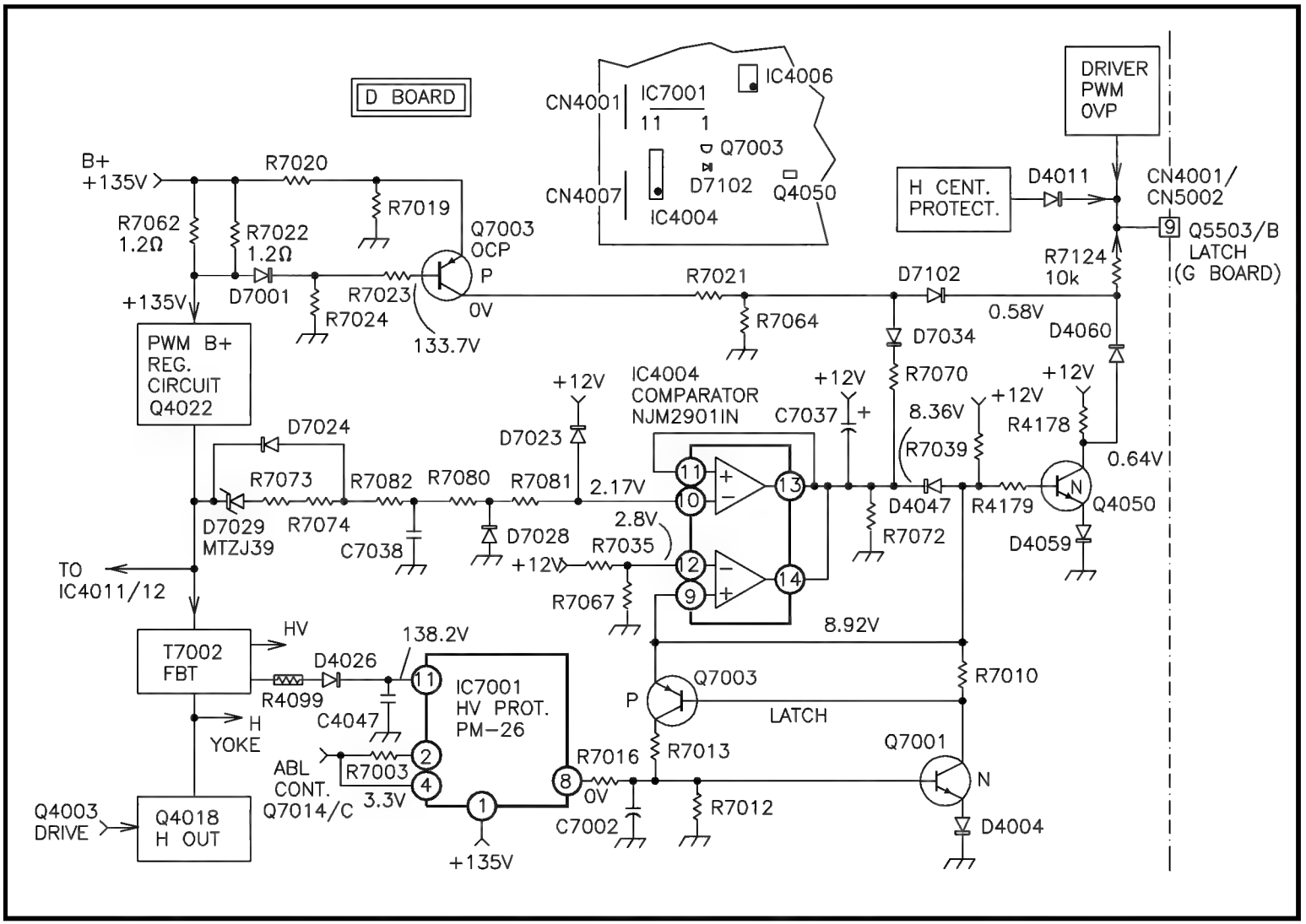
PROTECTION CIRCUIT 4

HDTV16 1051 3 9 99

D board Circuit Failure Detection

If the unit shuts down but the standby light does not blink, the problem is in one of the seven remaining areas that are not monitored by IC3251. Five of these items are on the D board. Three of these items are shown in Protection Circuit 4. However all five items are checked in this procedure:

1. Monitor the shutdown trigger voltage at the D board connector CN4001/ pin 9. If this voltage rises above the normal 0.3V to about 1.3V, the problem is caused by one of the sensing circuits on this D board.
2. Locate Q4005/collector (middle lead). Monitor the voltage here as you turn on the set and it shuts down. Normally this point will rise to 0.022V. If it continues to rise to the trip point of 1.5V, the problem is excessive driver PWM voltage from Q4003 or the Q4001/Q4005 sensing circuit is defective. (Protection Circuit 3 diagram)
3. Locate the photo coupler PH4006/pin 3 and monitor its voltage as you turn on the TV and it shuts down. The normal voltage here is 0V. If it rises to the trip point of 1.5V, the problem is a shorted IC4003 centering IC (Protection circuit #3 diagram).
4. Locate Q7003/collector (middle lead) or the anode of D7102 and monitor its voltage as you turn on the TV and it shuts down. The normal voltage here will not rise above 0V. If it rises to the trip point of 1.5V, the problem is excessive current to the PWM regulating circuit, FBT or Horizontal Output Transistor (Protection circuit #4 diagram).
5. Locate IC4004/pin 14 and monitor its voltage as you turn on the TV and it shuts down. The voltage here will rise to +8.35V and stay there. If it rises and comes down just before shutdown, the problem is excessive voltage from the horizontal output PWM stage caused possibly by a shorted Q4022 PWM Output MOSFET or the IC4004, D7029, Q7001 and Q7003 sensing circuit (Protection Circuit 4 diagram).
6. Locate IC7001/pin 8 and monitor its voltage as you turn on the TV and it shuts down. The normal voltage here will not rise above 0V. If it rises to the trip point of 1V, the problem is excessive FBT voltage. A possible defect is an open resonate capacitor in the Horizontal Output Transistor's collector circuit.
7. If all these voltages are normal, yet CN4001/pin 9 rises to 1.3Vdc, the problem is on the D board and Q4050 is probably defective (Protection Circuit 4 diagram). This is because it is the only part not yet checked.



PROTECTION CIRCUIT 4

HDTV16 1051 3 9 99

Vertical Deflection

The purpose of this stage is to:

- Manufacture a 60Hz vertical sawtooth signal to drive the yoke for vertical (downward) beam deflection.
- Synchronize the vertical drive signal to the station's vertical frequency.
- Monitor the output signal for linearity correction.
- Immediately stop horizontal drive and have the TV shut down if there is a loss of vertical output signal.

This vertical deflection stage consists of two signal paths:

1. The vertical output
2. The vertical feedback

Vertical Output

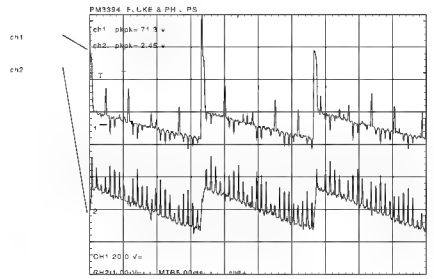
There are only a few stages of drive operation to make and amplify the vertical signal to drive the deflection yoke. The yoke creates the magnetic field to move the electron beam downward at a 60 Hz rate.

Vertical Signal to the Deflection Yoke			
Device	Input	Output	Purpose
Digital Deflection Control IC1305	+5V – pins 34, 43 Station sync Sample of the output signal	VD + /pin 21 VD - /pin 22	When +5V power is applied, sawtooth signal is output. Sample of the output signal is returned for frequency and linearity correction and proof of activity.
Vertical Output IC7003	Differential input - pins 1 and 7. Boost voltage – pin 6.	Vertical sawtooth output at pin 5.	Current amplifier to drive the low impedance yoke. Makes its own boost voltage used during vertical retrace time.

When +5V is applied, the vertical drive signal is made in IC1305 and output as an out-of-phase signal pair from pins 21 and 22. Each signal output is 2Vp-p.

The differential (out of phase) output signals are sent on long signal runs (to a different board) to take advantage of common mode rejection. When the same interference is picked up on both signal lines, one line can be inverted and added to the other to cancel the noise. The output signal level is added since they were originally complementary.

The vertical output IC7003 gets sufficient current from the ±15V supply to amplify the 2Vp-p input signal to 70Vp-p and drive the low impedance (12.1 ohms) yoke. The following output waveform shows the yoke's drive and return voltage.

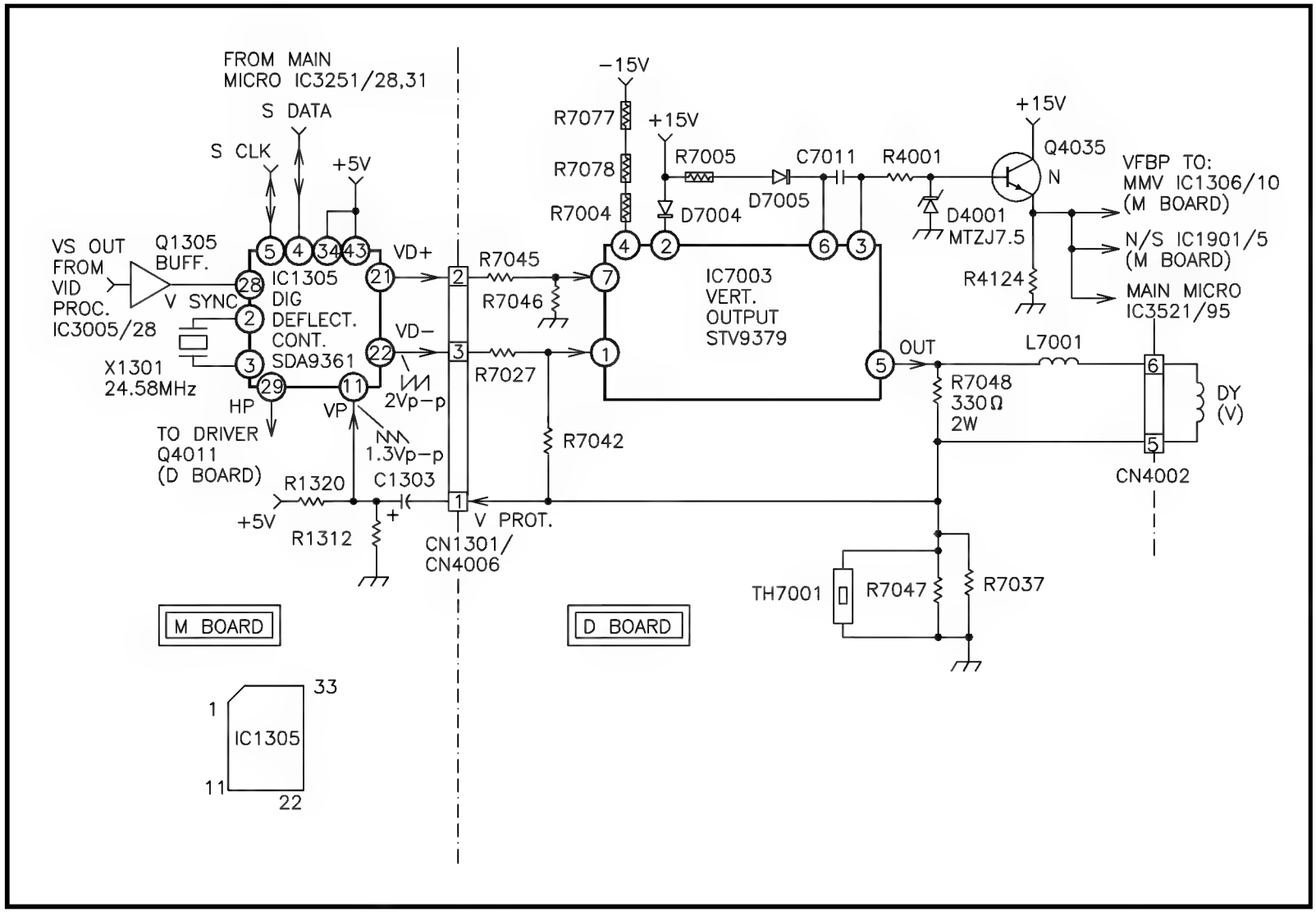


Waveform VD – Vertical Yoke signal			
	Name	Location	Voltage/div
Channel 1	Vert Output	CN4002/pin 6	60Vp-p
Channel 2	Vert return	CN4002/pin 5	2.45Vp-p
Time base	5msec/div		

IC7003 Flyback Generation

The vertical output signal is 60Vp-p from IC7003, but the supply voltage is only ±15Vdc. Examination of the output waveform (ch 1) shows that only the large retrace spike exceeds the 30-volt supply voltage.

The supply voltage necessary to meet the need during the retrace interval (when there is a large spike) comes from a "flyback generator" within IC7003. IC7003's flyback generator first uses the retrace portion of the input signal to make a 0.5msec pulse, then amplifies it to 30Vp-p (supply



VERTICAL DEFLECTION

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voltage limits). This pulse is output at IC7003/pin 3 and coupled by C7011 to pin 6. The pulse boosts the +15Vdc Vcc at pin 6 to the amplitude of the pulse. This method of developing the higher Vcc avoids having a large B+ supply voltage source that is not used most of the time. A loss of boost voltage seems to cause no vertical deflection in most sets.

Vertical Feedback Signal

The return end of the yoke at CN4002/pin 5 is grounded through low value resistors and a thermistor TH7001 for temperature compensation. The small signal that is developed across these resistors is AC coupled and fed back to IC71305/pin 11 for three purposes:

1. Linearity correction
2. Frequency correction
3. Picture tube protection

Linearity correction

Linearity correction takes place within IC1305 when the manufactured vertical signal is compared to the signal returned at pin 11. In addition, linearity and size corrections are performed from the service mode adjustments. The adjustments are input to IC1305 as serial data from the main micro (but the information is actually stored in an external memory).

Station Sync

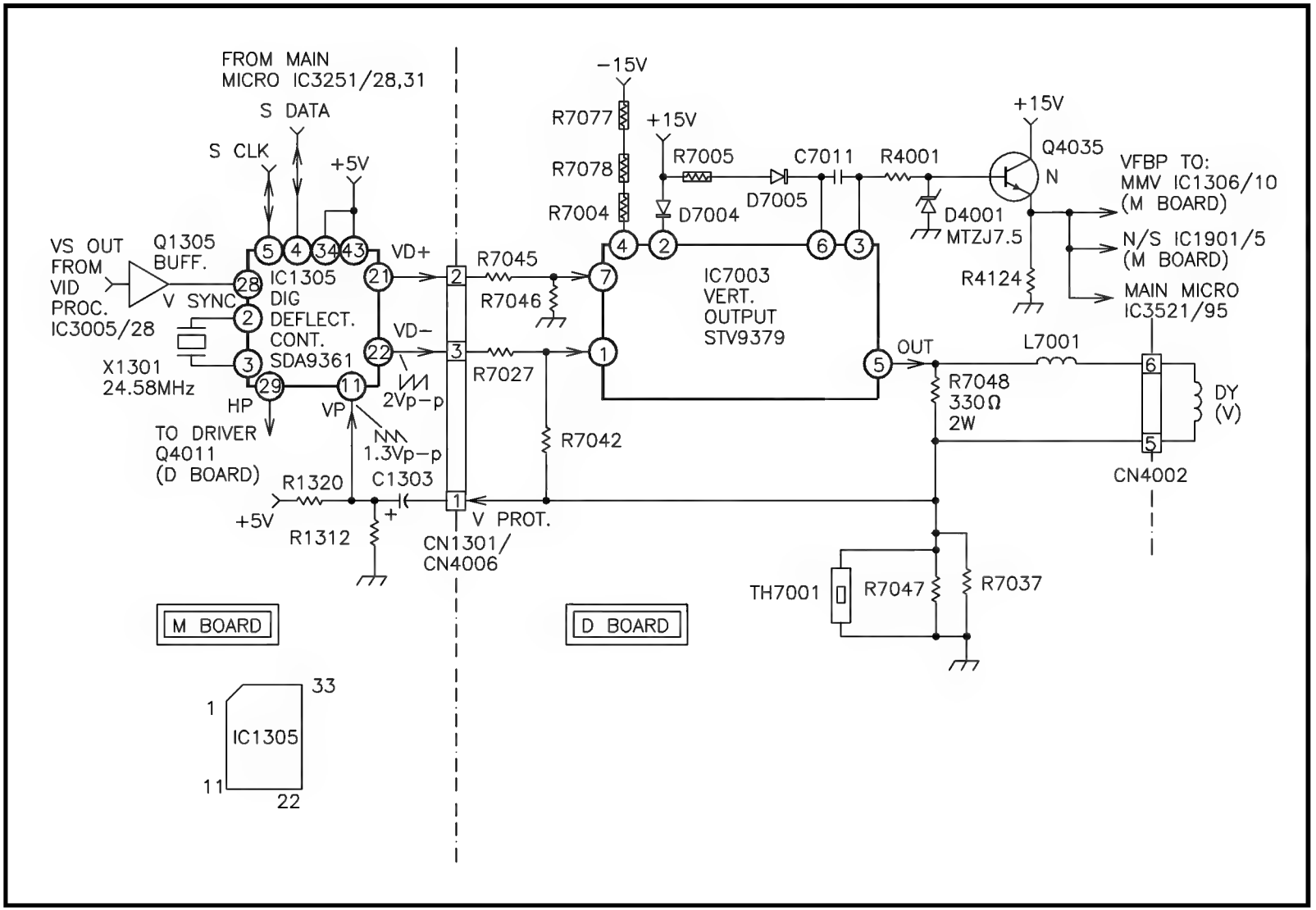
The frequency and phase of the VD signal output IC1305 must be the same as the station's vertical signal. Two inputs are used to accomplish this. One input is the station sync that comes into IC1305/pin 28. The second input is the sample of the vertical oscillator signal that enters IC1305/pin 11. The two inputs are compared in IC1305 and the frequency and phase of the vertical oscillator is corrected to match.

Picture tube protection

If there is a loss of vertical deflection, the picture would collapse. The scanning lines would be concentrated at the center of the screen (if there was no DC voltage to offset or move the beam). This would instantly damage the picture tube. To avoid this the vertical feedback signal is also used for protection.

A loss of vertical signal for two fields (1/30 second) into IC1305/pin 11 causes the IC to stop the horizontal drive output from pin 29. Therefore if there is a loss of horizontal drive signal from IC1305/pin 29, even though there is +5Vdc applied to the IC1305 at pins 34 and 43, check the vertical feedback signal path.

While this is occurring, serial data is output IC1305 to tell the main micro to shut off the TV set and blink the standby light. The light will blink four times, pause, and then repeat over and over until the set is unplugged or the front panel master power button is pressed.



VERTICAL DEFLECTION

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Horizontal Deflection Block

Both the horizontal driver and output stages have individual PWM stages that supply regulated B+ voltage to them. The H. output B+ comes from the PWM stage through the flyback.

This horizontal deflection block has several stages:

1. Horizontal Driver/Output stage feeds the FBT and H yoke.
2. Driver PWM stage controls the Driver transistor B+.
3. H. Output PWM stage controls the H. Output transistor B+.
4. Horizontal Centering stage positions the picture.

Horizontal Driver/Output stage

Horizontal Driver/Output stage		
Sections	Major parts	Purpose
Digital Deflection Control IC	IC1305	Makes horizontal drive signals.
Buffers	IC1705, Q1702, Q1703.	Current to voltage driver and current limiter.
MOSFET Driver	Q4011	Voltage amplifier
H. Output Transistor	Q4018	High current output device

When the Digital Deflection Control IC1305 is powered, 31.5KHz horizontal and 60Hz. vertical pulses are output. In this set the horizontal pulses are buffered so there is sufficient current to supply the gate of the MOSFET horizontal driver. The horizontal driver amplifies the drive signal. The signal is transformer coupled to the horizontal output transistor (Q4018). The output transistor feeds the yoke for deflection and the flyback transformer for high voltage.

Driver PWM stage

Driver PWM stage		
Sections	Major parts	Purpose
Shaper	IC1502	Shapes the H drive pulse into a single spike.
Driver PWM	Q4003	1. Change the spike into a pulse, 2. Control the pulse width (PWM), 3. Filter the output into DC.

The purpose of this stage is to:

1. Make B+ voltage for the driver MOSFET.
2. Regulate this voltage.
3. Increase the B+ voltage when a wide picture is called for.

Horizontal Output PWM stage

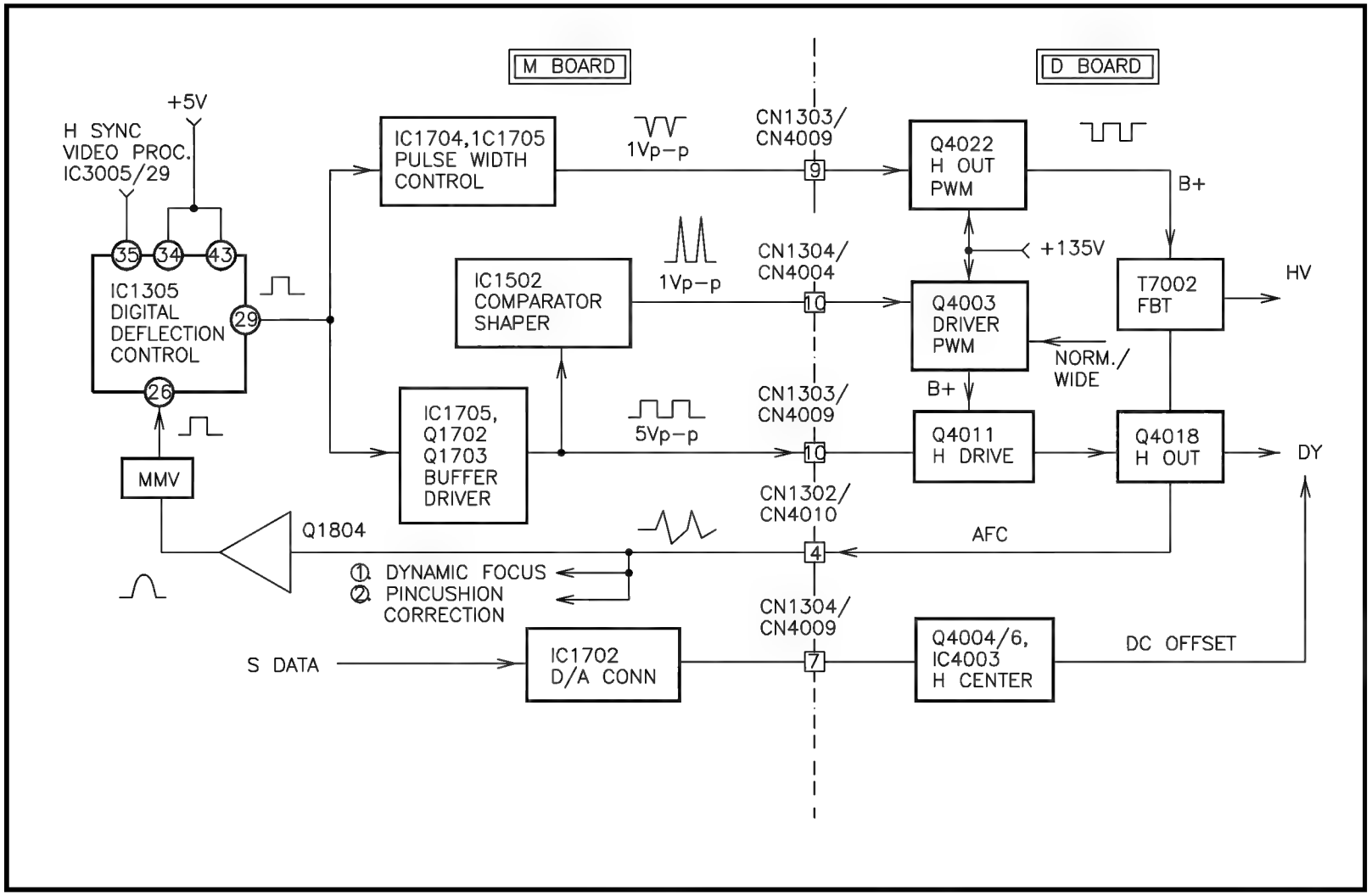
Horizontal. Output PWM stage		
Sections	Major parts	Purpose
Pulse width Control	IC1704, IC1705	Makes an output pulse of a fixed width regardless of the input frequency. Delays the pulse and uses it to insure rapid H Output transistor turn off.
H Output PWM	Q4022	Uses the pulse to develop B+ for the H. Output transistor. Regulates this B+ voltage to assure stable picture width and brightness. Changes the B+ slightly to adjust for a different horizontal frequency.

The pulse width control block makes a pulse that can be adjusted. At the higher horizontal frequency, it is important that the horizontal output transistor be turned off before the next cycle. To insure this will take place, a delayed pulse is used to lower the H. Output transistor's collector voltage after turn on.

The H Output PWM block also adjusts the B+ voltage to compensate for the slightly higher horizontal frequency used in HDTV reception.

Horizontal Centering stage

This stage only consists of three blocks. The Main Micro IC (not shown) sends serial data to D/A converter, IC1702 to output a DC voltage. This DC voltage is amplified by the H Center block, which applies it to the yoke. This offset voltage is used to center the picture by keeping a constant magnetic field in the yoke windings which positions the electron beam to the left or right. The amount of shift is dependent upon the magnitude of the voltage.



HORIZONTAL DEFLECTION BLOCK

HDTV23 1074 2 24 99

Horizontal Drive

Horizontal Driver / Output stage		
Blocks	Major parts	Purpose
Digital Deflection Control	IC1305	Creates horizontal drive signals.
Buffers	IC1705, Q1702, Q1703.	Current to voltage driver and current limiter.
PWM Shaper	IC1502	Shapes the H drive pulse into a single spike for PWM mfg.

Oscillator Manufacture and Sync

When powered, Digital Deflection IC1305 starts up the external X1301 24.58MHz crystal. Once oscillation occurs, the IC makes vertical and horizontal drive signals. Without sync, the oscillator runs at 31.1kHz. The horizontal drive signal leaves IC1305/pin 29 (as long as the vertical feedback signal at pin 11 is present - see Vertical Deflection). When station sync is received, the horizontal oscillator frequency is changed to 31.5kHz or 33.5kHz to match the signal received.

When a signal is received, its sync portion is squared into a 5Vp-p waveform by IC1302 and is input to IC1305/pin 35. The horizontal oscillator's frequency is fed back from the horizontal output transistor's collector to IC1306/pin 2. This signal is sent to a MMV (IC1306) that outputs a pulse when triggered. IC1306 prevents a double input pulse from shifting the horizontal oscillator frequency and produces a digital pulse that is accepted by the Digital Deflection IC1305 at pin 26.

The Digital Deflection IC1305 compares the sync signal input to pin 35 and the feedback signal input to pin 26. This locks the horizontal oscillator frequency to the station's sync.

Buffers

IC1705 eliminates any base noise in the horizontal drive signal. It performs this by comparing the input to a fixed voltage set by the R1743/R1745 voltage divider at IC1705/pin 8. Voltages above this threshold are allowed to pass and noise riding along the base line is not output pin 14. The comparator output signal is 12Vp-p.

Q1702 and Q1703 are buffers/drivers that provide a fixed current to drive the horizontal driver MOSFET device in the next stage (via CN1303/pin 10).

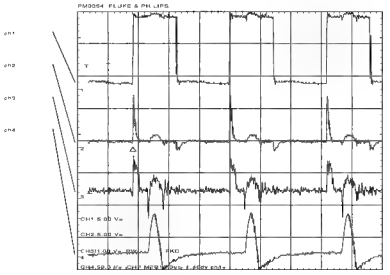
PWM Shaper

IC1502 is a comparator designed to shape the horizontal drive signal into a single pulse for the next PWM stage. The input of IC1502 is the horizontal drive signal and the output is a pulse that represents the leading edge of the input signal. This pulse is output CN1304/pin 10 and applied to the driver PWM stage.

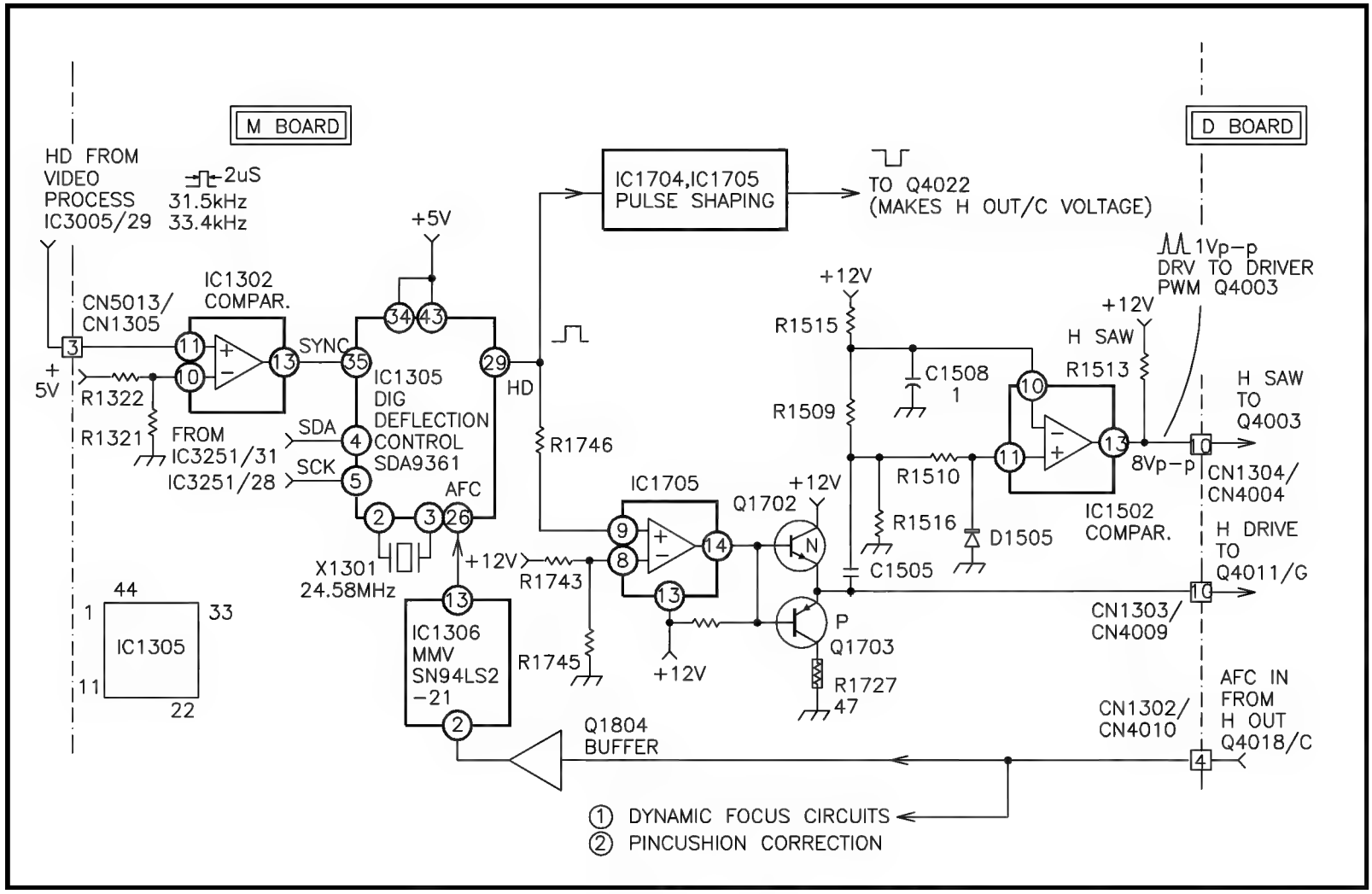
Operation:

C1505 couples the leading and training edges of the horizontal drive signal to IC1502/pin 11 (ch 2). Diode D1505 eliminates the negative or trailing parts of the signal, leaving only the leading edges present at pin 11 (ch 2). The comparator outputs this pulse (ch 3) when its input level is greater than the fixed voltage at IC1502/pin 10. The result is a positive pulse at the drive frequency. This pulse is used in the next stage to make B+ for the MOSFET driver device.

The waveforms show the signals input the comparator with a horizontal AFC feedback pulse (ch 4) for reference.



Waveform HD1e – IC1502 Comparator Operation			
	Name	Location	Voltage/div
Channel 1	H. Drive signal	CN1303/pin 10	12Vp-p
Channel 2	Cap coupled	IC1502/pin 11	9Vp-p
Channel 3	IC1502 output	CN1304/pin 10	1.5Vp-p
Channel 4	H. AFC	CN1302/pin 4	85Vp-p
Time base	10usec/div		



HORIZONTAL DRIVE

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Horizontal Driver

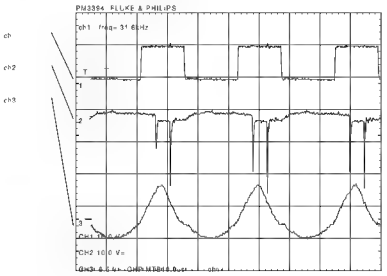
This horizontal driver stage consists of:

1. The horizontal driver MOSFET
2. The Driver PWM stage that makes B+ for the driver

Horizontal Driver MOSFET

A MOSFET horizontal driver is used to boost the horizontal drive level before applying the signal to the H Output stage. The horizontal drive signal from Q1703 is input to the gate and the amplified signal leaves Q4011's drain. The signal is coupled through T4001 to the Horizontal Output Transistor Q4018/base (not shown).

The horizontal drive signal can be seen in this scope shot showing the horizontal drive signal (ch 1) compared to the FBT pulse (channel 3).



Waveform HD22A – Horizontal Drive Signals			
	Name	Location	Voltage/div
Channel 1	H. Drive signal	CN4009/pin 10	12Vp-p
Channel 2	H. Output/base	Q4018/base	2Vp-p without spikes
Channel 3	FBT pulses	FBT	N/A
Time base	10usec/div		

MOSFET/Transistor Characteristic Comparison

A power MOSFET device in an N channel format is most similar to a NPN transistor in overall operation, just as a P channel device is similar to a PNP.

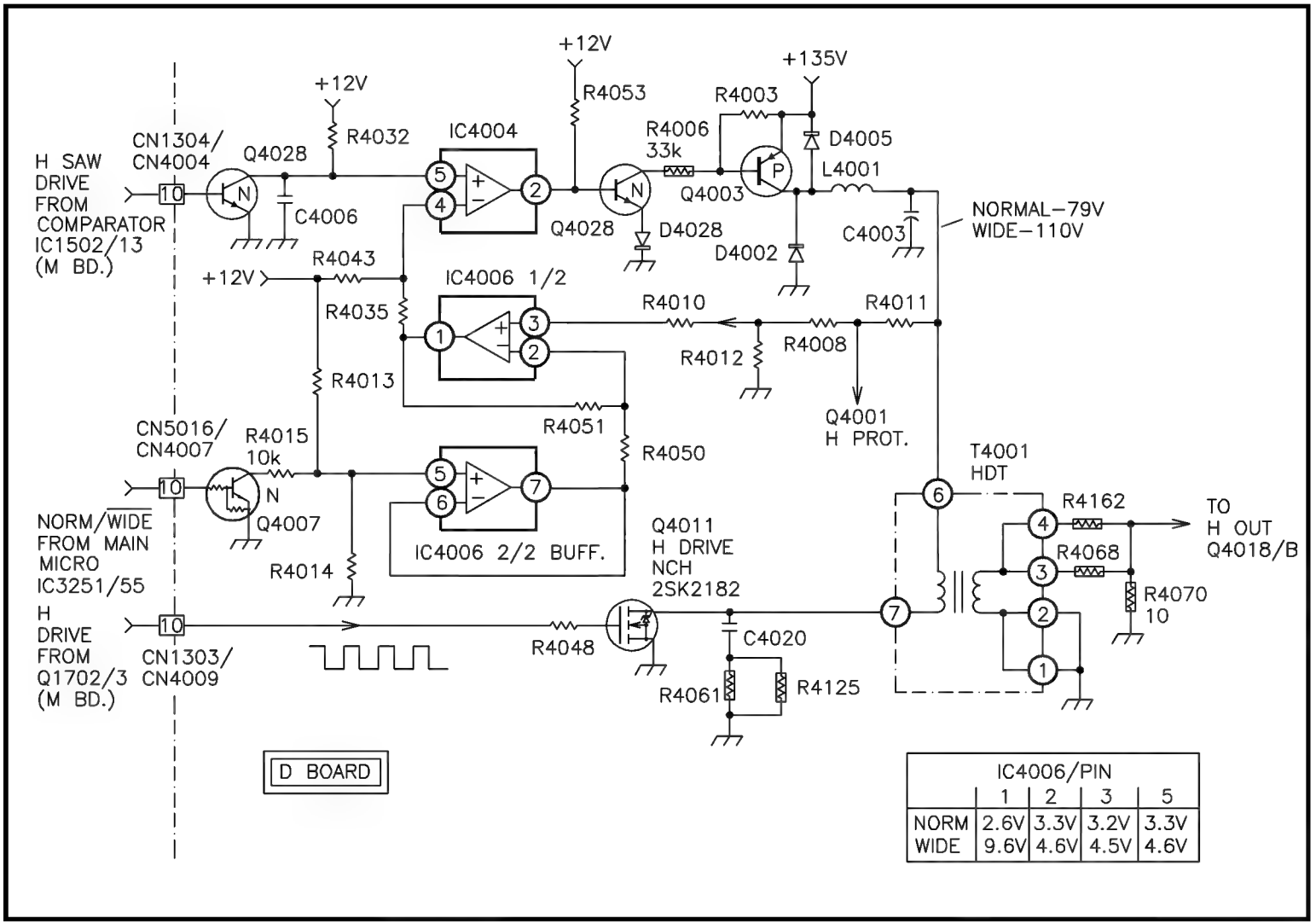
MOSFET – Transistor Operation Comparison	
Differences	Similarities
Maximum gate voltage can go to about +20 Volts with reference to the source lead.	The gate is referenced to the source, like the base is to the emitter.
Turn ON gate threshold voltage is 1-2V (low power) or 2-4V (high power TO-220 case or larger).	A gate voltage that is brought toward the drain voltage turns it ON, just like a base voltage being brought toward the collector potential turns a transistor ON.
On and OFF times are affected by internal gate capacitance so gate current determines ON time.	NPN and N channel are similar in circuit configuration. Summarily, so are PNP & P channel MOSFETs.
The OFF time is delayed by load capacitance that increases the gate capacitance (Cgd).	
In HV applications, a saturated MOSFET (drain to source is approx. 2V. This is greater than a transistor's Vce sat voltage.	
MOSFETs do not have thermal runaway and can therefore withstand simultaneous high current and voltage, but fails instantly when specs are exceeded.	
MOSFETs have lower high frequency switching losses	

Testing a MOSFET

Testing a MOSFET device is easy. The leads show infinite resistance to any other lead except for some power MOSFETs that have an internal protective zener connected between the drain and source.

To prove the device is functional:

1. Connect the negative lead of the ohmmeter to the SOURCE lead.
2. Touch the ohmmeter positive lead to the gate, to pre-charge it.



HORIZONTAL DRIVER

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3. Connect the ohmmeter positive lead to the DRAIN.
If the device is good you will get a resistance reading of about 400-1k ohms.

Driver PWM stage

The purpose of this stage is to make and regulate the driver's drain voltage (Q4011) using a processed PWM signal. In addition, the supply voltage can be increased to widen the picture to fill the screen. The higher drive voltage causes a larger signal that drives the output transistor harder. The increased collector current cause more yoke current to create a larger magnetic field to increase deflection and picture width.

This is series of processing steps that is used to make and control the PWM signal:

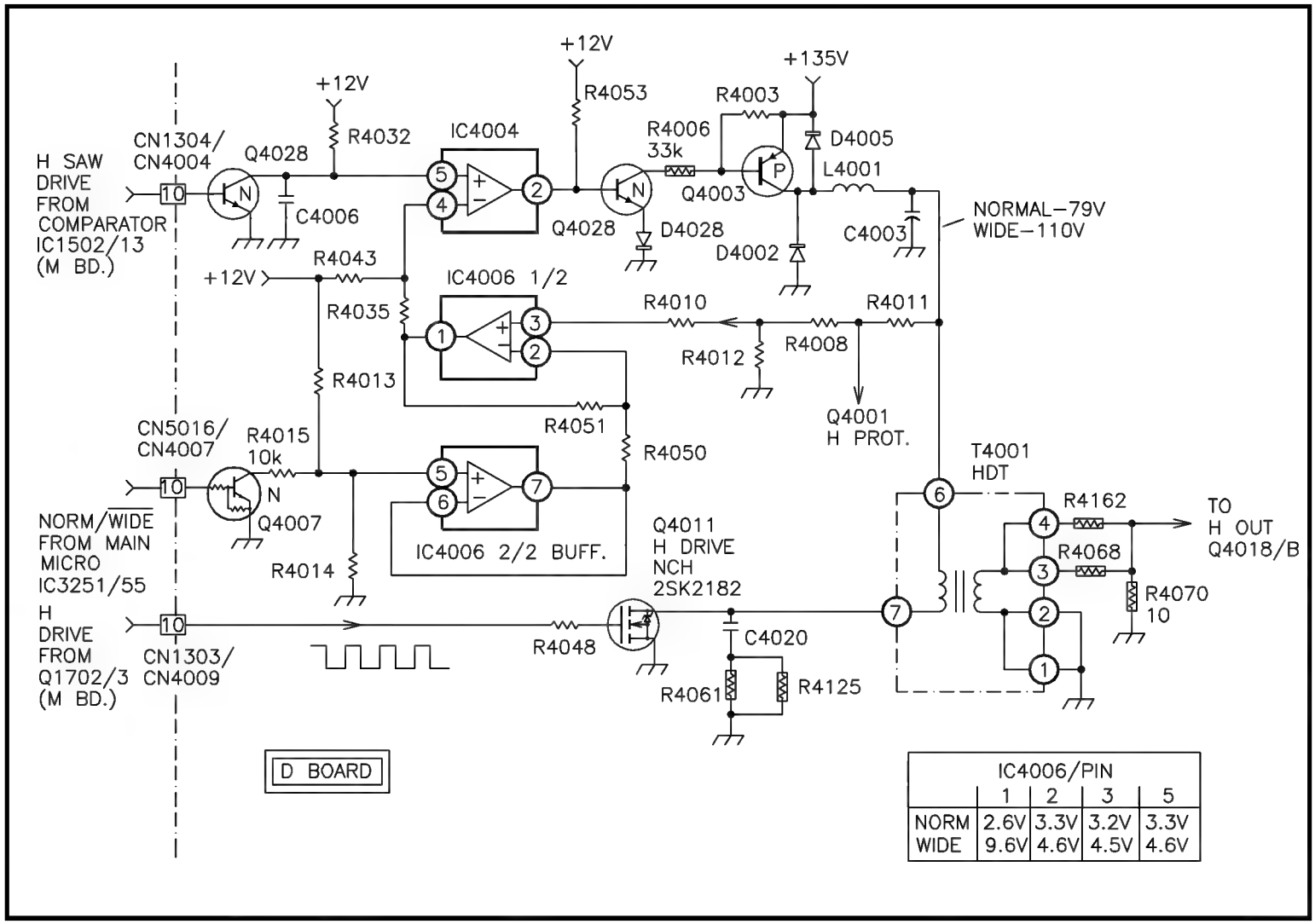
PWM Stage			
Device	Input	Output	Purpose
Q4028, C4006	CN1304/10 Positive pulse at the H. drive frequency	IC4004/5 - Ramp voltage	Makes a ramp voltage by charging C4006. Discharges with CN1304/10 pulse.
IC4004 comparator	Ramp voltage - pin 5 DC voltage – pin 6	IC4004/2 - Positive pulse	DC voltage input controls pulse width (PWM).
Q4028, Q4003	Positive pulse	Amplified pulse	Voltage / Current amp.
D4002, L4001, C4003.	PWM signal	DC voltage	Damper and low pass filter.
IC4006/pins 1-3	Sampled DC from voltage divider R4008, R4011, R4012 to IC4006/pin 3.	IC4006/pin 1 – DC voltage.	DC regulation.
Q4007, IC4006/pins 5-7.	CN4007/pin 10 5V = wide 0V = Normal picture width.	IC4006/pin 7 – DC voltage.	Pulse width control

In the previous stage a positive pulse is made and enters this stage from CN1304/pin 10. This pulse resets a ramp that is applied to IC4004. IC4004 makes another pulse from this ramp and the DC voltage at pin 4. Pin 4's DC voltage is not fixed. It comes from the main micro IC3251/pin 55 via IC4006.

When a wide width picture is called for, a low DC voltage from IC3251/pin 55 is applied to Q4007. The high output at its collector is input to buffer IC4006/pin 5. Then IC4006 amplifies and inverts this voltage. The low voltage that is output IC4006/pin 1 is applied to comparator IC4004/pin 4 to change the pulse width.

As a result, the lower voltage at IC4004/pin 4 produces a wider positive output pulse at IC4004/pin 2. Q4028 and Q4003 amplify the output pulse. The pulse is low pass filtered into a DC voltage to become the supply voltage for the horizontal driver device

A wider positive pulse produces a higher DC supply voltage. The higher voltage increases the horizontal driver's amplification, resulting in an increased picture width.



IC4006/PIN	1	2	3	5
NORM	2.6V	3.3V	3.2V	3.3V
WIDE	9.6V	4.6V	4.5V	4.6V

HORIZONTAL DRIVER

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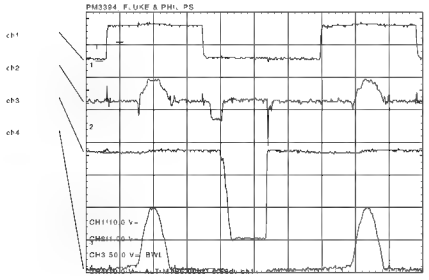
Horizontal Output PWM 1

The purpose of the Horizontal Output PWM stage is to manufacture a regulated B+ source for the Horizontal Output transistor. This first part of the H. Output PWM circuit manufactures a pulse that occurs when the beam is at the middle of the screen. This pulse is later used for B+ regulation, so its correction (regulation) actually takes place on screen time. This is not evident in the picture.

The reason the pulse is delayed is to shut off the horizontal output transistor before the next cycle. This is why the correction pulse occurs in the middle of the screen. Horizontal Output transistor Q4018's large base current when the transistor is ON prevents it from cutting off immediately upon the falling edge of the drive pulse. This delay in cutoff is anticipated and the position of the correction (also an OFF) pulse is set in order to ensure transistor cutoff before the next drive pulse.

The following scope shot shows the PWM processing, starting with a horizontal drive pulse (ch 1). After shifting (ch 2), a regulation correction pulse (ch 3) occurs in the middle of the picture between the FBT pulses (ch 4).

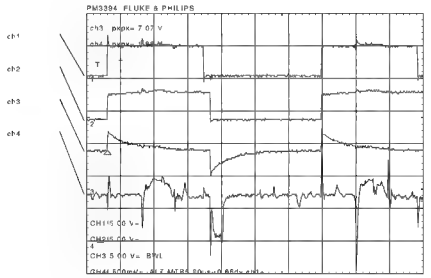


Waveform HD1b – PWM Manufacture			
	Name	Location	Voltage/div
Channel 1	H Drive	CN4009/pin 10	12Vp-p
Channel 2	Delayed drive	CN4009/pin 9	1.2Vp-p
Channel 3	PWM Output	Q4022/drain	144Vp-p
Channel 4	Ref FBT pulse	FBT	N/A
Time base	5usec/div		

Horizontal Drive Pulse First Delay

Monostable multivibrator (MMV) IC1704/pins 2-13 and comparators IC1705/pins 1-7 perform the first delay. The output at CN1303/pin 9 is a delayed low going pulse.

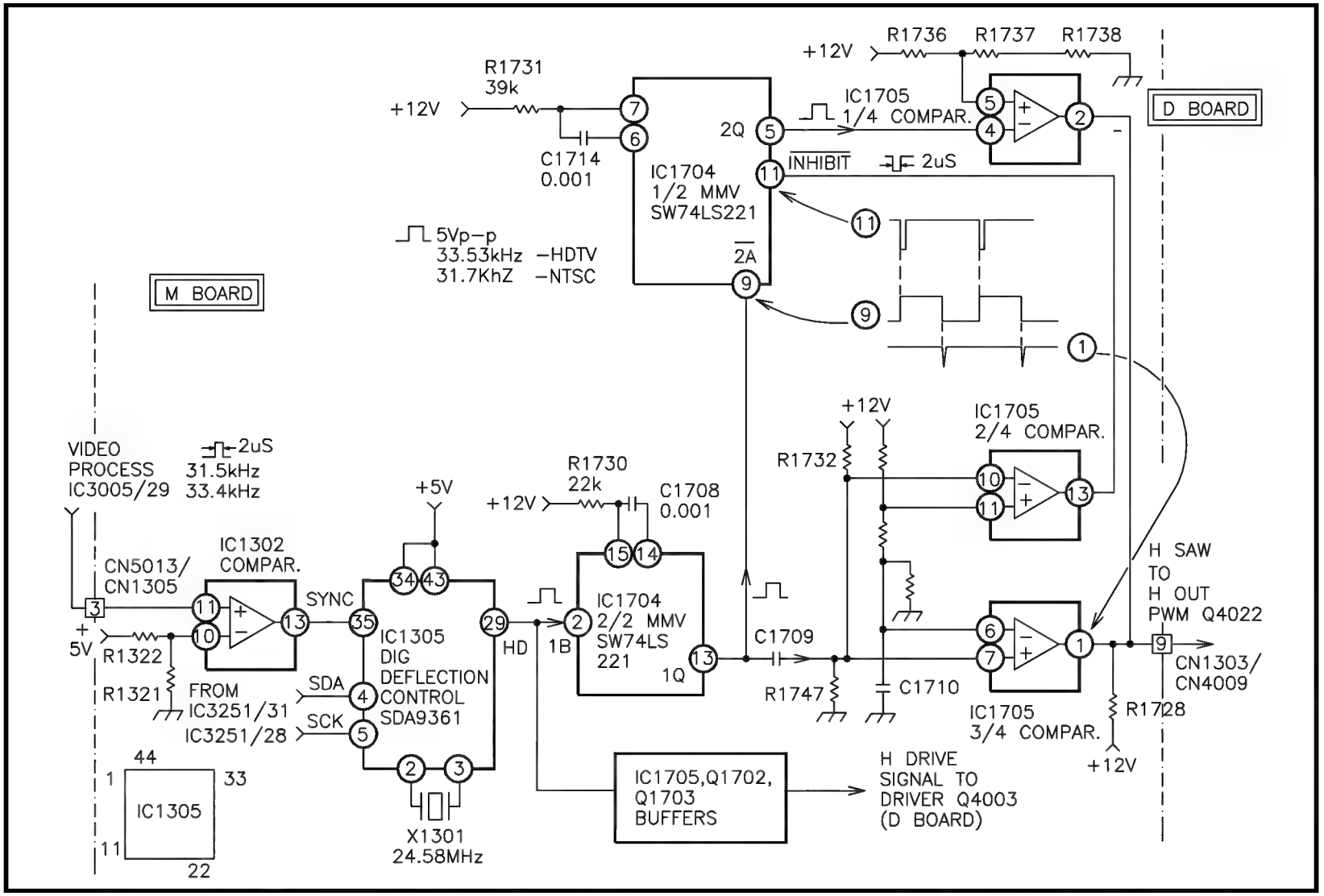
The details can be seen in the waveforms of the following scope shot and are explained below:



Waveform HD1c – First Delay			
	Name	Location	Voltage/div
Channel 1	H. Drive	IC1704/pin 2	5Vp-p
Channel 2	Ist MMV Output	IC1704/pin 13	5Vp-p
Channel 3	Cap coupled	IC1705/pin 7	7Vp-p
Channel 4	1st Delayed pulse	IC1705/pin 1	1.88Vp-p
Time base	5usec/div		

The horizontal drive signal is input at IC1704/pin 2 (ch 1). This monostable multivibrator is triggered by the leading edge of the drive signal and creates an output pulse (ch 2). The pulse width is dependent upon the RC values at IC1704/pins 14 and 15. The second pulse is coupled to comparator IC1705/pin 7 (ch 3) through C1709. The charging and discharging of C1709 forms the peaks of this waveform.

R1732 and R1747 form a voltage divider that prebiases the input of the comparator IC1705/pin 7 (ch 3). The prebiasing permits only the delayed bottom peaks of the input waveform to produce an output pulse at IC1705/pin 1. This low going output pulse is delayed from the original horizontal drive signal and is applied to the second delay circuit on the D board via CN1303/pin 9.



HORIZONTAL OUTPUT PWM 1

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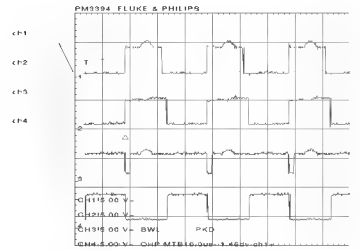
Additional Circuits

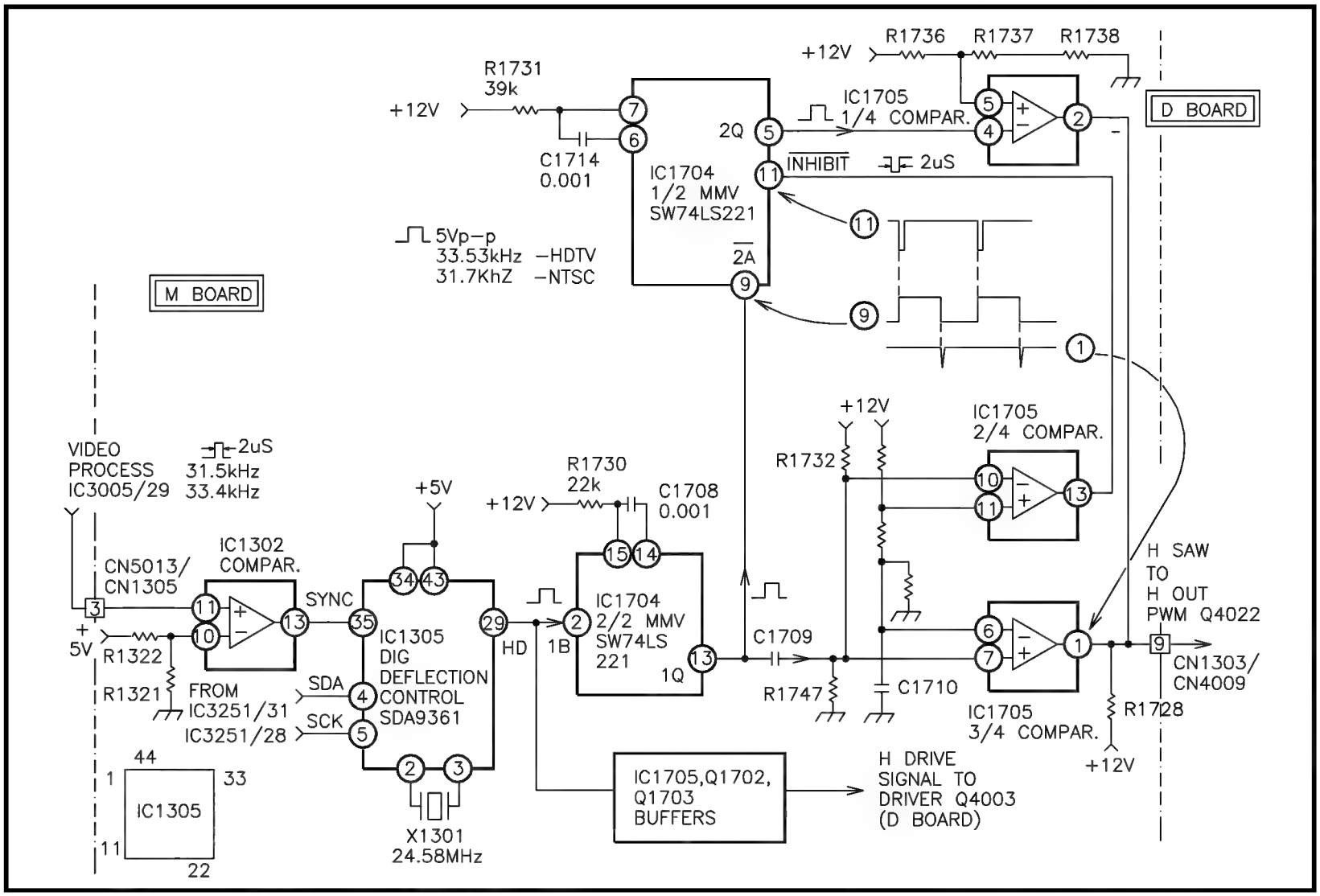
The purpose of the IC1704 MMV at pins 9-5 and the comparator at IC1705/ pins 2-5 is to provide an operating window for the low output pulse leaving this stage at CN1303/pin 9. The output pulse can only go low within this window. This prevents a double pulse that could be caused by local noise and the danger of shutting off the H. Output transistor early after turn on.

Operating Window Circuit			
Device	Input	Output	Purpose
MMV	IC1704/pin 9	IC1704/pin 5	Creates an operating window pulse.
Comparator	IC1705/pin 10	IC1705/pin 13	Makes a low pulse to end the window pulse.
Comparator	IC1705/pin	IC1705/pin	Inverter

The scope shot shows the H. drive signal input IC1704/pin 2 and output of the first MMV (ch 1, 2) which triggers the second MMV, closing the window. The second MMV output is shown in the last waveform (ch 4). It is reset at the end of its timing by the inhibit pulse applied to IC1704/pin 11 (ch 3). After being reset, the window is opened, permitting the main output pulse from IC1705/pin 1 to occur and leave CN1303/pin 9.



Waveform HD1a – Operating Window			
	Name	Location	Voltage/div
Channel 1	H. Drive	IC1704/pin 2	5Vp-p
Channel 2	1st MMV Output	IC1704/pin 13	5Vp-p
Channel 3	Inhibit/reset pulse	IC1704/pin 11	5Vp-p
Channel 4	2nd MMV Output	IC1704/pin 5	5Vp-p
Time base	10usec/div		



HORIZONTAL OUTPUT PWM 1

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Horizontal Output PWM 2

The purpose of the entire Horizontal Output PWM stage is to manufacture a regulated B+ source for the horizontal output transistor. The first part of the H. Output PWM circuit manufactures a pulse that places the B+ correction at the middle of the screen. In the second part of the H. Output PWM circuit the B+ source is regulated.

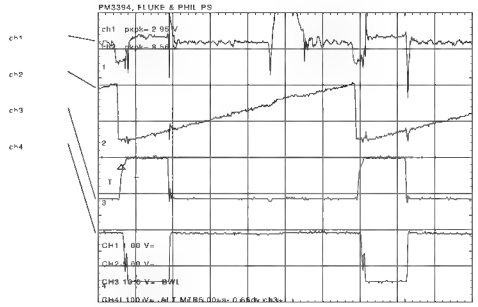
Regulation

Regulation Circuitry			
Device	Input	Output	Purpose
Q4016, Q4023, C4007	H. Saw low reset pulse.	Ramp voltage	Transistors reset charging capacitor to make a ramp voltage.
IC4004	Ramp – pin 6 B+ error – pin 7	PWM – pin 1	Adjusts pulse width to correct B+ voltage.
IC4011 Error regulator	PWM – pin 12 NTSC/DTV sw – pin 5	Error Out – pin 6	Creates a B+ correction voltage. Adjusts voltage for higher H. freq. Used in DTV.
IC4005	DC – pin 5 FH status – pin 6	DC – pin 7	Amplifier Lowers B+ when there is no H phase lock (FH status)

Ramp Manufacture

At CN4009/pin 9 the 1.5Vp-p low going pulse made by the previous MMV stage is input to transistor Q4016/base. The low turns off Q4016, which turns on Q4023 to discharge C4007. When Q4023 turns off, C4023 charges. This creates a ramp at the horizontal frequency. This ramp is applied to comparator IC4004/pin 6 and produces an output pulse at pin 1. The width of that output pulse is dependent upon the DC error voltage input IC4004/pin 7.

The following scope shot shows the ramp (ch 2) and the input pulse used to reset it (ch 1). The ramp waveform (ch 2) can be compared to the output pulse (ch 3) to see that approximately 1.3 volts was input at IC4004/pin 7 to produce this pulse width. The output waveform (ch 4) shows the pulse is inverted and amplified by the output MOSFET.



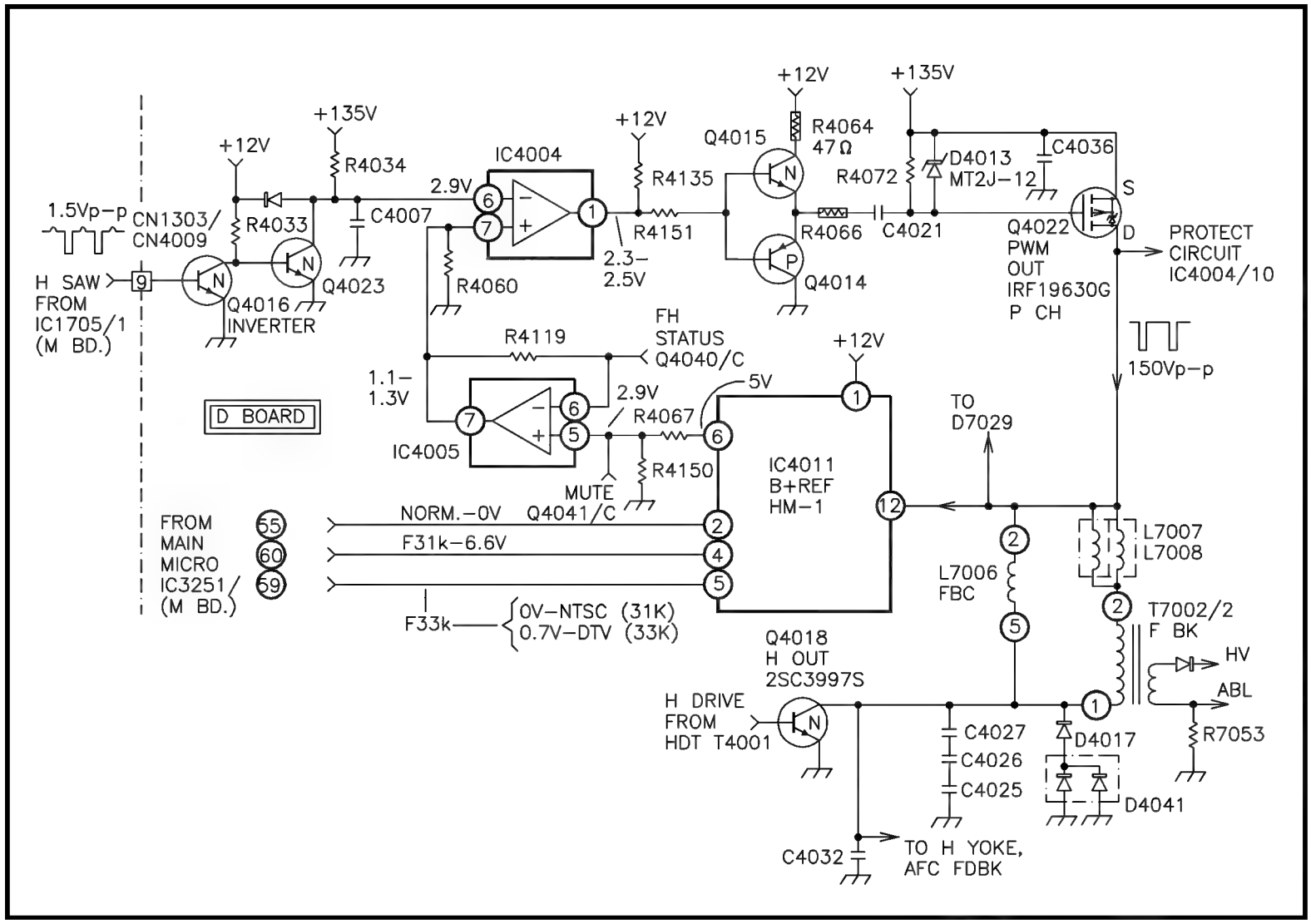
Waveform HD2 –Pulse Width Control			
	Name	Location	Voltage/div
Channel 1	H. Saw used to make ramp voltage.	CN4009/pin 9	1.2Vp-p
Channel 2	Ramp voltage	IC4004/pin 6	8Vp-p
Channel 3	PWM pulse	IC4004/pin 1	12Vp-p
Channel 4	PWM Output	Q4022/drain	150Vp-p
Time base	5usec/div		

Error Voltage

IC4011 makes an error voltage by comparing the PWM B+ output at Q4022/drain to an internal reference voltage. The difference is an error voltage output IC4011/pin 6. This error voltage is used to maintain the B+ voltage despite the load variations that occur when the brightness or scan width changes.

When a HDTV signal is received, the horizontal oscillator frequency is slightly higher than that from an NTSC signal. The change in frequency results in a change in horizontal efficiency. To maintain the same picture brightness and focus, the reference voltage in IC4011 is adjusted to compensate for this input change. The NTSC/DTV input at IC4011/pin 5 is monitored for this change. However, the correction has little effect on the output voltage even if pin 5 was changed manually.

The B+ error signal leaves IC4011/pin 6 and is amplified by IC4005. The other input to amplifier IC4005 is used to reduce the B+ voltage when no TV station (H sync) is detected. An FH status voltage from the main micro IC3512 is input to C4005/pin 6 for this purpose. When there is no H sync detected, the FH line goes high. This reduces the voltage at IC4005/pin 6 to narrow the output pulse width and lower the PWM B+ slightly.



HORIZONTAL OUTPUT PWM 2

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Summary

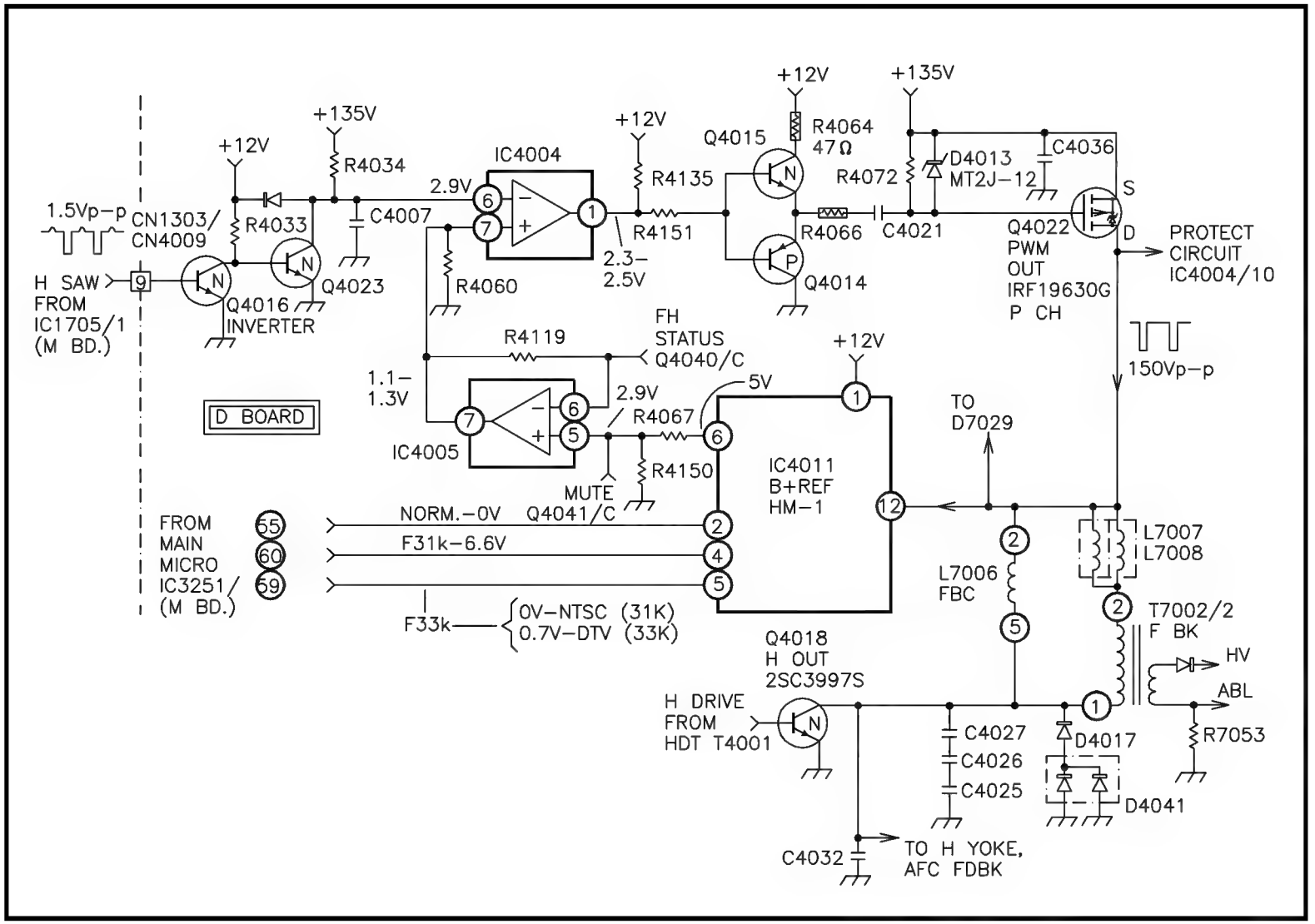
The regulation path that corrects for B+ variations can be shown in this chart that begins with an increased load that reduces the B+:

Regulation for Increased Load					
PWM B+ Q4022/D	Error out IC4011/6	Amp IC4005/7	Pulse IC4004/1	Pulse Q4022/G	Output Q4022/D
↓	↓	DC is lower	Width is Narrower	Width is Narrower	↑

A positive gate pulse is used to turn OFF the P channel PWM output device (Q4022) so the narrower the pulse, the higher the B+ voltage.

PWM Output Circuit

This output circuit consists of a buffer (Q4015 and Q4014) which is used to supply drive current to the gate of Q4022. An inverted pulse is output at Q4022's drain and applied through FBT T7002 to the horizontal output transistor Q4018 collector. This PWM voltage serves as the regulated B+ voltage for Q4018.



HORIZONTAL OUTPUT PWM 2

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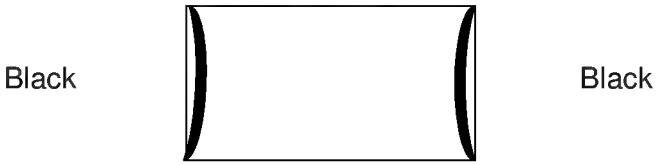
Pincushion Correction

Electronic pincushion correction is necessary because it is difficult for the yoke to generate perfectly uniform magnetic fields in all areas. Without this circuit a yoke will display a reduced scan creating a caved in hour-glass picture.



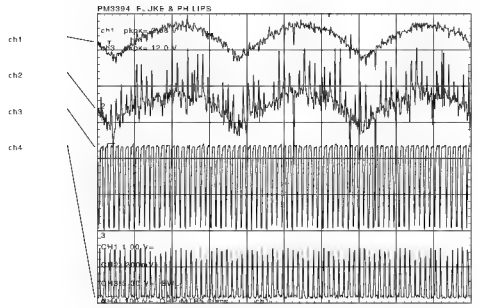
By increasing the current through the yoke, a larger magnetic field is created that will stretch the picture, filling the screen. To produce a straight picture, the magnetic field must be increased gradually while the electron beam is scanning from the top down to the center. From the center of the picture down, the magnetic field intensity should then gradually decrease.

The correction signal required is at a 60 Hz. vertical rate. This signal comes from the Digital Deflection Control IC1305/pin 20.

Circuitry

The Digital Deflection Control IC1305 makes the vertical drive signal and the pincushion correction signal. The correction signal leaves IC1305/pin 20 as a parabola waveform labeled EW (east/west correction).

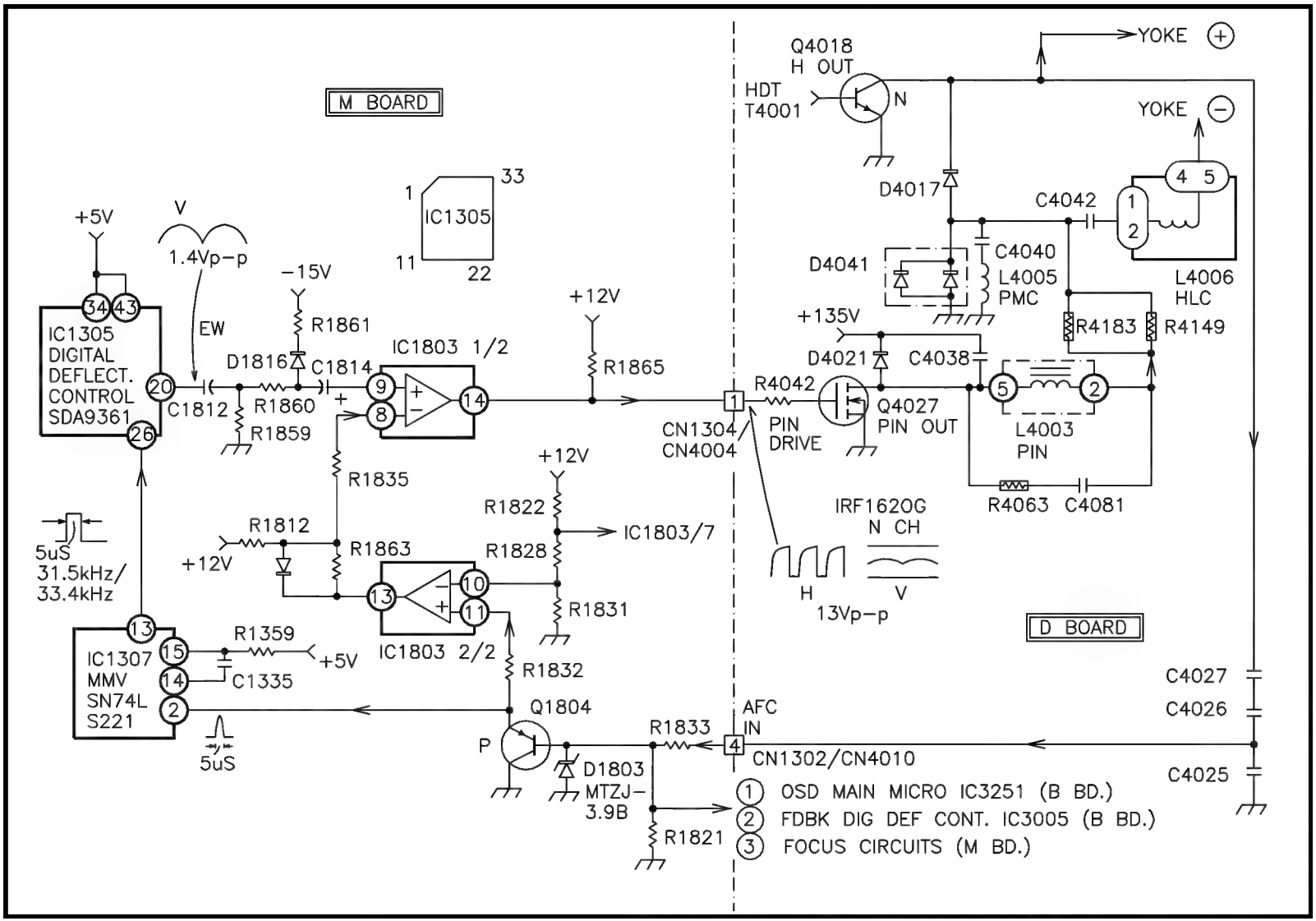
The low frequency 60Hz signal is added line by line using a horizontal AFC pulse input IC1803/pin 8. The output signal at IC1803/pin 14 looks like the E/W parabola chopped up at a horizontal rate.



Waveform Pin 1 - Parabola Signal Processing			
	Name	Location	Voltage/div
Channel 1	E/W parabola	IC1305/pin 20	1Vp-p
Channel 2	Reduced parabola	IC1803/pin 9	0.3Vp-p
Channel 3	Chopped parabola	IC1803/pin 14 CN1304/pin 1	12Vp-p
Channel 4	Pin Output	Q4027/drain	142Vp-p
Time base	5msec/div		

The 12Vp-p chopped parabola signal is amplified by MOSFET Q4027 and applied to the low end of the yoke (-) via HLC coil L4006. When Q4027 conducts, it shunts the PMC coil L4005, providing a higher current path to ground for the energy in the yoke. This increases magnetic deflection. The amount of deflection is dependent upon Q4027's conduction. The conduction is based upon the gate's parabola voltage level.

The following waveforms were taken at the same location as above, but at a 10usec/div time base so you can see the horizontal pulses chopping the vertical parabola.



PINCUSHION CORRECTION

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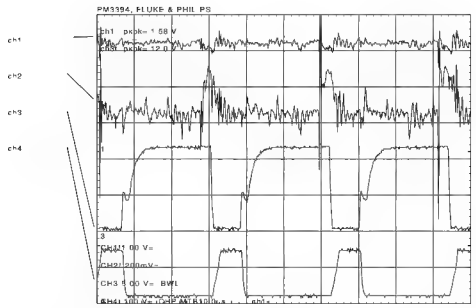
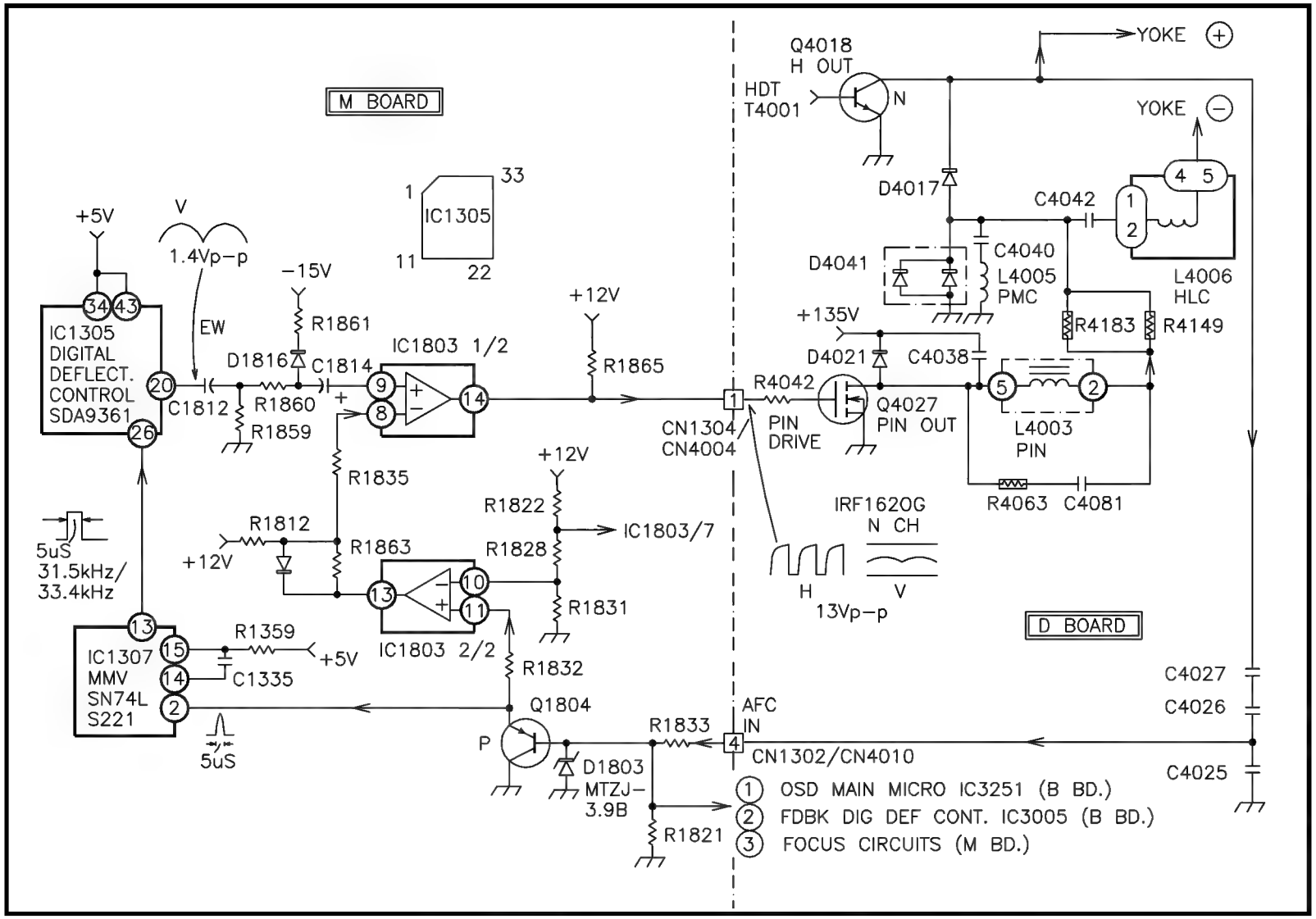


A sample of the horizontal flyback pulse from Q4018's collector is buffered by Q1804. This signal performs two functions:

1. Pincushion modulation at IC1803/pin 11,
2. Horizontal AFC at IC1305/pin 25 (automatic picture phase lock correction).



PINCUSHION CORRECTION

HDTV25 1047 3 9 99

Picture Tilt Circuit

This circuit produces a signal that is applied to the black N/S coil suspended around the plastic yoke frame by the picture tube bell. This N/S coil serves two purposes:

1. Left or right picture tilt (rotation); and
2. Horizontal trapezoid correction.

The N/S in N/S coil stands for north/south because it compensates for the north-south terrestrial magnetism.

Picture Tilt

The picture tilt circuit has been added to straighten the picture. The picture could have been rotated by earth's magnetic field and is no longer parallel to the front panel.

Applying a current to a coil of wire creates a magnetic field. As an electron beam is passed through this field, the electron beam producing the picture will twist. The greater the current, the greater the twist. Reversing the polarity causes the beam to turn in the opposite direction.

The picture tilt feature in this HDTV can be controlled from the user menu and service mode. The tilt command path from the user menu to the N/S coil is shown in the chart below:

Picture Tilt Path			
Device	Purpose	In	Out
Main Micro IC3251	Selects tilt data previously stored in external memory.	Remote control SIRCS data IC3251/pin 7 (not shown)	Serial bus data and clock IC3251/pins 28 and 31.
D/A Converter IC1701	Interprets data to make a DC voltage.	Data – pin 21 Clock – pin 20	DC voltage – pin 4.
Amplifier Q1906	Expands the 5V input range to a ±15V range.	Q1906/Base	Q1906/Collector
Output IC1901	Current drive	DC input IC1901/pins 3 and 6.	DC differential output @ pins 2 and 8.
N/S Coil	Changes current flow into a magnetic field.	CN1901/ pins 1 and 3.	Magnetic field

User Tilt Adjustment

The user has an on screen display (OSD) menu number that displays the tilt amount from –10 to +10. The number zero should correspond to no DC voltage entering the N/S coils if the coarse tilt adjustment in the service mode is set correctly.

This chart shows DC circuit voltages at the three settings of the user tilt control.

Picture Tilt Voltages						
OSD	D/A Conv IC1701/pin		N/S Output IC1901/pin			
Tilt #	3	4	3	6	7	Bet 2-8
+10	2.4V	4.8V	-9.48	-10.1V	-10.3	-7.5V
0	2.4V	2.4V	-9.44	-9.3V	-9.47	0.326
-10	2.4V	0.1V	-9.41	-8.5V	-8.63	+7.9

Note that the D/A Converter IC1701/pin 3 voltage does not change with the tilt settings. This is because IC1701/pin 3's voltage is used for trapezoid correction, not tilt correction.

Service Mode Tilt Adjustment

The coarse tilt adjustment is set in the service mode. The data that corresponds to the tilt voltage output at D/A Converter IC1701/pin 4 is found in:

Category DM; register #6, name = NSCO.

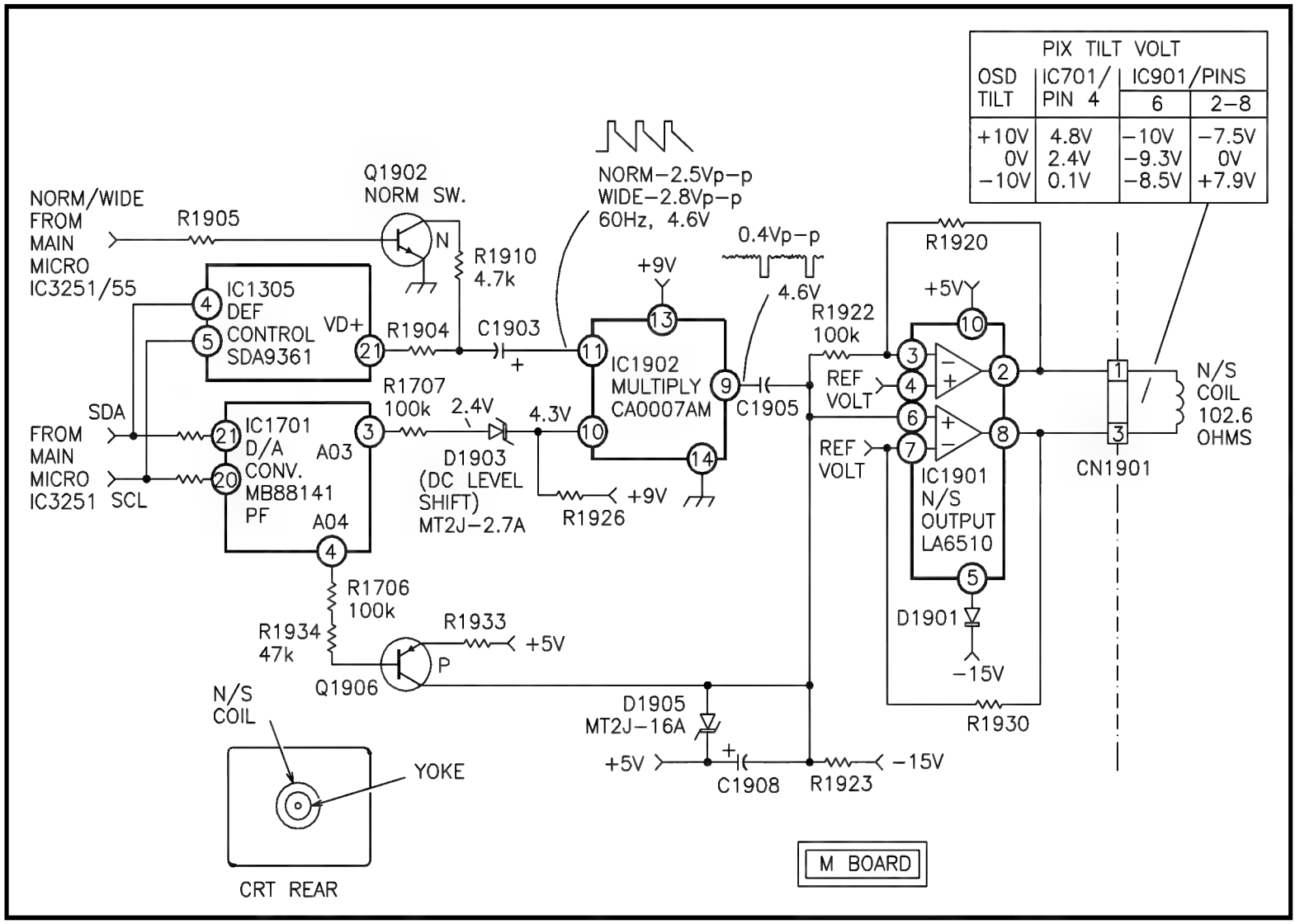
This information is shown this way on the TV screen in the service mode:

DM 6 **31** Service

NSCO Normal TV

In register #6 there are seven pieces of data, one for each of the 7 seven picture geometry modes. The Normal 4:3 ratio picture data is shown above. Pressing the Full, Zoom, Caption, and Wide Zoom permits you to access the data for the four other geometry modes. The remaining two modes apply when a HDTV picture is received in the 1080I and 480I line resolution.

In this typical set, the coarse tilt data level for a normal (4:3 ratio) width picture is 31. This is corresponded to **NO** DC voltage applied to the N/S coil when the user tilt setting is zero.



PICTURE TILT CIRCUIT

HDTV28 1048 3 9 99

Horizontal Trapezoid Correction

In addition to tilt correction, the N/S coil also performs a mild trapezoid (keystone) picture correction. This is controlled in the service mode as register HTPZ #5 in the DM category. The data in the sample set is 32 during the normal, full, zoom and CC geometry modes. It is 31 in the two DTV modes.

Correction data 32 causes D/A Converter IC1701 to output 2.4Vdc from pin 3. This voltage is applied to the anode of zener diode D1903. As long as the zener is forward biased, the cathode will be at 2Vdc (the zener voltage) higher that the anode voltage. This results in a 2V addition to the original D/A Converter voltage. The final voltage in this sample set is about 4.3Vdc and is applied to Multiplier IC1902/pin 10 for trapezoid correction control.

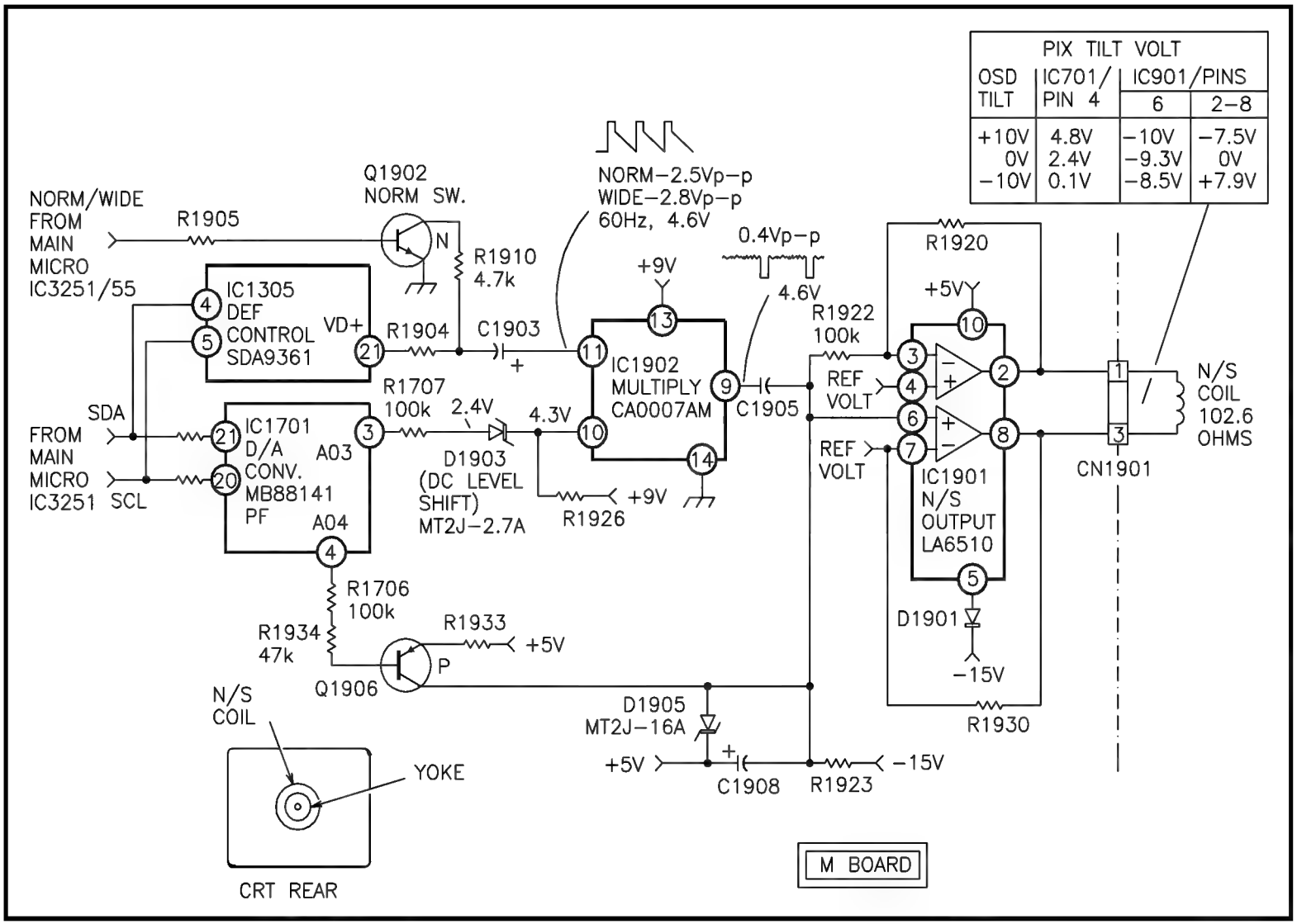
Multiplier IC1902 also has a vertical sawtooth signal input at pin 11 for trapezoid correction. The polarity and amount of sawtooth signal output is set by a single DC voltage input IC1902/pin 10.

Multiplier IC1902 Outputs			
"DM" Category HTPZ register # 5 Data	Input IC1902 pin 10	Output – IC1902/pin 9	
		Voltage	Waveform
32 (Normal)	4.44V	0.2Vp-p, 4.6V	
0 (Minimum)	2.18V	3Vp-p, 4.51V	
63 (Maximum)	6.58V	2.5Vp-p, 4.68V	
34 (no output)	4.58V	0.2Vp-p, 4.6V	----------

The signal from IC1902/pin 9 is coupled by C1905 to the N/S Output Driver IC1901/pin 6 and 3 and added to the DC picture rotation voltage for trapezoid correction.

Additional Components

Additional Components	
Device	Purpose
Q1902 Norm switch	Reduces the vertical signal to the multiplier IC1902/pin 11 during normal picture width to increase the effective multiplier IC operating range.
D1905 16V Zener	Prevents the multiplier IC1902 signal from exceeding the +5 to –11Volt range.
D1901 Diode	Temperature stabilizes IC1901.



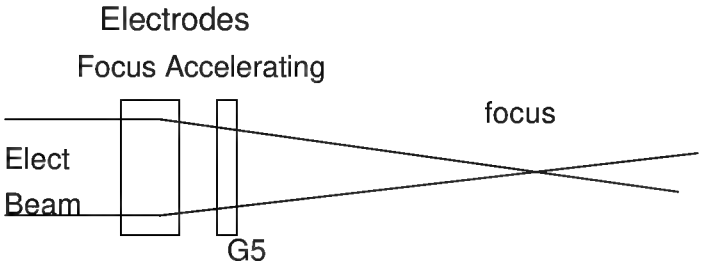
PICTURE TILT CIRCUIT

HDTV28 1048 3 9 99

Dynamic Focus Block

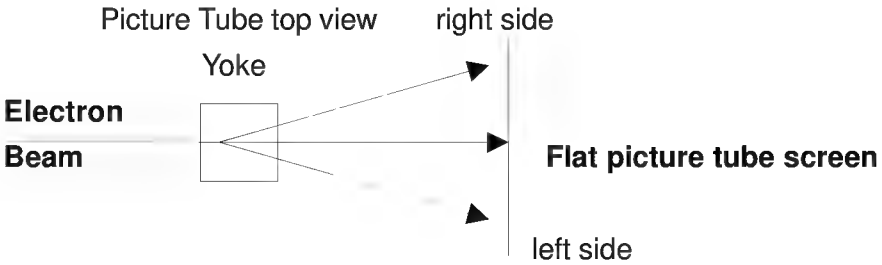
Static Focus

An electron beam within the picture tube consists of many electrons that are slowed down by the focus electrode and then accelerated by the following (G5) electrode into a fine point at the screen. The focus point is positioned by adjusting the voltage at the focus electrode relative to the accelerating voltage. The G5 voltage is usually fixed at the HV potential from the flyback secondary.



Picture Tube Focus

The focus points form an arc as the electron beam is moved from side to side (swept) by the magnetic field created by the external horizontal deflection yoke. The picture tube glass screens were made into a similar arc (actually sphere) to maintain focus.



Focus Arc

Modern picture tube screens are flat to reduce annoying room glare. This means the focus point must be moved up at the left and right sides to meet the flat picture tube screen.

Dynamic Focus

DC Voltage for Static Focus Voltage (fv) is applied to the focus electrode of the picture tube from the FBT T7002. This establishes focus on a curve or arc just behind the flat CRT screen.

Dynamic focus voltage comes from transformer DFT T7001. The dynamic focus voltage is added to the static focus voltage from FBT T7002 to create the final focus voltage (fv) that is applied to the picture tube's focus electrode. This voltage corrects the screen's left and right side focus.

Circuit Block Operation

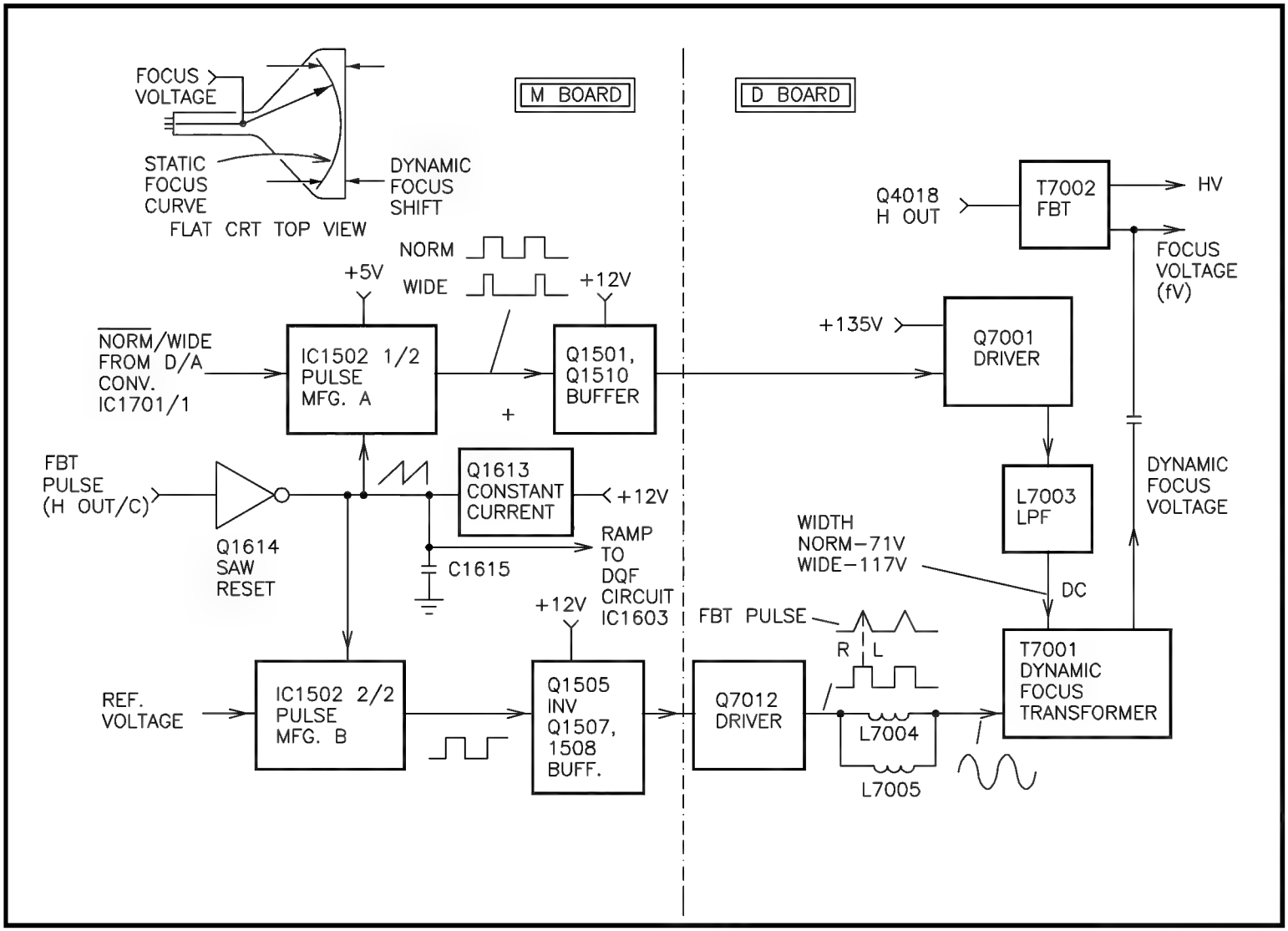
The four blocks along the top and the three blocks along the bottom of the dynamic focus block diagram make up the dynamic focus stage that feeds the dynamic focus transformer T7001. The top and bottom blocks have different purposes:

Dynamic Focus Circuit		
Circuitry	**Purpose**	**Major Parts**
Four Upper Blocks	Create and regulate the DC voltage applied to the DFT T7001. A higher voltage is used when a wide picture is selected.	IC1502, Q1501, 1510, Q7009
Three Lower Blocks	Marks the left and right side of the screen for dynamic focusing.	IC1502, Q1505, Q1507, Q1508, Q7012

Top Circuit Blocks

The pulse mfg. A, buffer, driver and LPF blocks along the top create and regulate the supply voltage for Driver Q7012. The higher the supply voltage applied, the greater the dynamic focus voltage amplitude is generated for focus correction. A larger dynamic focus voltage is required when the deflection is at full width.

A ramp signal is needed to begin making this supply voltage. Capacitor C1615 is charged to make this ramp. C1615 is reset using flyback pulses via Q1614 so the ramp is at the horizontal scan frequency. This ramp is applied to pulse manufacturing blocks A & B.



DYNAMIC FOCUS BLOCK

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The top pulse mfg. A block compares the input ramp to a DC voltage to produce a pulse. By changing this DC voltage, the pulse width can be controlled for more or less dynamic focus correction. More correction is required during a wide picture so a low input voltage produces a wider low going pulse.

The second block is a current buffer (Q1501 and Q1510) that feeds the pulse to driver Q7001 in the third block. The driver amplifies and inverts the pulse so that a wider low going pulse results in longer conduction time for Q7001 and consequently a higher supply voltage.

The fourth LPF block consists of a coil and capacitor that filters the pulse into a DC voltage. This supply voltage is applied through DFT T7001's primary to driver Q7012.

Bottom Circuit Blocks

The pulse mfg. B, inverter/buffer and Q7012 driver circuit blocks along the bottom of the dynamic focus block diagram is discussed next. The purpose of these blocks is to make a single pulse that identifies the left and right sides of the screen for dynamic focus correction.

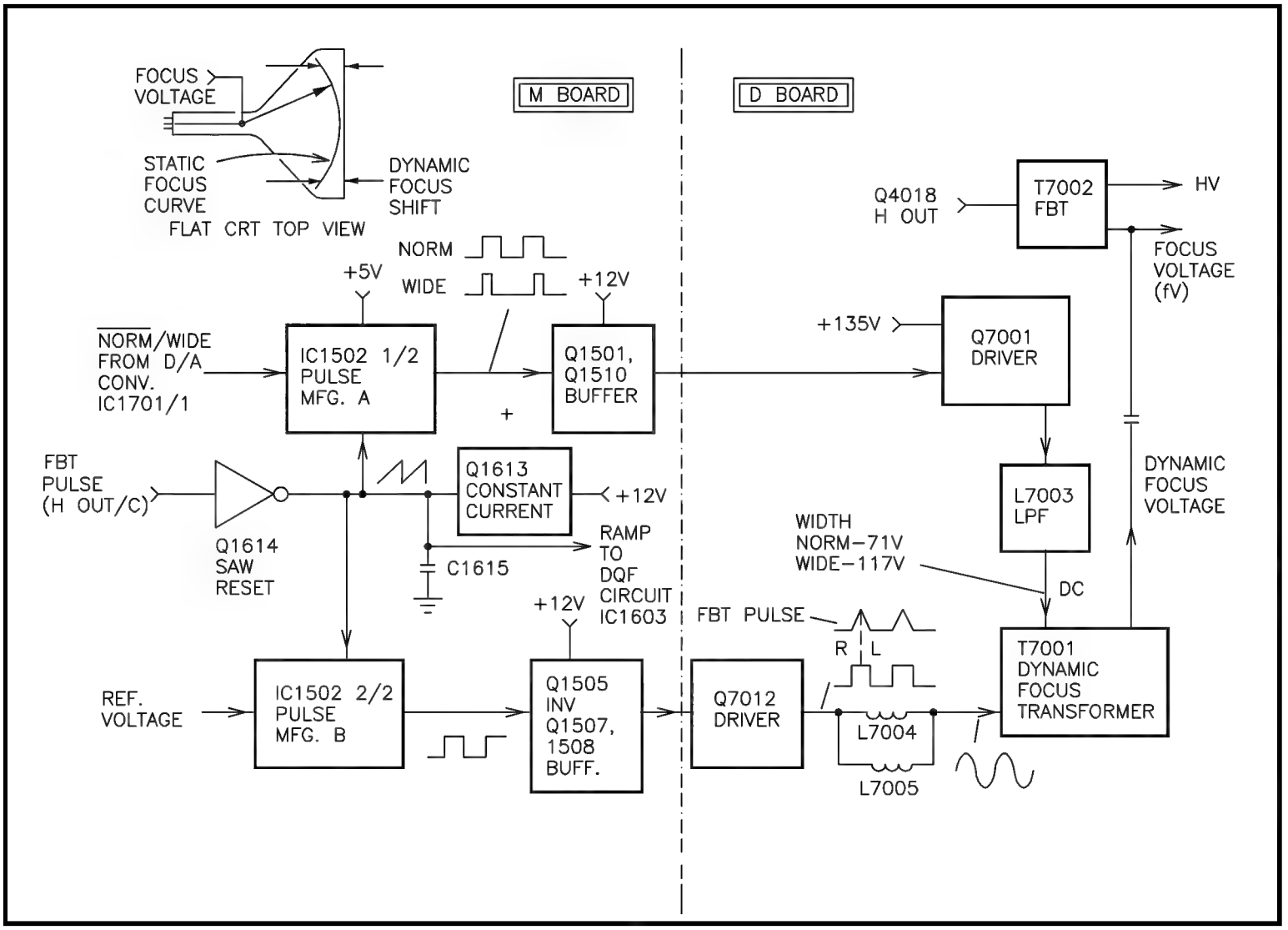
This location pulse is manufactured from the pulse manufacture B block. A ramp and reference voltage are input to the first block. A pulse is created that begins when the electron beam is at the right side of the screen. After the beam has retraced and ventured into the left side of the screen, the pulse ends. This pulse marks the area that dynamic focusing takes place (at the left and right sides of the screen).

The second block inverts this location pulse and buffers it for voltage/current gain. The third driver block amplifies this pulse and applies it to the Dynamic Focus Transformer T7001. In this output stage, the location pulse is shaped into a sine wave by L/C components. This sine wave is coupled by T7001 to the DC focus voltage from the FBT, modulating it. The modulation increases the focus voltage when the electron beams are at the left and right sides of the screen.

Output Waveform

A lower DC voltage of 71Vdc in normal picture width causes just the peaks of the bottom waveform to be added to the focus voltage for minimal focus correction. In a wide width picture the focus point must be moved further so a larger 117-supply voltage is produced. The higher voltage increases the amplitude of the sine waveform for greater focus correction.

The resultant FV focus voltage is now a dynamic voltage that adjusts the focus point to match the center, left and right sides of the flat TV screen.



DYNAMIC FOCUS BLOCK

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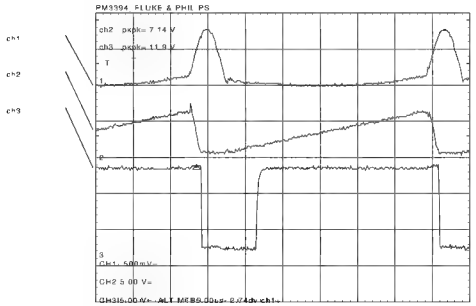
Dynamic Focus 1 – B+ Mfg.

This first half of the dynamic focus circuitry stage consists of several parts:

1. Horizontal ramp manufacture
2. PWM manufacture
3. Current and voltage amplification
4. Regulation

Horizontal Ramp Manufacture

Charging capacitor C1615 at IC1502/pin 8 creates a ramp signal (ch 2). Q1614 resets the ramp by using the horizontal pulses. The resultant ramp is at the horizontal scan frequency.

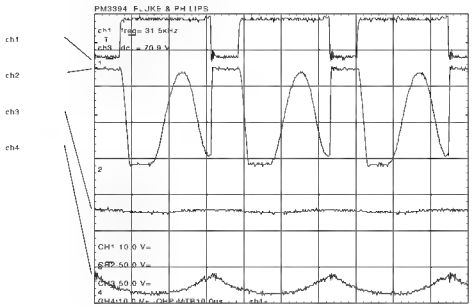


Waveform DFh – Ramp Output			
	Name	Location	Voltage/div
Channel 1	FBT	Probe at FBT	N/A
Channel 2	Ramp input	IC1502/pin 9	7Vp-p
Channel 3	Pulse Output	IC1502/pin 14	12Vp-p
Time base	5usec/div		

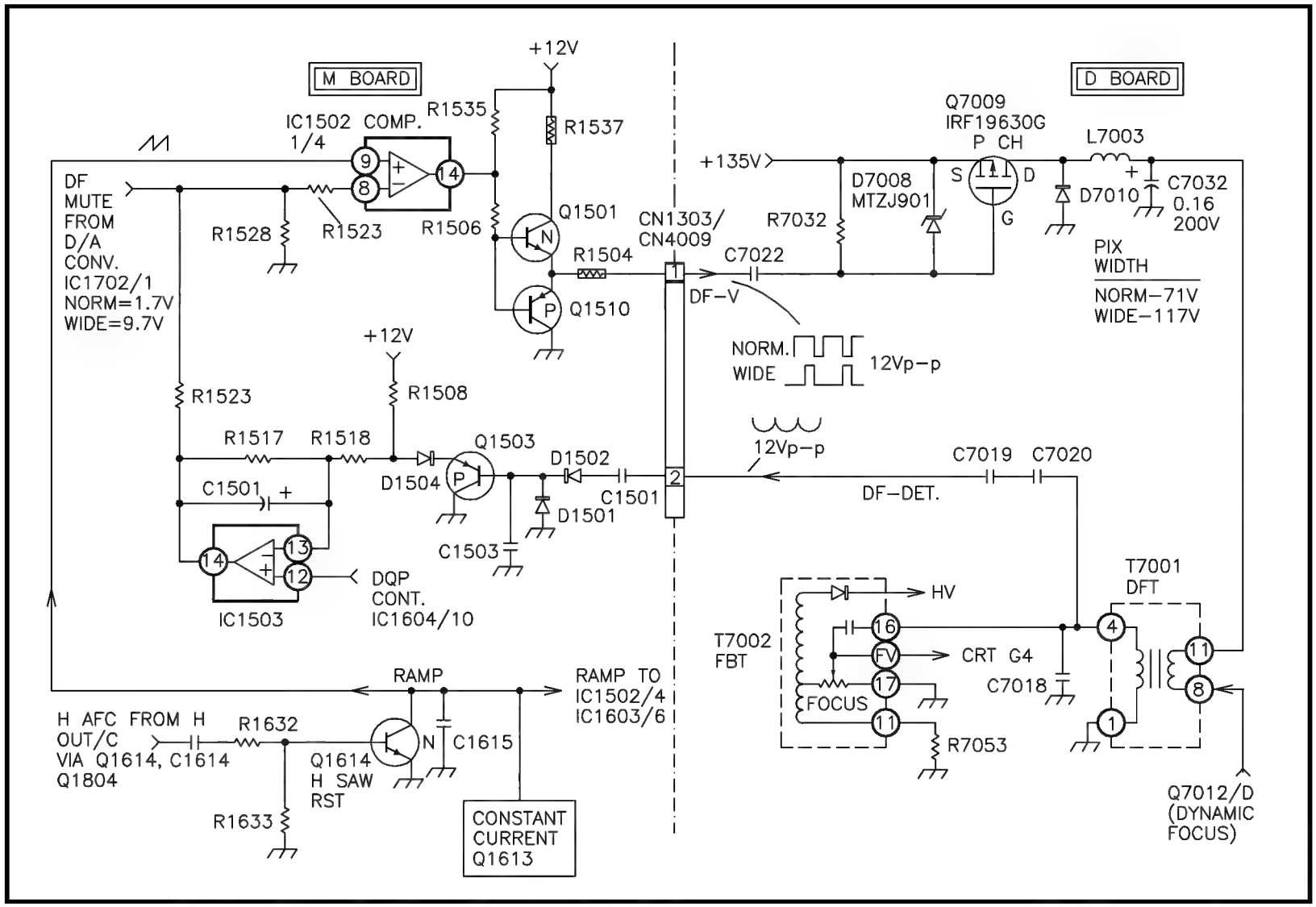
Pulse Manufacture

The horizontal rate ramp signal is input at IC1502/pin 9 and a DC voltage is input at pin 8 of this comparator. This DC voltage input at pin 8 governs the output pulse width at IC1502/pin 14. When a normal 4:3 ratio picture is requested by Main Micro IC3251 (not shown), D/A Converter IC1702/pin 1 is LOW (1.7Vdc). When a wide 16:9 (called Full, CC, Zoom or HDTV) picture is requested, D/A Converter IC1702/pin 1 is HIGH (9.7Vdc).

A 4:3 ratio picture produces a narrow low going output pulse. A wider low going pulse is output during a 16:9 aspect ratio picture. The signals manufactured during a 4:3 and 16:9 picture can be seen in the waveforms below.



Waveform DFa – Normal 4:3 aspect ratio picture			
	Name	Location	Voltage/div
Channel 1	DF-V	CN1303/pin 1	12Vp-p
Channel 2	Amplified DF-V	Q7009/D	135Vp-p
Channel 3	B+ to DFT	T7001/pin 11	71Vdc
Channel 4	DF-Det	CN1303/pin 2	7Vp-p
Time base	10usec/div		



DYNAMIC FOCUS 1 – B+MFG

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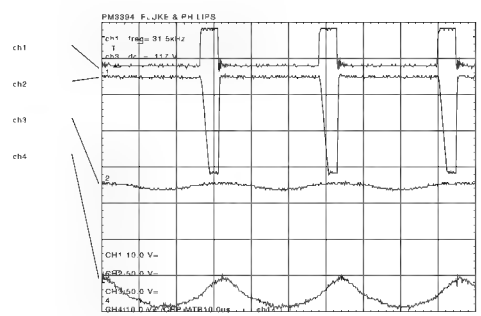


Waveform Dfb – Wide 16:9 aspect ratio picture			
	Name	Location	Voltage
Channel 1	DF-V	CN1303/pin 1	12Vp-p
Channel 2	Amplified DF-V	Q7009/D	135Vp-p
Channel 3	B+ to DFT	T7001/pin 11	71Vdc
Channel 4	DF-Det	CN1303/pin 2	7Vp-p
Time base	10usec/div		

Current and Voltage Amplification

The pulse manufactured by comparator IC1502/pin 14 is buffered by Q1501 and Q1510. It leaves the M board through fusible resistor R1504 at CN1303/pin 1 as the DF-V signal (ch 2).

On the D board, this pulse is amplified and inverted by Q7009. Q7009's source is receiving +135Vdc supply voltage that leaves from its drain lead when turned on (conducting).

As with any MOSFET, when the voltage at its gate is kept at the source potential, the MOSFET is OFF (no D-S current). As the gate voltage is brought towards the drain potential, the MOSFET begins to conduct. Unlike a transistor, conduction begins when the gate voltage is about 2-4 volts.

Therefore when the DF-V pulse brings the gate voltage low, Q7009 conducts, passing the +135Vdc from its source to the drain. The input voltage of only 12Vp-p at Q7009's gate is amplified to 135Vp-p at its drain. The signal is also inverted. This signal is low pass filtered into a DC voltage by L7003 and C7032. The resultant DC voltage is applied to T7001/pin 11. D7010 at Q7009's Drain lead prevents a negative voltage there. The negative voltage is caused by the collapsing field of the resonate tank circuit connected to the drain lead.

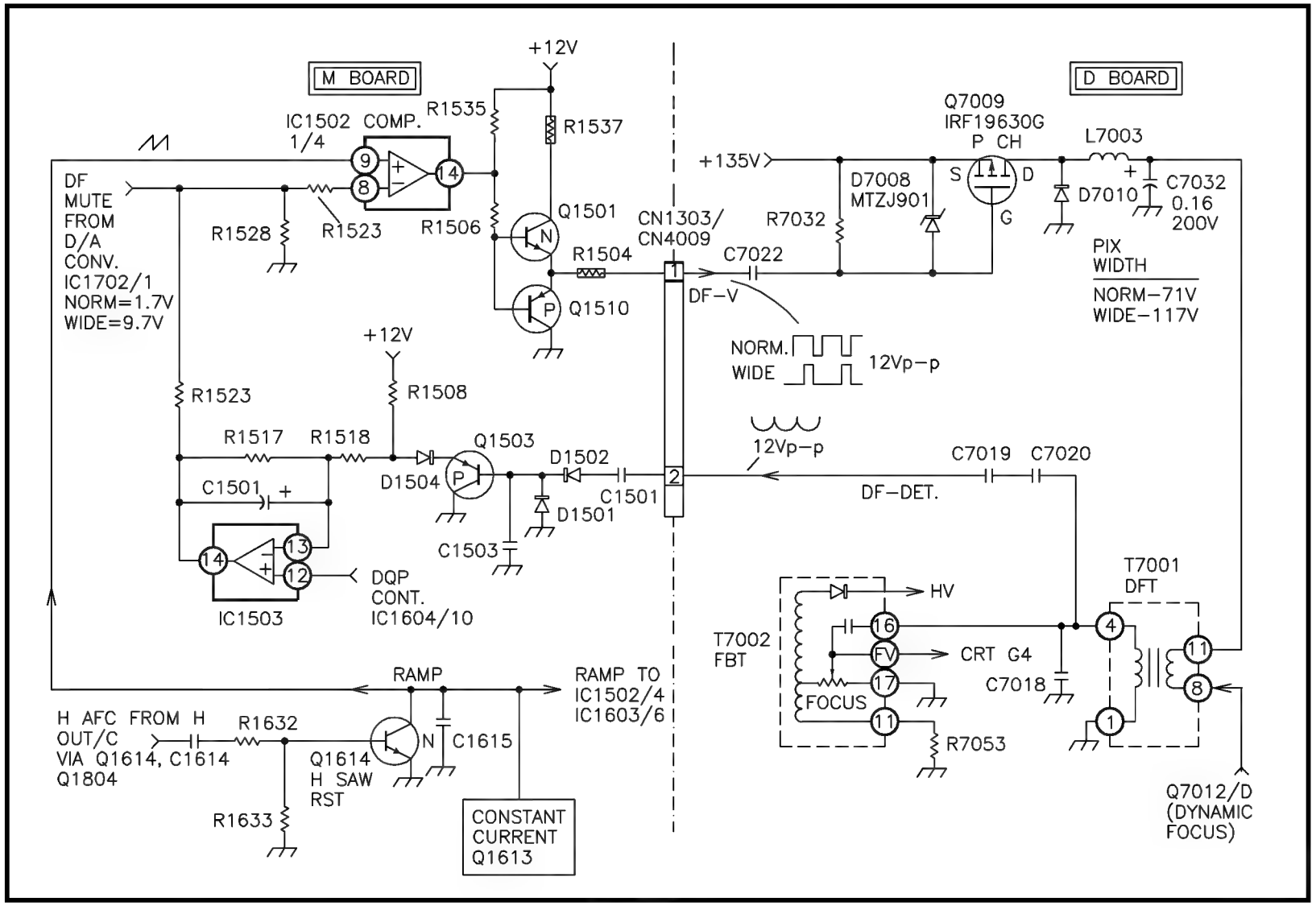
DC Voltage Output to DFT T7001/pin 11		
Mode	Aspect Ratio	DC Voltage
Normal	4:3	71V
Zoom, Full, CC, HDTV reception.	16:9	117V

Regulation

A sample of the dynamic focus voltage from DFT T7001/pin 4 (and the FBT pulse) is returned to the first pulse manufacturing stage at IC1502/pin 8 for regulation. C7019 and C7020 couples the DFT T7001/pin 14 signal on the D board to become the DF-Det signal (ch 4).

The DF-DET signal is then rectified by D1502 on the M board before being buffered by Q1503, inverted by IC1503, and returned to IC1502/pin 8 for fine pulse width correction. These changes to the static focus voltage will also result in corresponding changes to the dynamic focus voltage.

Regulation Voltages				
Mode	DF-DET CN1303/2	D1502/ Cathode	D1504/ Anode	IC1503/ Pin 14
Normal 4:3	7Vp-p	3.26V	4.55V	1.76V
Full	10Vp-p	6.07V	7.3V	9.7V
Zoom	10Vp-p	6.07V	7.3V	9.7V
HDTV	10Vp-p	6.07V	7.3V	9.7V



DYNAMIC FOCUS 1 – B+MFG

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Dynamic Focus 2 – Location

This second half of the dynamic focus circuitry stage consists of several parts:

1. Horizontal ramp manufacture
2. Pulse manufacture
3. Current and voltage amplification

These circuit parts are similar to the first half of the dynamic focus circuitry except this stage:

- Creates a single width pulse instead of two different pulse widths
- Uses an N channel power MOSFET Driver Q7012 instead of a P channel device.

The purpose of the stages in the second half of the circuitry is to create a pulse that locates the portion of the screen that needs dynamic focus correction. Specifically, it is the area before and after the horizontal retrace pulse that corresponds to the right and left sides of the screen.

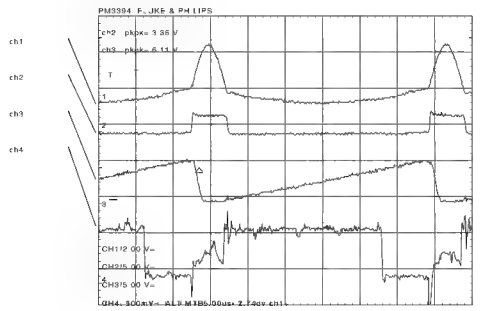
The voltage levels that come from the first half of the dynamic circuitry determine the amount of correction. A higher supply voltage to driver Q7012/D increases its dynamic focus signal level and consequently the amount of outer focus correction.

Horizontal Ramp Manufacture

Capacitor C1615 at IC1502/pin 8 makes this ramp signal. Q1614 uses horizontal pulses to reset the ramp. The resultant ramp is at the horizontal frequency.

Pulse Manufacturing

There are two inputs in the pulse manufacturing stage. A horizontal ramp waveform is input at IC1502/pin 4 (ch 2). A DC reference voltage is input to pin 5 of this comparator. The reference voltage is chosen to produce a low going pulse (ch 4) from the comparator prior to the next FBT retrace pulse (ch 1).



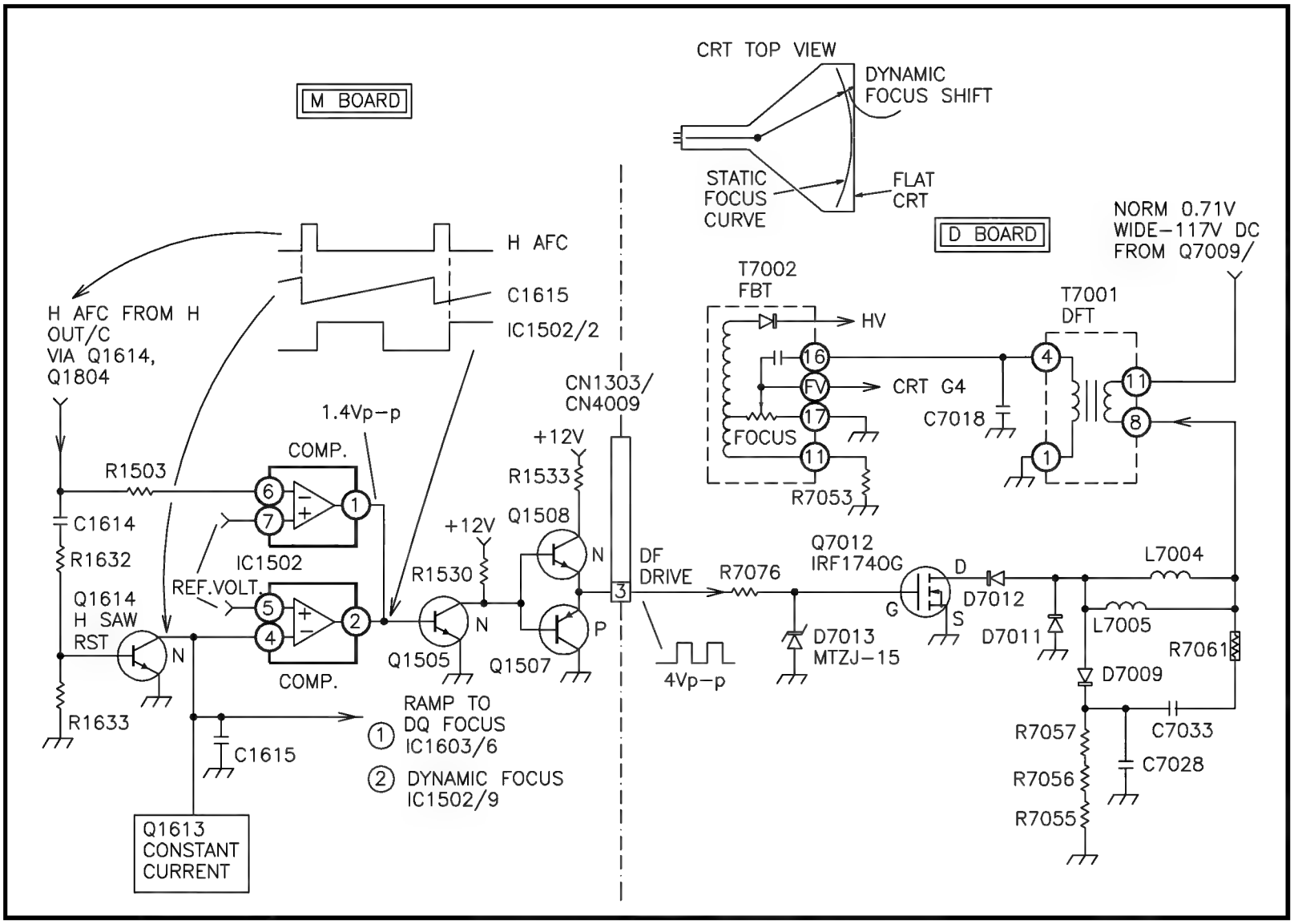
Waveform DFf - Pulse Mfg.			
	Name	Location	Voltage/div
Channel 1	FBT pulse	FBT	N/A
Channel 2	H Reset pulse	Q1614/base	5Vp-p
Channel 3	Ramp voltage	Q1614/collector	7Vp-p
Channel 4	Output pulse	IC1502/pin 2	1.4Vp-p
Time base	5 usec/div		

The low going pulse that outputs comparator IC1502 at pin 2 is reset at the beginning of the next horizontal retrace pulse (Ch 2). To extend the output pulse further, the comparator above it receives a horizontal retrace pulse at IC1502/pin 6. The pulse is inverted and combined with the IC1502/pin 2 output. Finally, the composite output at IC1502/pins 1 or 2 is a low pulse that starts before the retrace interval and ends at its conclusion.

Current and Voltage Amplification

The noisy 1.4Vp-p signal from IC1502/pin 2 is amplified by Q1505 and buffered by Q1508 and Q1507 for sufficient current gain to drive Q7012. Dynamic focus driver Q7012 receives the 12Vp-p gate signal and amplifies it. The amount of its amplification is dependent upon its supplied voltage. The DC supply voltage is higher for a wider picture. A wider picture needs more dynamic focus correction at the sides.

Dynamic Focus Output Signal		
	DC Supply Voltage from T7001/pin 11	Q7012/Drain (Output Signal)
Normal 4:3 picture	71 V	178Vp-p
Wide 16:9 picture	117V	273Vp-p



DYNAMIC FOCUS 2 – LOCATION

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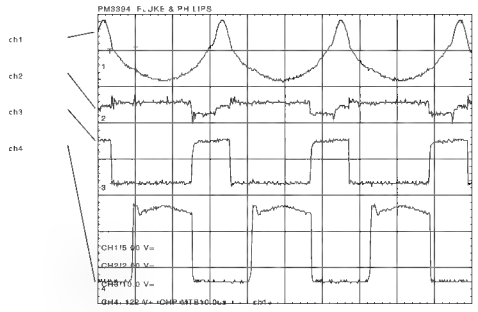
Summary

The following waveforms show the operation of the entire stage from pulse manufacture (ch 2), through inversion (ch 3), to the final dynamic focus signal at Q7012/drain (ch 4). Note that the width of the final dynamic focus signal at Q7012's drain (ch 3) is now extended beyond the horizontal re-trace interval.

This is a normal and planned characteristic of the resonate output stage consisting of T7001, C7040 and C7023. When Q7012 is off, the output stage rings at the resonate frequency. However, when Q7012 is on, L7004 and L7005 are added to the tank circuit, lowering the frequency. The result is that the negative portion of the resonate sine wave is longer than the top. The longer negative portion keeps the pulse at Q7012/drain low for a longer period than the input gate signal. This is why the drain signal is extended beyond the horizontal retrace interval.

The output pulse width (ch 3) extends beyond the FBT retrace interval (ch 1) to mark the left side of the TV screen for focus correction. This means the final dynamic focus correction signal (Q7012/drain) starts before the FBT retrace signal and ends after it. This corresponds to the left and right side of the TV picture where dynamic focus correction is needed. This signal is coupled by DFT T7001/pin 4 to the static focus voltage (FBT T7002/pin 16) for dynamic focus correction.

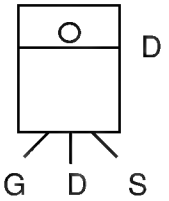


Waveform DFg - Signal Amplification			
	Name	Location	Voltage/div
Channel 1	FBT signal	FBT	N/A
Channel 2	Delayed. pulse	IC1502/pin 2	1.4Vp-p
Channel 3	DF-Drive	CN1303/pin 3	12Vp-p
Channel 4	Dynamic focus signal	Q7012/drain	178Vp-p (Norm) 273Vp-p (wide)
Time base	10usec/div		

Static MOSFET Resistance Tests

Static MOSFET Resistance Tests		
	+ / -	- / +
Gate – Source	Infinity	Infinity
Gate - Drain	Infinity	Infinity
Drain - Source	There is a zener diode connected internally across these terminals	

Power MOSET
TO 220 case
P or N channel

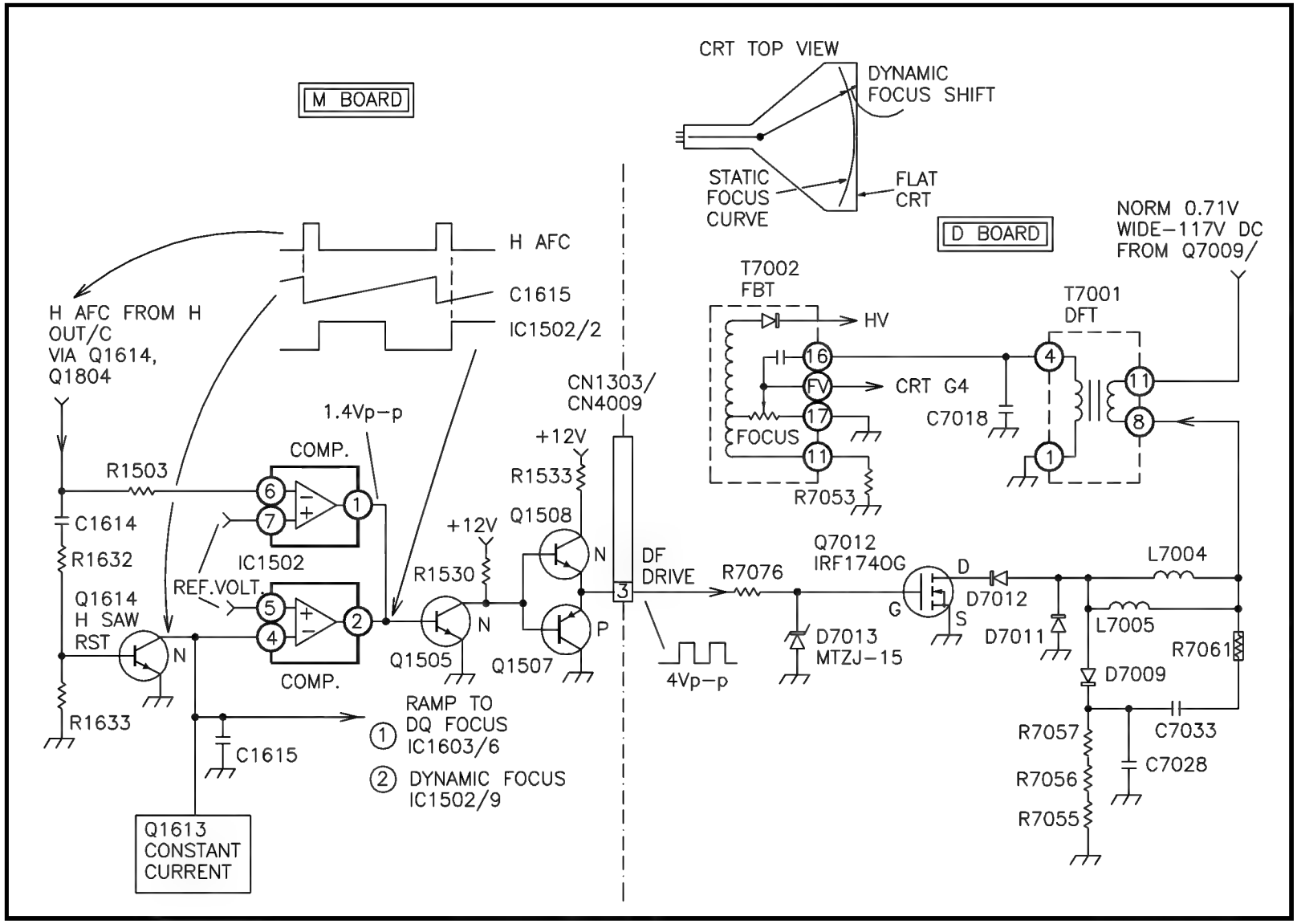


Operational test

To prove the device is functional:

1. Connect the negative lead of the ohmmeter to the SOURCE lead.
2. Touch the ohmmeter positive lead to the gate to pre-charge it.
3. Connect the ohmmeter positive lead to the DRAIN.

If the device is good you will get a resistance reading of about 400-1k ohms.



DYNAMIC FOCUS 2 – LOCATION

HDTV32 1060 3 9 99

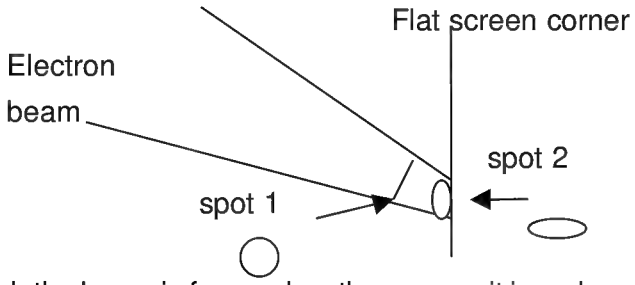
Dynamic Quadrapole Focus

There are three types of electron beam focus circuits used in this flat screen TV:

Static focus – A DC voltage is applied to the picture tube's focus grid. This produces a line of focus points forming an arc pivoting at the yoke where the beam is swept. The focus point can be moved toward or away from the yoke by changing the DC focus voltage.

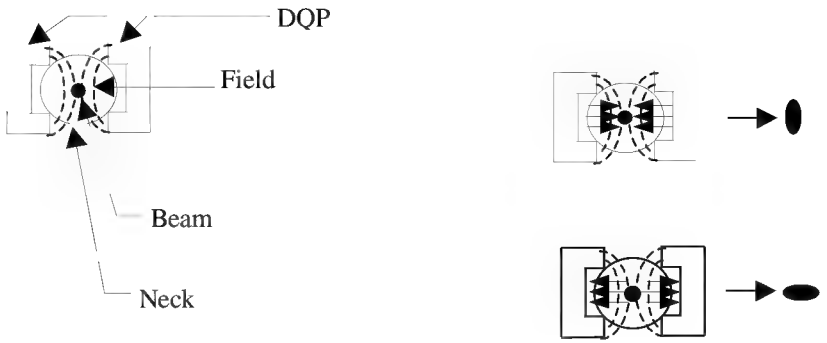
Dynamic focus – The electron beam must focus on the screen. Because the picture tube screen is flat and does not match the focus arc, the dynamic focus circuitry moves the focus point up on the left and right sides to meet the flat screen.

Dynamic Quadrapole focus – Static focus places a round focused spot at any point along the focus arc, perpendicular to the electron beam (spot 1). This focus point was moved to the flat screen with dynamic focusing.



Although the beam is focused on the screen, it is no longer round (spot 2) because of the angle the beam strikes the screen. One side of the electron beam that strikes the screen (spot 2) travels further, forming an oval instead of a circle. This oval shape is pronounced at the four corners of the screen if this correction circuit becomes inoperative. This quadrapole focus circuit reshapes the spot by using the magnetic field from four coils mounted at the picture tube neck.

The four QP coils work in magnetic pairs; either pushing or pulling the beam so it is oblong in transition but round at the target screen. The diagram shows the effects of two facing QP coils:



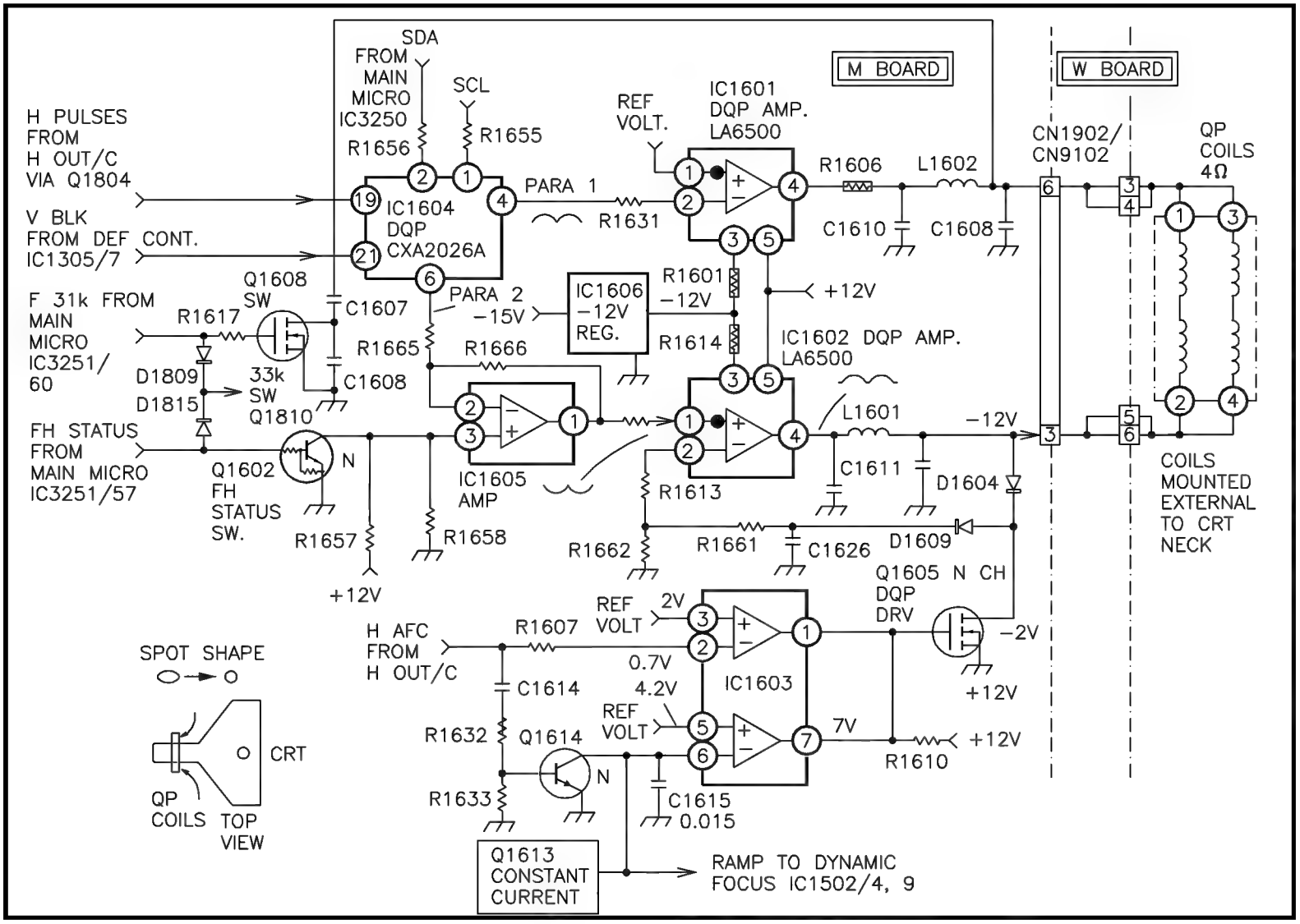
Dynamic Quadrapole Circuitry

To reshape the spot in the four corners of the picture tube, horizontal and vertical scanning signals are necessary to locate those corners. They are input to the DQP Control IC1604 at pins 19 and 21. Serial data and clock are input to control the amount of correction signal that outputs as Parabola signals 1 and 2 (IC1604/pins 4 and 6).

IC1604 Quadrapole focus Correction		
Input Name	Input to	Outputs
Horiz AFC from Horiz Out Q1804/Collector	DQP IC1604/pin 19 Horizontal pulses	Quadrapole correction: Parabola 1 from IC1604/pin 4
Vertical Blanking pulses from IC1305/7	DQP IC1604/pin 21 Vertical pulses	
Serial Data bus from Main Micro IC3251/pin 31	DQP IC1604/pin 1	Quadrapole correction: Parabola 2 from IC1604/pin 6
Serial Clock bus from Main Micro IC3251/pin 28	DQP IC1604/pin 2	

DQP Drive

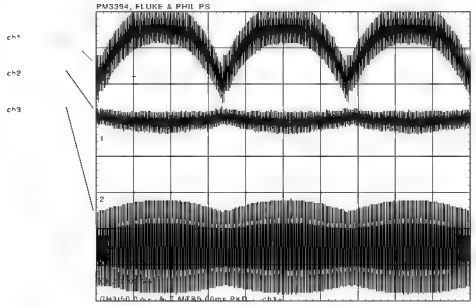
Parabola 1 output from IC1604/pin 4 is current amplified by IC1601 before being applied to the QP coils. Parabola 2 is inverted by IC1605 before also being current amplified by IC1602. The inverted signal is applied to the other end of the QP coils.



DYNAMIC QUADRAPOLE FOCUS (DQF)

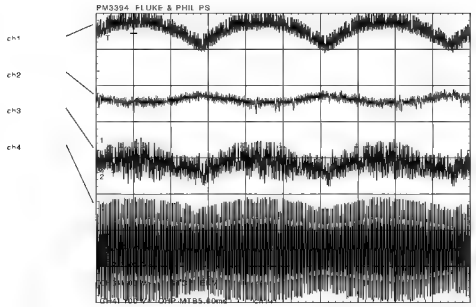
HDTV26 1059 3 9 99

The first scope shot shows the parabola 1 signal processing from its beginning at IC1604/pin 4 (ch 1) to the QP coils (ch 3)



Waveform DQP1 – Parabola 1 Process			
	Name	Location	Voltage
Channel 1	Parabola 1	IC1604/pin 4	6Vp-p
Channel 2	Driver output	IC1601/pin 4	1Vp-p
Channel 3	Signal at QP coil	CN1902/pin 6	135Vp-p
Channel 4			
Time base	5msec/div		

The second scope shot shows the parabola 2 signal processing from its beginning at IC1604/pin 6 (ch 1) to the QP coils (ch 4)



Waveform DQP2 – Parabola 2 Process			
	Name	Location	Voltage
Channel 1	Parabola 2	IC1604/pin 6	2Vp-p
Channel 2	Inverter output	IC1605/pin 1	1Vp-p
Channel 3	Driver output	IC1602/pin 4	1.5Vp-p
Channel 4	Signal at QP coil	CN1902/pin 3	300Vp-p
Time base	5msec/div		

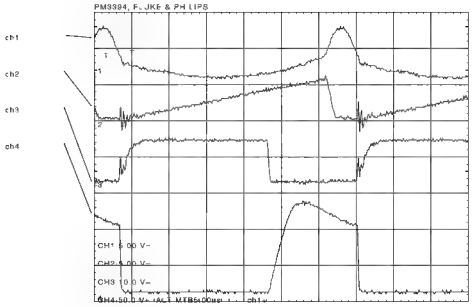
DQP Magnetic field Drive

The Dynamic Quadrapole correction signals were provide by parabola 1 and 2. The higher current used to manufacture the large magnetic fields in the QP coils and introduce the lower 60 Hz frequency parabola signals into the horizontal frequency scan are created by IC1603 and Q1605.

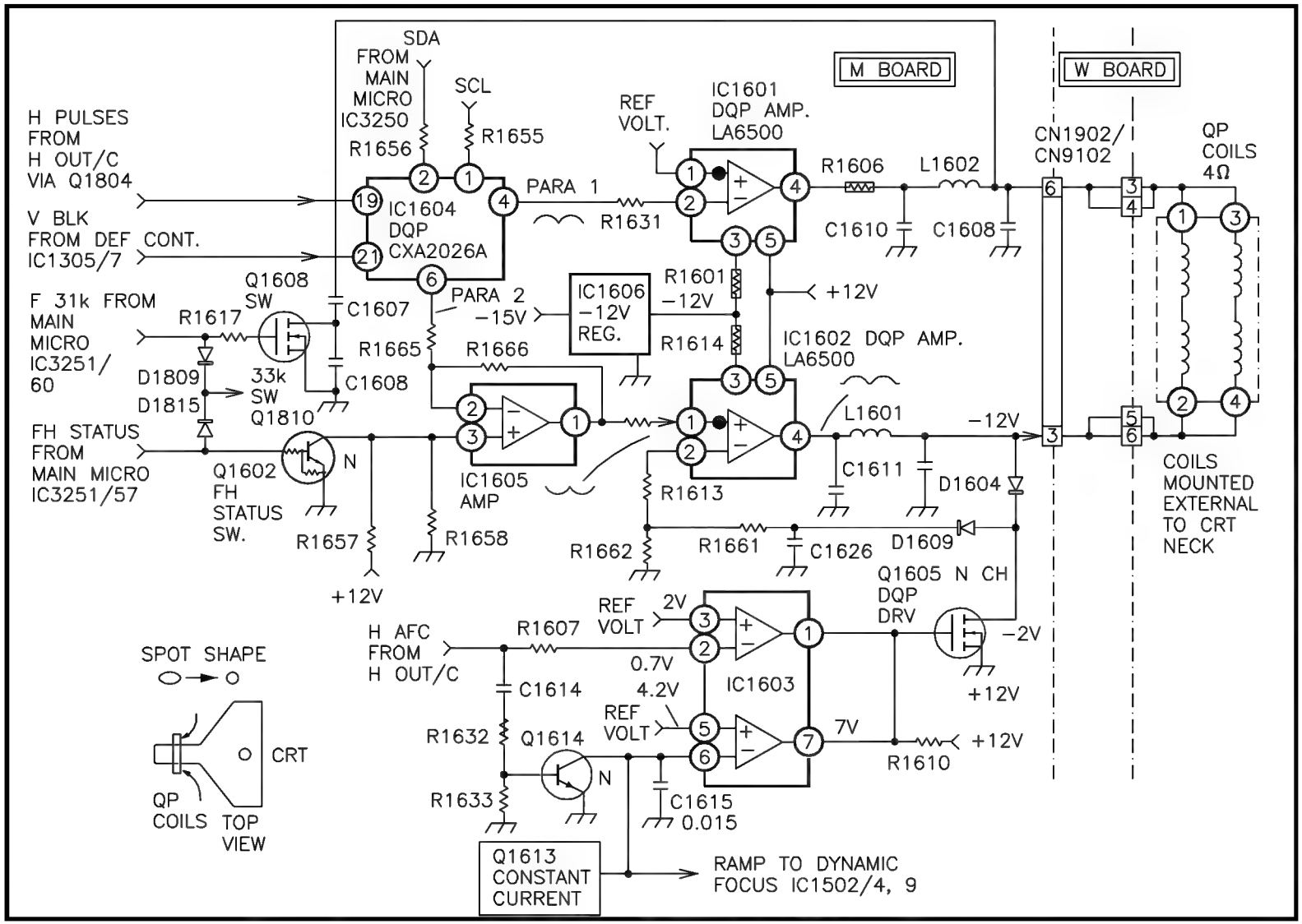
The source of this drive signal is comparator IC1603. It manufactures a pulse to mark the areas of the screen that need to be corrected. The circuit begins when a horizontal ramp is formed by C1616 at IC1603/pin 6. The output of this comparator is a low pulse at IC1603/pin 7.

Because the pulse ends at the beginning of the next horizontal cycle, the second comparator in IC1603/pins 2-1 is used to extend this low pulse through the horizontal retrace interval. This second comparator inverts the positive horizontal pulse and outputs it as a low pulse in parallel with the first comparator output to keep the output low.

This low going output pulse begins just before the horizontal interval and is applied to DQP driver Q1605. This drive signal applies the parabola 1 and 2 signals to the right and left areas of the screen by permitting QP correction current to flow through the QP coils at this time.



Waveform DQP3 – Magnetic field Drive			
	Name	Location	Voltage/div
Channel 1	FBT pulse	FBT	N/A
Channel 2	H ramp	IC1603/pin 6	7Vp-p
Channel 3	Drive pulse	IC1603/pin 7	12Vp-p
Channel 4	QP Drive signal	Q1605/Drain	135Vp-p
Time base	5usec/div		

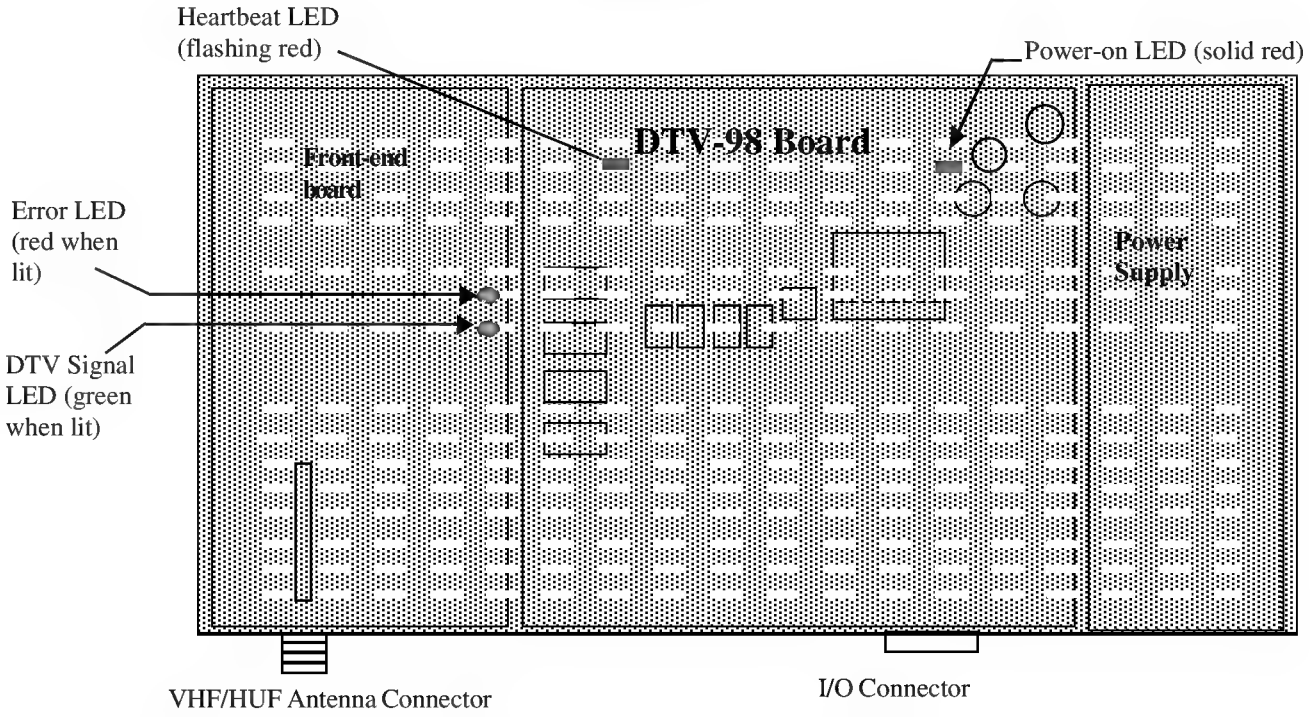


DYNAMIC QUADRAPOLE FOCUS (DQF)

HDTV26 1059 3 9 99

Appendix

Set-Back Box



Power-on LED (red): Lit whenever SBB is powered on.

Heartbeat LED (red): Flashes at a steady rate when unit is powered on; indicates that SBB operating program is running.

DTV Signal LED (illuminates green when DTV signal is being received): Should be on steady when the TV is tuned to a DTV station in the customer's reception area and the customer has a good antenna that is pointed properly.

Error LED (illuminates with a flash of red light whenever a non-correctable error is detected in the DTV data).

When the TV is tuned to a valid DTV channel, the Power-on LED should be on steadily, the heartbeat LED should be flashing, the DTV Signal LED should be lit.

Using LEDs inside the Set-back Box ("SBB") as troubleshooting tools.

There are four LEDs inside the SBB that can be used to identify certain levels of functionality. **The LEDs can be seen by looking through the vent slots in the SBB top cabinet.** Two are mounted on the tuner board (also known as "Front-end" or "FE" board), and two are mounted on the main board (also known as the DTV-98 board).

The red power LED on the DTV-98 board should be on whenever the SBB is powered on by a control signal from the TV. In practice, the power LED should be on whenever the I/O cable is connected and the TV is also powered on.

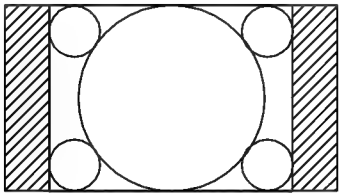
Another red LED on DTV-98 board is the "heartbeat" LED, which should be flashing at a steady rate whenever the SBB is on. This heartbeat indicates that the operating program used to run the CPU in the SBB is running properly, i.e. the program is not locked up.

The two LED's on the front-end board may be clear in color when they are not lit, but when lit, one will be red and the other will be green. When the SBB is receiving a valid DTV signal **on the physical channel it is tuned to**, the green LED will be lit. The red led will light only when a valid DTV signal is being received (green LED is lit) and errors in the received data could not be corrected by the SBB's error correction software. Very often, a non-recoverable error (red LED on the front-end board flashed) will be accompanied by a viewable abnormality in the picture (digital artifacts such as pixelization, tiling, blocking, and freezing). The best installation is one where the green LED is lit when the SBB is tuned to a valid DTV channel and the red LED never illuminates

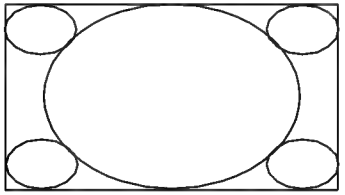
NTSC TRANSMISSION PICTURE SIZE MODES	
1. NORMAL 4:3 ASPECT RATIO	4. WIDE ZOOM
2. FULL 16:9 ASPECT RATIO	5. CLOSED CAPTION (TOP & BOTTOM COMPRESSED)
3. ZOOM	6 TWIN VIEW

SD DTV 4:3 ASPECT RATIO TRANSMISSION PICTURE SIZE MODES	
1. NORMAL 4:3 ASPECT RATIO	4. WIDE ZOOM
2. FULL 16:9 ASPECT RATIO	5. CLOSED CAPTION (TOP & BOTTOM COMPRESSED)
3. ZOOM	6 TWIN VIEW

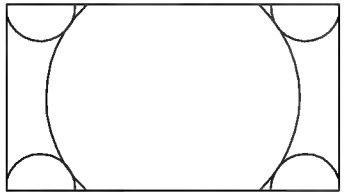
HDTV OR SD DTV 16:9 TRANSMISSION PICTURE SIZE MODES
1. FULL
2. TWIN VIEW



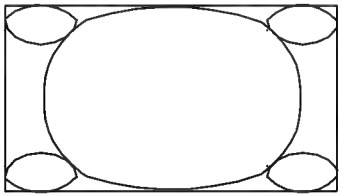
NORMAL



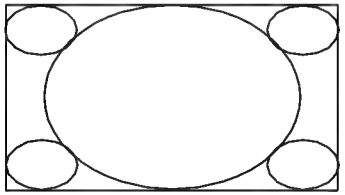
FULL
EXPANDED



ZOOM
EQUALLY EXPANDED



CLOSED CAPTION
BOTTOM COMPRESSED



WIDE ZOOM
TOP/BOTTOM COMPRESSED

PICTURE SIZE MODES

HDTV37 1089 2 23 99

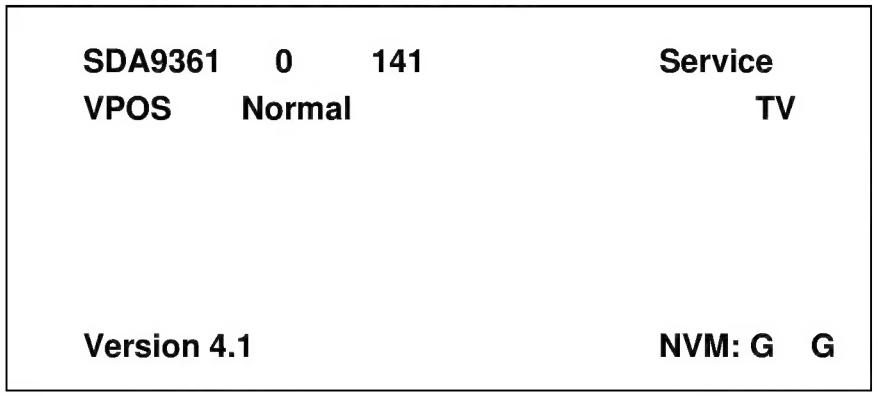
Board Replacement

Board Removal	Functions	Possible Failure Symptom(s)	After board replacement
A The A board is plugged into the G board and secured with a plastic L bracket. Remove the plastic L bracket from the G board by squeezing the tabs under the G board.	Input Video & DVD switching, Y/C separation, Closed Caption, Main and Sub tuners and picture processing.	1. Loss of color, or luminance (B & V boards also possible). 2. Inability to receive TV, PIP, Video, DVD or standard definition (SD) Digital TV. (B board also possible). 3. No closed caption in the main or sub pictures.	May have to program TV stations in again for faster station capture. Verify PIP, DVD and Video inputs work.
V The V board is plugged into the G board. Pry the socket tabs outward while rocking the V board out.	Digital processing for standard definition (525 line) input, PIP processing.	1. Solariztion (bright splotches in the picture). 2. Large squares in the picture. 3. One picture missing in twin view (A board also possible). 4. Noise in the main picture but not in the Twin View. 5. Loss of color, or luminance (A & B boards also possible). 6. Standby light blinks 6 times pauses and repeats (+5VOCP)	Verify main NTSC and Twin View pictures. Transplant shielding to new board. Check to see that contrast and color levels are similar when switching between NTSC and DTV pictures. If not, follow the procedure is on pages ___ of the adjustment manual.
B The B board is plugged into the G board and secured with a plastic L bracket. Remove the plastic L bracket from the G board by squeezing the tabs under the G board. Note that white connectors CN3002 & CN3007 are not used.	Main Micro Processing, Sound Effect Processing for Dolby inputs, Video Processing, Video & some deflection memory.	1. No OSD menu or channel numbers (also no sync from D, or M, board). 2. No or constant audio or video muting. 3. Inconstant contrast or color between the Twin View pictures, Full width NTSC and DTV pictures. 4. Distorted or no sound effects (Thru-Sourround and Simulated). 5. Can not select Main Video and/or HDTV video signal from the set-back box (Setback box also possible). Sound switches OK but no video. 6. No vertical or horizontal sync (M board also possible). 7. Will not hold last volume level at power off. 8. Will not hold individual settings for the 7 picture sizes (normal, full, zoom, etc). 9. Standby light blinks 5 times pauses and repeats (IK white balance failure).	♦ Transplant memory IC3252 in an anti -static atmosphere or ♦ Enter the service mode and press 08 enter to load defaults into a blank memory. ♦ Adjust the contrast, color level and hue for the two Twin View pictures, Full width NTSC and DTV picture so the picture is of equal contrast and color intensity as the pictures are switched. The procedure is on pages ___ of the adjustment manual. ♦ Perform the size adjustments for all the 7 picture sizes (normal, full, zoom, etc) on pages _____ of the adjustment manual.

M The M board is held down with two screws.	Channel and picture size memory, Picture width control, H & V oscillator, Picture tilt, Dynamic focus, Pincushion.	1. No VHF/Cable channel memory (no channel up/down function). 2. Picture convergence, size, position, pincushion can not be adjusted or will not hold in memory. 3. Picture changes in size (horizontally and vertically). 4. No picture sync (B board also) 5. Shutdown (G & D boards also) 6. Poor focus at sides/corners.	Transplant memory IC1304 in an anti - static atmosphere or load default data for SDA9361 and DM groups. Perform the size adjustments for all the 7 picture sizes (normal, full, zoom, etc) on pages _____ of the adjustment manual.
D Four screws	Horizontal Output Vertical Output Horiz. Centering Dynamic Focus Output	1. Shutdown (M & G boards also). See Protection Circuit 3 for procedure to determine if this board is at fault. 2. Standby light blinks 2 times pauses and repeats (OCP). 3. Standby light blinks 4 times pauses and repeats (No Vert).	Touch up adjustments of picture size and position. (picture distortion adjustments are on page __ of the adj manual.)
G Remove rear panel & ground shield. Unscrew board and lift out with 3 boards plugged into it. Unclamp the outer 2 (A & B) boards that plug into the G board from the bottom and unplug the middle V board.	Power Supply	1. Dead set (D & K boards also). 2. Shutdown (D & M, C, & K boards also. K = audio output) 3. Standby light blinks 3 times pauses and repeats (OVP). 4. Standby light blinks 6 times pauses and repeats (+5V OVP. V board also possible as +5V OCP).	Inspect picture for noise due to loose shielding on adjacent plug in boards.
K 1 screw and plastic flap at rear panel.	Audio Output	Dead set (D & G boards also).	Check that both channels are at equal volume.
C	CRT Drive	5. Shutdown (D & M, G, & K boards also). 1. Standby light blinks 5 times pauses and repeats (IK white balance failure). (B board also).	None

Service Mode Display

Service mode initial display:



Description of the Service Mode Information			
Initial display example	Other names	Description	Bd
SDA9361 (Names of register Groups. IC name is often used)	SDA9361	Deflection parameters IC1305 (Each register has data corresponding to the 7 pix geometry modes).	M
	DM	Convergence/Focus. IC1701 (Each register has data corresponding to the 7 pix geometry modes).	M
	CXA8070	Static Convergence IC1402 (Each register has data corresponding to the 7 pix geometry modes).	M
	DEF-Adj	Horiz position/size. D/A Conv IC1701-2 (Each register has data corresponding to the 7 pix geometry modes).	M
	C2101-1	Video Drive. Processor IC3005	B
	C2101-2	Input Select, AKB. Processor IC3005	B
	C2101-3	Pix Masking/Cropping Processor IC3005	B
	C2101-4	Contrast, bright, color (main and DTV) Processor IC3005	B
	Chroma 1	Main Pix Contrast, bright, color. IC2404	A
	Chroma 2	Sub Pix Contrast, bright, color. IC2403	A
	CXD2053	Data is fixed at 0. This IC is not used in the USA set.	
	AP	Volume, Balance, T&B. Audio IC3103	B
	TC9447F	Surround Processor IC3101	B
	3DHH	Main Signal Comb filter IC2202	A
	MID	Twin View Process IC506	V
	DTV	DTV's V & H Position	
	FE	Set-back box data loaded during DTV auto-programming.	
	OP	OSD, main, sub pix position	
VPOS	various	Individual adjustment register names	
0		Each adjustment register is numbered.	
141		Data representing the level of adjustment	
Service	none	The word identifies service mode entry.	
TV	Video 1-3, DVD, HD-no sync.	Identifies the input used for the display.	
NVM:G G	NVM:NG G NVM:G NG	Displays the condition of the Non-Volatile Memory ICs. The first G = IC3252 on the B board. The second G = IC1304 on the M board.	
Version: 4.1		Main Micro version	

Adjustment Data by Geometry

Some registers contain data that is stored in a single memory location. Other registers have multiple memory locations. These multiple memory registers have data stored by picture geometry.

There are seven picture geometry modes

1. Normal – 4:3 aspect ratio picture with black borders.
2. Full - 4:3 picture stretched to fill the 16:9 picture tube.
3. Caption – Full picture but compressed on bottom to see lettering.
4. Zoom – 4:3 picture expanded horizontally and vertical to maintain the aspect 4:3 ratio of the picture.
5. Wide Zoom – Full picture but equally compressed on top and bottom.
6. SD – DTV – Standard definition digital reception presented in the transmitted 4:3 or 16:9 aspect ratio.
7. HD – DTV – High definition digital reception presented in the transmitted 16:9 aspect ratio.

When the geometry is changed, the data may be different for each of the pictures. For example in the HSIZ (horizontal size) register within group SDA9361, the data for a normal picture and a full picture will be different because the pictures are of different widths. However, it is expected that the horizontal data to be the same between the full and caption geometry modes since the horizontal width is the same (only the vertical linearity is different).

Number of Memory Locations per Register		
Register Group Name	Number of memory locations/register	Memory Location Names (Geometry modes)
SDA9361	7	Normal, Full, Caption, Zoom, Wide Zoom, SD-DTV, HD-DTV.
DM	7	Normal, Full, Caption, Zoom, Wide Zoom, SD-DTV, HD-DTV.
CXA8070	7	Normal, Full, Caption, Zoom, Wide Zoom, SD-DTV, HD-DTV.
DEF-Adj	7	Normal, Full, Caption, Zoom, Wide Zoom, SD-DTV, HD-DTV.
C2101-1	3	Normal, HD-DTV, and the 5 others.
C2101-2	2	HD-DTV, and the 6 others
C2101-3	2	HD-DTV, and the 6 others
C2101-4	1	The data is the same regardless of the geometry modes.
Chroma 1	1	The data is the same regardless of the geometry modes.
Chroma 2	1	The data is the same regardless of the geometry modes.
CXD2053	0	Not used in this set.
AP	1	The data is the same regardless of the geometry modes.
TC9447F	1	The data is the same regardless of the geometry modes.
3DHH	2	HD-DTV, and the 6 others
MID	2	HD-DTV, and the 6 others
DTV	1	The data is the same regardless of the geometry modes.
FE	1	The data is the same regardless of the geometry modes.
OP	1	The data is the same regardless of the geometry modes.